CW1051

3~5 Channel Secondary Protection IC

Features

- 3~5 Cells Application
- Overcharge Protection
  - Threshold from 4.100V to 4.500V
  - 25mV Steps, ±25mV Accuracy
- Internal Overcharge Protection Delay Time
- Overcharge Delay Counter Reset Time
- Open Wire Protection
- Low Power Dissipation
  - Normal Working 4μA (25°C)
- Package Type: MSOP8L, DFN3*4-8L

Applications

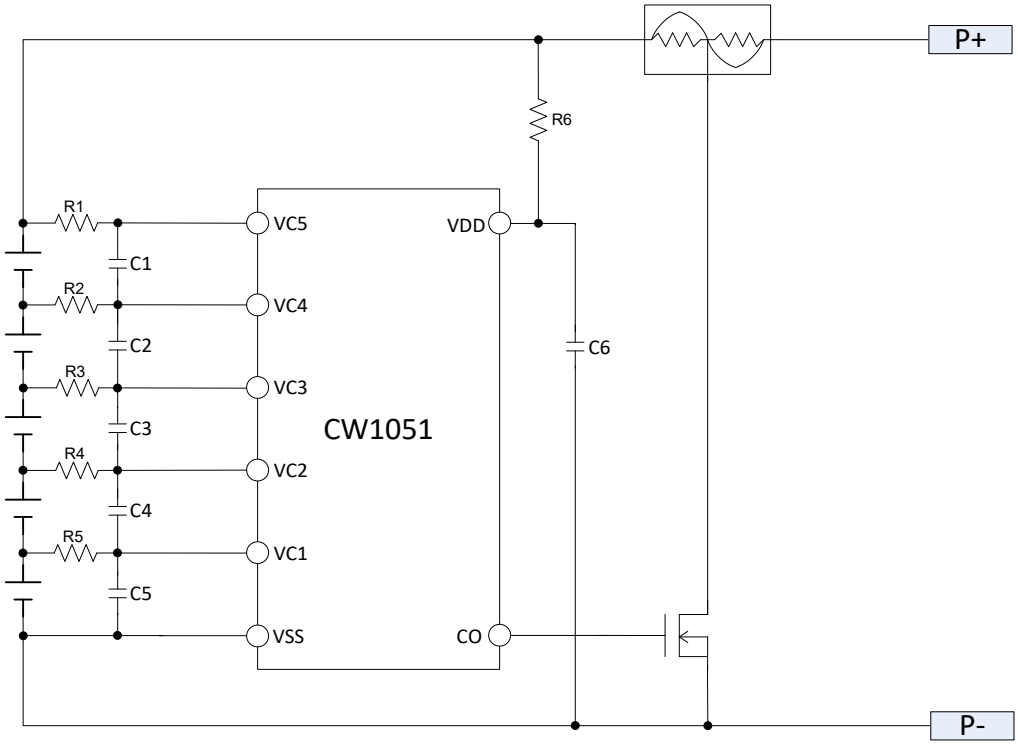
- NoteBook
- Tablet PC
- E-Tools
- Backup Power Supply
- Other Lithium-ion or Lithium Polymer Battery Packs

General Description

The CW1051 series products are highly integrated secondary protection ICs for 3 to 5 lithium-ion and lithium polymer battery cells connected in series. CW1051 provides overcharge protection for battery pack by measuring each cell's voltage.

Application Circuits

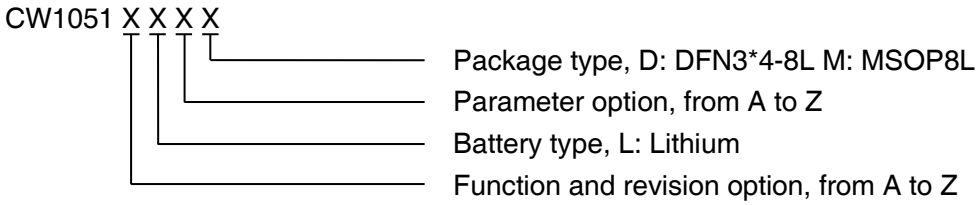
For 5 cell connect in series（CMOS, Active H）



Recommended parameter

SYMBOL	TYPICAL	RANGE	UNIT
R1,R2,R3,R4,R5	1000	200~2000	Ω
R6	200	200~1000	Ω
C1,C2,C3,C4,C5	0.1	0.1~0.22	μF
C6	0.1	0.1~0.47	μF

Product Name



Ordering Information

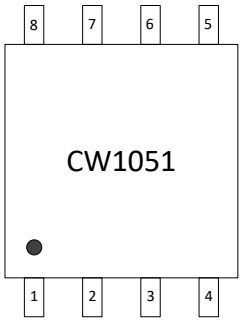
TYPE	OVER CHARGE THRESHOLD [VOC] (V)	HYSTERESIS VOLTAGE*1 [VHYS] (V)	DELAY TIME*2 [TOC] (S)	OUTPUT TYPE*3
CW1051ALAM	4.220	0.300	1	CMOS, Active H
CW1051ALAD				
CW1051ALBM	4.220	0.050		CMOS, Active L
CW1051ALBD				
CW1051ALCM	4.350		6	CMOS, Active H
CW1051ALCD				
CW1051ALDM	4.400		1	
CW1051ALDD				
CW1051ALEM	4.220			
CW1051ALED				
CW1051ALFM	4.300	0.300	4	
CW1051ALFD				
CW1051ALGD	4.300		1	
CW1051ALHD	4.275	0.050	2	NMOS open drain, Active L
CW1051ALHM				
CW1051ALJM	4.250	0.100	1	CMOS, Active H
CW1051ALKM	4.220			NMOS open drain Active L
CW1051ALLM	4.250	0.300		CMOS, Active L
CW1051ALMM	4.200	0.050		NMOS open drain Active L
CW1051ALMD	4.200	0.050		
CW1051ALOM	4.250	0.100	4	CMOS, Active H
CW1051ALPM	4.175	0.100	1	CMOS, Active L
CW1051ALQD	4.350	0.300	4	CMOS, Active H

*1 Optional hysteresis voltage: 0V, 0.050V, 0.100V, 0.300V

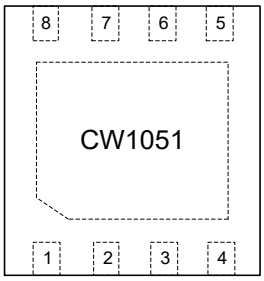
*2 Optional delay time: 1s, 2s, 4s, 6s

*3 Optional output type: CMOS active H, CMOS Active L, PMOS open drain Active H, PMOS open drain Active L, NMOS open drain Active H, NMOS open drain Active L

Pin Configuration



MSOP8L Package



DFN3*4-8L Package

Pin Descriptions

PIN	NAME	DESCRIPTION
1	VDD	Power supply
2	VC5	Positive input of cell5
3	VC4	Positive input of cell4
4	VC3	Positive input of cell3
5	VC2	Positive input of cell2
6	VC1	Positive input of cell1
7	VSS	Ground
8	CO	Overcharge output driver

Absolute Maximum Ratings

		VALUE		UNITS
		MIN	MAX	
PIN voltage range respect to VSS	VDD, VCx	-0.3	36	V
PIN voltage range respect	CO	-0.3	VDD+0.3	V
Operation Temperature		-30	85	°C
Storage Temperature	T_{stg}	-40	125	°C

Caution:

Stresses beyond "Absolute Maximum Ratings" condition may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VDD Input Voltage Range	V_{DD}		4.5		28	V
VCx Input Voltage Range	V_{Cx}		0		4.5	V

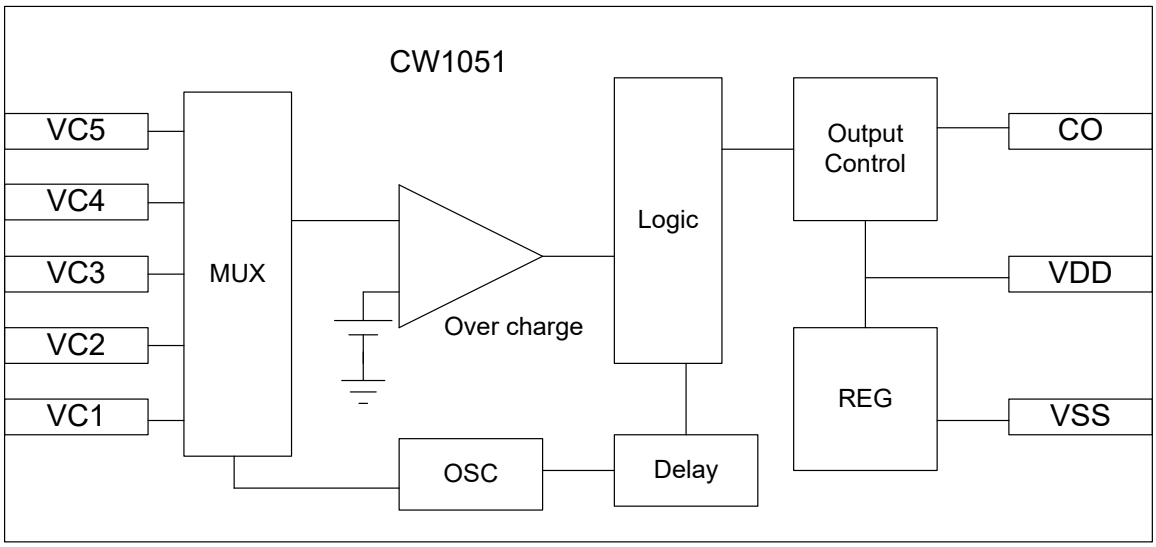
Electrical Characteristics

Operation under 25°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CURRENT						
Operation Current	I_{OPR}	VC1=VC2=VC3=VC4=VC5=3.7V		4	7	μA
VOLTAGE/TEMPERATURE DETECT AND PROTECTION THRESHOLD						
Overcharge Threshold	V_{OC}	VC1=VC2=VC3=VC4=3.7V Sweep VC5 from 3.7V to 4.5V	V_{OC}-0.025	V_{OC}	V_{OC}+0.025	V
Overcharge Threshold in whole Temperature Range		From -5°C to 55°C	V_{OC}-0.040	V_{OC}	V_{OC}+0.040	V
OC Release Threshold V_{OCR}=V_{OC}-V_{HYS}	V_{OCR}	VC1=VC2=VC3=VC4=3.7V Sweep VC5 from 4.5V to 3.7V	V_{OCR}-0.025	V_{OCR}	V_{OCR}+0.025	V
ACTION DELAY						
Overcharge Delay	T_{OC}	VC1=VC2=VC3=VC4=3.7V Sweep VC5 from 3.7V to 4.5V	0.80* T_{OC}	T_{OC}	1.30* T_{OC}	s
Overcharge Release Delay	T_{OCR}	VC1=VC2=VC3=VC4=3.7V Sweep VC5 from 4.5V to 3.7V		5		ms
Overcharge Reset Delay	T_{RESET}			20		ms
Open-wire Detection Delay	T_{OW}	Input capacitor = 0.1μF		2		s
Open-wire Release Delay	T_{OWR}			10		ms
PIN OUTPUT VOLTAGE						
CO Logic High Output	V_{OC}	VC1=VC2=VC3=VC4=VC5=3.7V	VDD-0.3			V
CO Logic Low Output*[1]		VC1=VC2=VC3=VC4=VC5=4.5V			0.3	V
PIN DRIVE ABILITY						
CO High Output Drive Ability	CO	CO logic HIGH		20		μA
CO Low Output Drive Ability		CO logic LOW		0.5		mA

*[1] There is several output types, detail please refer to the product selection table. Take CMOS Active H for example here.

Functional Block Diagram



Notes: Some buffer blocks omitted

Detailed Description

Normal State

CW1051 works under a normal state when each cell voltage is less than Voc.

Overcharge State

When any cell voltage becomes higher than overcharge threshold voltage (V_{OC}) and stays longer than overcharge protection delay time (T_{OC}), CO will output a high-level signal, and CW1051 enters over charge state. CO signal can be used to inform the external device or control the MOSFET. If within Toc, cell voltage drops lower than V_{OC} but stays shorter than overcharge reset delay time (T_{RESET}) before rising up over V_{OC} again, this spike will be ignored. Otherwise, accumulated delay time of overcharge will be reset. Overcharge protection state will release when all the cell voltages are less than the overcharge release threshold (V_{OCR}) and stay longer than the release delay time (T_{OCR}).

Open-wire Detection

Any wire connected between the battery cell and IC will be monitored.
When the wire disconnects and maintains (T_{OW}) time, IC will enter to the open-wire protection state.
CO outputs a high-level voltage to cut off the charge loop.
Open-wire protection will release when all wires reconnect and stay longer than the release delay time (T_{OWR}).

Test Mode

Test mode is used to reduce the protection delay time for test of mass production.
CW1051 will enter the test mode when add a VDD+7V voltage on VDD pin and maintains 80ms. Test mode lasts 8s then recovers to the normal status.
Detailed test mode timing is illustrated as bellow:

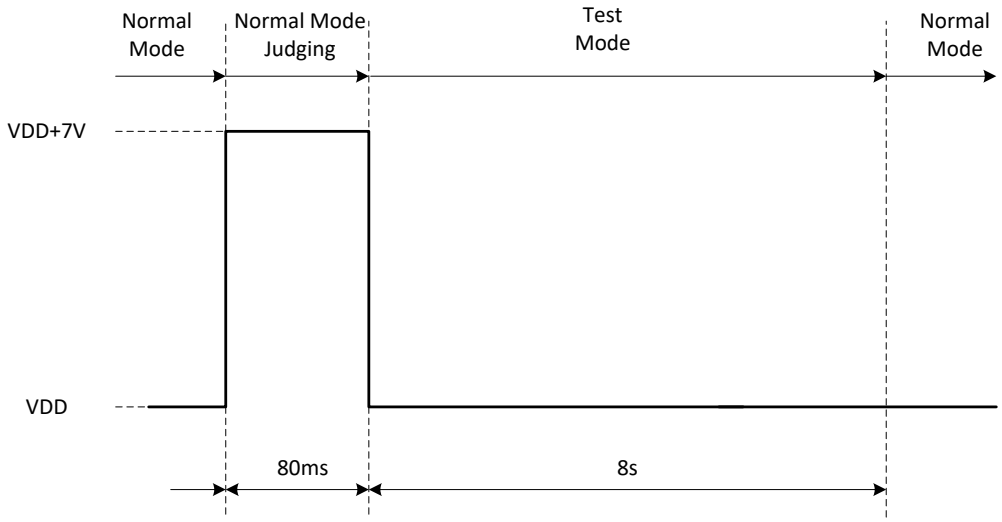
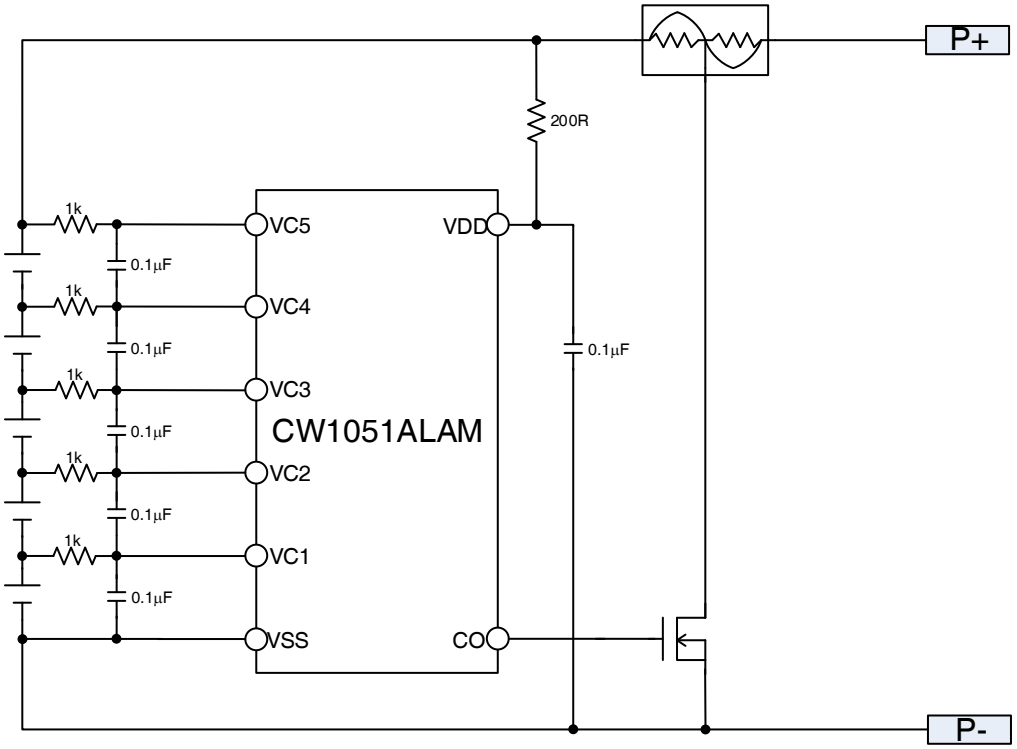
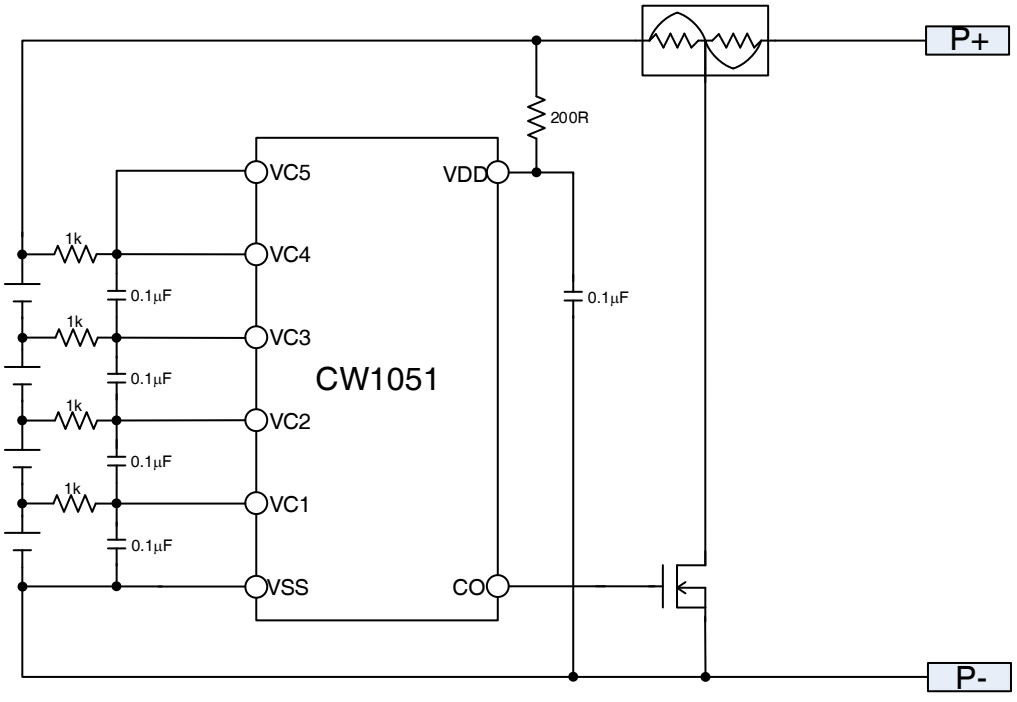


Figure 1. Test Mode Timing

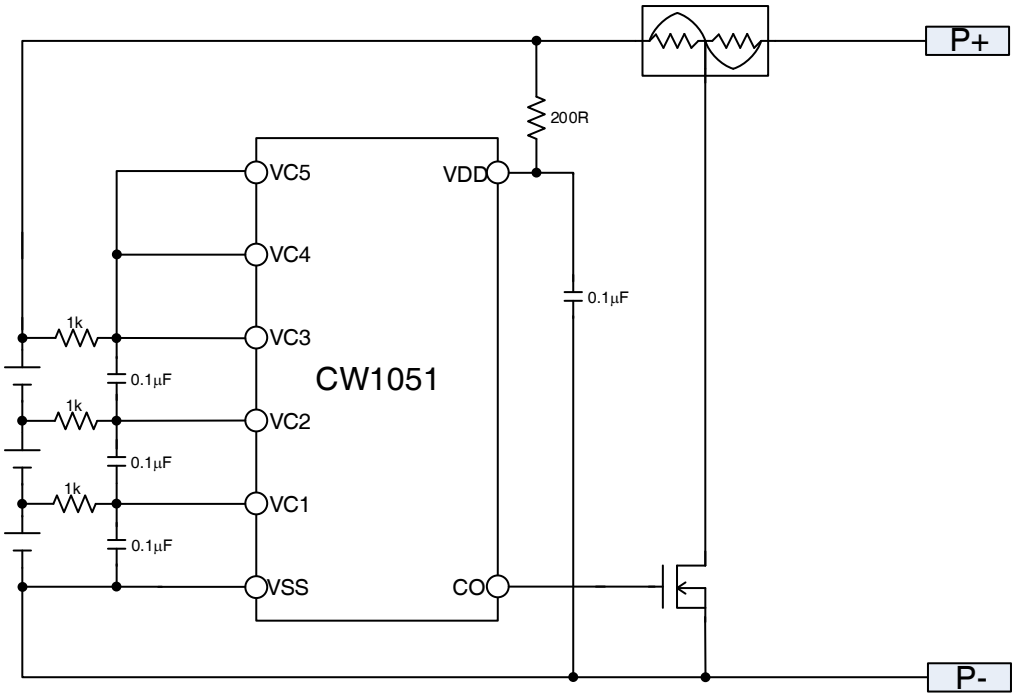
Reference Schematic



Reference Schematic for 5 cells



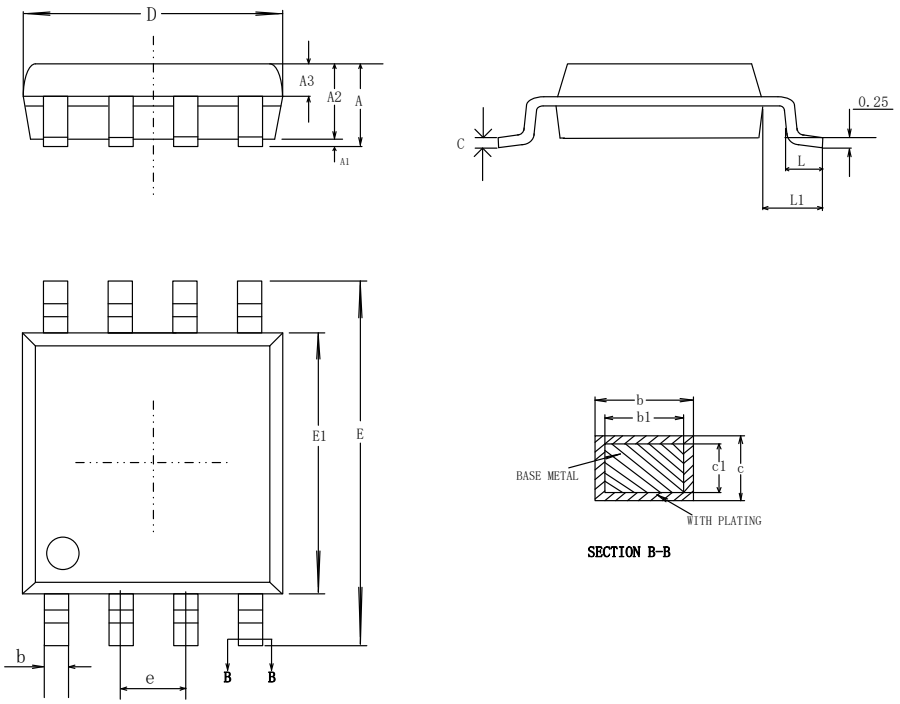
Reference Schematic for 4 cells



Reference Schematic for 3 cells

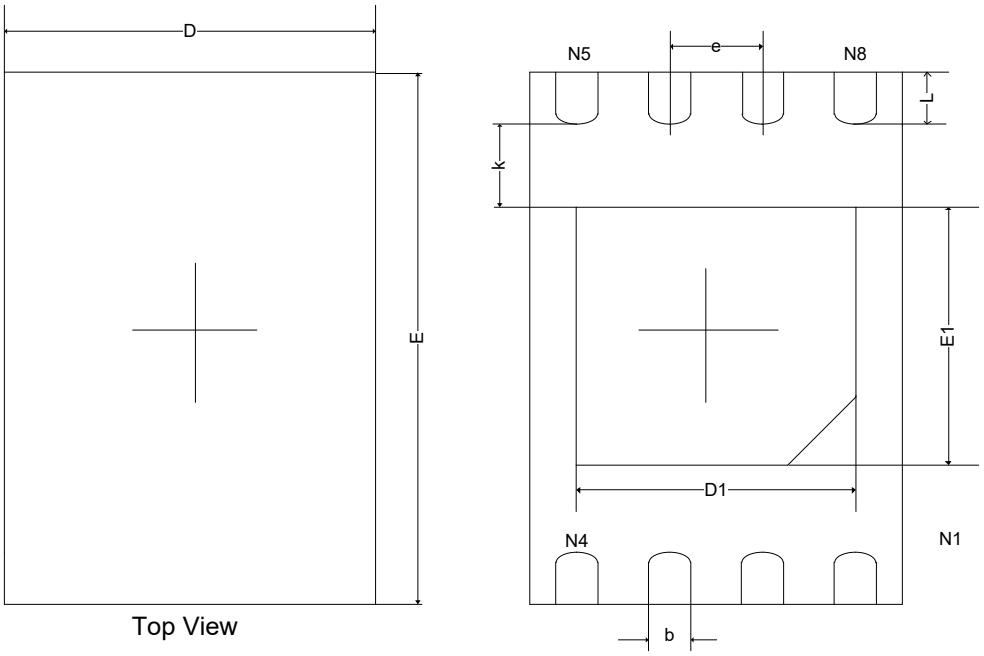
Package Information

MSOP8L PACKAGE OUTLINE DIMENSIONS



SYMBOL	MILLIMETER	
	MIN.	MAX.
A		1.10
A1	0.05	0.15
A2	0.75	0.95
A3	0.30	0.40
b	0.29	0.38
b1	0.28	0.33
c	0.15	0.20
c1	0.14	0.16
D	2.9	3.1
E	4.7	5.1
E1	2.9	3.1
e	0.65BSC	
L	0.40	0.70
L1	0.95BSC	

DFN3X4-8L PACKAGE OUTLINE DIMENSIONS



SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	-	0.02	0.05
A3	0.18	0.20	0.25
D	2.90	3.00	3.10
E	3.90	4.00	4.10
D1	2.20	2.30	2.40
E1	1.70	1.80	1.90
K	0.230MIN.		
b	0.15	0.20	0.25
e	0.65TYP.		
L	0.35	0.40	0.45

Revision History

DATE	VERSION	CHANGED ITEM	WRITTEN BY	APPROVED BY
2015-12-24	1.0	New document established	Kang	Jun
2016-07-10	1.1	1. Corrects the format 2. Revised Open-wire Detection Delay	Kang	Jun
2016-11-10	1.2	1.Revised CW1051ALAM parameter 2. Add CW1051ALEM Ordering Information	Kang	Jun
2017-08-02	1.3	Add CW1051ALFM/ALFD Ordering Information	Kang	Jun
2017-10-17	1.4	Add CW1051ALGD Ordering Information	Kang	Jun
2017-11-17	1.5	1. Add CW1051ALHD/ALJM/ALKM Ordering Information 2. Revised V_{OCR} parameter	Kang	Jun
2018-02-05	1.6	1.Add CW1051ALLM/ ALHM Ordering Information 2.Add Product Name 3.R6 parameter range modify to 200Ω~1000Ω. 4.CO PIN voltage range modify to -0.3V～VDD+0.3V.	Kang	Jun
2018-3-12	1.7	Add CW1051ALMM Ordering Information	Kang	Jun
2018-4-18	1.8	Add Reference Schematic	Kang	Jun
2018-6-19	1.9	Add CW1051ALOM\ ALPM\ ALQD Ordering Information	Kang	Jun

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