CA-IS374xC General Quad-Channel Digital Isolators

1. Features

- **Data rate: DC to 40Mbps**
- **Robust isolation barrier**
  - High lifetime: >40 years
  - Up to 5000 V_{RMS} isolation rating (Wide body packages)
  - ±150 kV/μs typical CMTI
- **Wide supply range: 3.0V to 5.5V**
- **Wide operating temperature range: -40°C to 125°C**
- **No start-up initialization required**
- **Default output *High* (CA-IS374xCH) and *Low* (CA-IS374xCL) Options**
- **High electromagnetic immunity**
- **Low power consumption**
  - 2.0mA per channel at 1Mbps with V_{DD} = 5.0V
  - 3.5mA per channel at 40Mbps with V_{DD} = 5.0V
- **Best in class propagation delay and skew**
  - 22ns typical propagation delay
  - 2.5ns propagation delay skew (chip -to-chip)
  - 1ns pulse width distortion
  - 20ns minimum pulse width
- **CMOS inputs logic**
- **Safety regulatory approvals**
  - VDE 0884-17 isolation certification
  - UL according to UL1577

2. Applications

- Industrial Automation
- Motor Control
- Medical Systems
- Isolated Power Supplies
- Solar Inverters
- Isolated ADC, DAC

3. General Description

The CA-IS374xC devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS digital I/O. Each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO_2) insulation barrier, and each channel input integrated Schmitt trigger to provide excellent noise immunity.

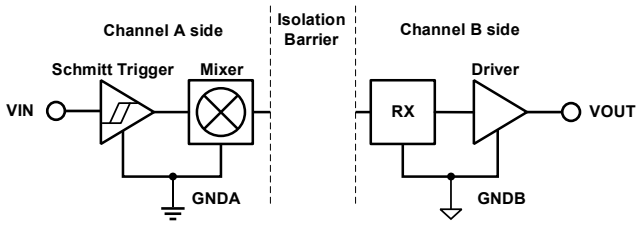
The CA-IS3740C features 4 channels transferring digital signals in one direction and output enable for the B side is active-high. The CA-IS3741C device has three forward and one reverse-direction channels, making it ideal for applications such as isolated SPI, RS-485 communication. The CA-IS3742C provides further design flexibility with two channels in each direction. When the input is either not powered or is open-circuit, the default output is low for devices with suffix L and high for devices with suffix H.

The CA-IS374xC family are specified over the -40°C to +125°C operating temperature range and are available in 8-pin SOIC narrow body package, 8-pin SOIC wide body package and 16-pin SOIC wide body package.

Device information

Part number	Package	Package size (NOM)
CA-IS3740C, CA-IS3741C, CA-IS3742C	SOIC16-WB(W)	10.30 mm × 7.50 mm

Simplified Channel Structure



GNDA and GNDB are the isolated grounds for A side and B side respectively.

4. Ordering Information

Table 4-1 Ordering Guide for Valid Ordering Part Number

Part Number	Number of Inputs A Side	Number of Inputs B Side	Default Output	Isolation Rating (kV_{RMS})	Package
CA-IS3740CLW	4	0	Low	5.0	SOIC16-WB (W)
CA-IS3740CHW	4	0	High	5.0	SOIC16-WB (W)
CA-IS3741CLW	3	1	Low	5.0	SOIC16-WB (W)
CA-IS3741CHW	3	1	High	5.0	SOIC16-WB (W)
CA-IS3742CLW	2	2	Low	5.0	SOIC16-WB (W)
CA-IS3742CHW	2	2	High	5.0	SOIC16-WB (W)

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5 Revision History

Revision	Description	Date	Page
Version 1.00	NA	2024.08.12	NA

6 Pin Descriptions and Functions

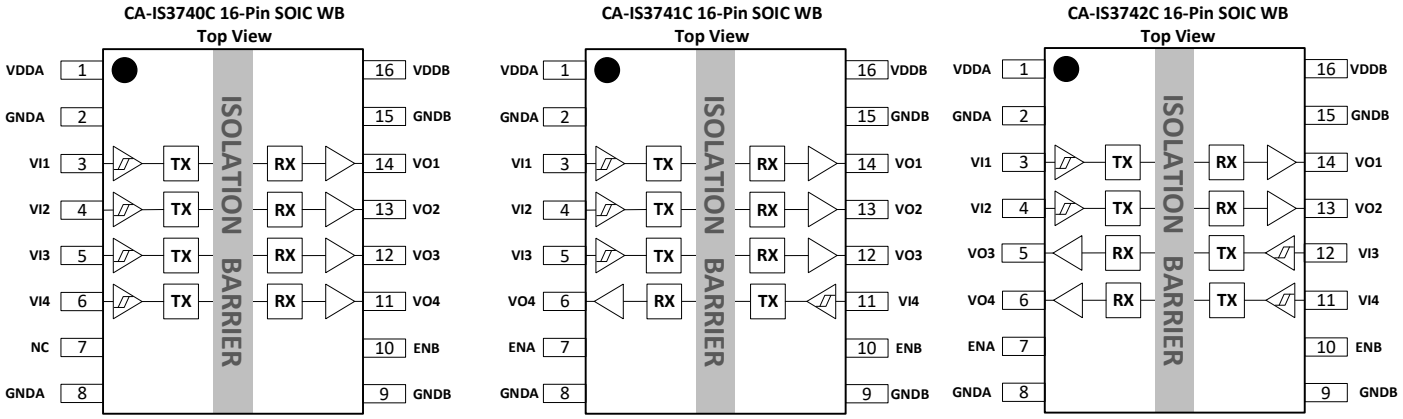


Figure 6-1. CA-IS374xC pin configuration

Table 6-1. Pin description for the CA-IS374xC 16-Pin Wide body SOIC packages

16-SOIC Pin#			Name	Type	Description
CA-IS3740C	CA-IS3741C	CA-IS3742C			
1	1	1	VDDA	Supply	Power supply for side A.
2, 8	2, 8	2, 8	GNDA	Ground	Ground reference for side A.
3	3	3	VI1	Digital I/O	Digital input 1 on side A, corresponds to logic output 1 on side B.
4	4	4	VI2	Digital I/O	Digital input 2 on side A, corresponds to logic output 2 on side B.
5	5	12	VI3	Digital I/O	Digital input 3 on side A/B, corresponds to logic output 3 on side B/A.
6	11	11	VI4	Digital I/O	Digital input 4 on side A/B, corresponds to logic output 4 on side B/A.
7	-	-	NC [1]	No Connect	Not internally connected. It can be left floating, tied to VDDA or tied to GNDA.
-	7	7	ENA[2]	Digital I/O	Output enable A. Output pin on side A is enabled when ENA is high or floating; Output pin on side A is open and in high-impedance state when ENA is low.
9, 15	9, 15	9, 15	GNDB	Ground	Ground reference for side B.
10	10	10	ENB[2]	Digital I/O	Output enable B. Output pin on side B is enabled when ENB is high or floating; Output pin on side B is open and in high-impedance state when ENB is low.
11	6	6	VO4	Digital I/O	Digital output 4 on side B/A, VO4 is the logic output for the VI4 input on side A/B.
12	12	5	VO3	Digital I/O	Digital output 3 on side B/A, VO3 is the logic output for the VI3 input on side A/B.
13	13	13	VO2	Digital I/O	Digital output 2 on side B, VO2 is the logic output for the VI2 input on side A.
14	14	14	VO1	Digital I/O	Digital output 1 on side B, VO1 is the logic output for the VI1 input on side A.
16	16	16	VDDB	Supply	Power supply for side B.

Notes:
1. No Connect. This pin is not internally connected. It can be left floating, tied to VDD_ or tied to GND.
2. Enable inputs ENA and ENB can be used to put the respective outputs in high impedance for multi master driving applications, external clock synchronization etc. With internal pull-up resistors, these pins can be connected to logic high or left floating to enable the outputs. If ENA, ENB are unused, it is recommended to connect these pins to a logic level, especially in the noisy environment.

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
V_{DDA}, V_{DDB}	Supply voltage[2]	–0.5	7.0	V
V_{IN}	Voltage at VIx, ENx	–0.5	$V_{DD\_}$ + 0.5[3]	V
I_O	Output current	–20	20	mA
T_J	Junction Temperature	–40	150	°C
T_{STG}	Storage Temperature	–65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to the local ground (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not exceed 7V.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, pins at same side	±8	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±2	

7.3 Recommended Operating Conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{DDA}, V_{DDB}	Supply voltage		3.0	3.3 or 5.0	5.5	V
$V_{DD\ (UVLO+)}$	V_{DDX} undervoltage-lockout threshold @ rising edge		2.55	2.7	2.85	V
$V_{DD\ (UVLO-)}$	V_{DDX} undervoltage-lockout threshold @ falling edge		2.35	2.5	2.65	V
$V_{HYS\ (UVLO)}$	V_{DDX} undervoltage-lockout threshold hysteresis		150	200	250	mV
I_{OH}	High-level output current	V_{DDO}[1] = 5V	-4			mA
		V_{DDO}[1] = 3.3V	-2			
I_{OL}	Low-level output current	V_{DDO}[1] = 5V			4	mA
		V_{DDO}[1] = 3.3V			2	
V_{IH}	High-level input voltage		0.7 × V_{DDI}[2]		V_{DDI}[2]	V
V_{IL}	Low-level input voltage		0		0.3 × V_{DDI}[2]	V
DR	Data rate		0		40	Mbps
T_A	Ambient temperature		-40	27	125	°C
T_J	Junction temperature		-40		150	°C

NOTE:

1. V_{DDO} = output-side supply V_{DD}.
2. V_{DDI} = input-side supply V_{DD}.

7.4 Thermal Information

THERMAL METRIC		PACKAGE	UNIT
		SOIC16-WB (W)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.4	°C/W

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CA-IS3740C						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5V, C_L = 15pF, T_J = 150°C, Input a 20-MHz 50% duty cycle square wave			120	mW
P_{DA}	Maximum Power Dissipation on Side A				34	mW
P_{DB}	Maximum Power Dissipation on Side B				86	mW
CA-IS3741C						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5V, C_L = 15pF, T_J = 150°C, Input a 20-MHz 50% duty cycle square wave			120	mW
P_{DA}	Maximum Power Dissipation on Side A				45	mW
P_{DB}	Maximum Power Dissipation on Side B				75	mW
CA-IS3742C						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5V, C_L = 15pF, T_J = 150°C, Input a 20-MHz 50% duty cycle square wave			120	mW
P_{DA}	Maximum Power Dissipation on Side A				56	mW
P_{DB}	Maximum Power Dissipation on Side B				64	mW

7.6 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE W	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1s (100% production)	7070	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50-µs waveform per IEC 62368-1	8700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in air or oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	11312	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin(2πft), f = 1MHz	~ 0.5	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5000	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.7 Safety-Related Certifications

VDE	UL (Pending)
Certified according to DIN EN IEC60747-17(VDE 0884-17):2021-10; EN IEC60747-17:2020+AC:2021	Recognized under UL 1577 Component Recognition Program
Reinforced Isolation: V_{IORM}: 1414V_{PK} V_{IOTM}: 7070V_{PK} V_{IOSM}: 11312V_{PK}	Single protection SOIC16-WB: 5000V_{RMS}
Certification Number Reinforced Isolation Certificate: 40057278	Certification Number:

7.8 Electrical Characteristics

7.8.1 V_{DDA} = V_{DDB} = 5V ± 10%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4mA; See Figure 8-3	V_{DDO}[1] - 0.4	V_{DDO}[1] - 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4mA; See Figure 8-3		0.2	0.4	V
$V_{IT+(IN)}$	Logic input high level threshold		0.7 × V_{DDI}[1]			V
$V_{IT-(IN)}$	Logic input low level threshold				0.3 × V_{DDI}[1]	V
I_{IH}	High-Level input leakage current	V_{IH} = V_{DDI}[1] at VIx or ENx			20	µA
I_{IL}	Low-Level input leakage current	V_{IL} = 0V at VIx	–20			µA
Z_O	Output impedance[2]			50		Ω
CMTI	Common mode transient immunity	V_I = V_{DDI}[1] or 0V, V_{CM} = 1200V; See Figure 8-4	100	150		kV/µs
C_I	Input capacitance[3]	V_I = V_{DD}/2 + 0.4 × sin(2πft), f = 1MHz, V_{DD} = 5V		2		pF

NOTE:
1. V_{DDI} = input-side VDD supply voltage, V_{DDO} = output-side VDD supply voltage.
2. The nominal output impedance of each isolator driver is 50Ω ± 40%.
3. Measured from pin to Ground.

7.8.2 V_{DDA} = V_{DDB} = 3.3V ± 10%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2mA; See Figure 8-3	V_{DDO}[1] - 0.4	V_{DDO}[1] - 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2mA; See Figure 8-3		0.2	0.4	V
$V_{IT+(IN)}$	Logic input high level threshold		0.7 × V_{DDI}[1]			V
$V_{IT-(IN)}$	Logic input low level threshold				0.3 × V_{DDI}[1]	V
I_{IH}	High-Level input leakage current	V_{IH} = V_{DDI}[1] at VIx or ENx			20	µA
I_{IL}	Low-Level input leakage current	V_{IL} = 0V at VIx	–20			µA
Z_O	Output impedance[2]			50		Ω
CMTI	Common mode transient immunity	V_I = V_{DDI}[1] or 0V, V_{CM} = 1200V; See Figure 8-4	100	150		kV/µs
C_I	Input capacitance[3]	V_I = V_{DD}/2 + 0.4 × sin(2πft), f = 1MHz, V_{DD} = 3.3V		2		pF

NOTE:
1. V_{DDI} = input-side VDD supply voltage, V_{DDO} = output-side VDD supply voltage.
2. The nominal output impedance of each isolator driver is 50Ω ± 40%.
3. Measured from pin to Ground.

7.9 Supply Current

7.9.1 V_{DDA} = V_{DDB} = 5V ± 10%, T_A = -40 to 125°C

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3740C							
Supply Current – Outputs disabled	ENB = 0V; V_{IN} = 0V (CA-IS3740CL); V_{IN} = V_{DDA} (CA-IS3740CH)		I_{DDA}		1.9	3.2	mA
			I_{DDB}		4.7	7.4	
	ENB = 0V; V_{IN} = V_{DDA} (CA-IS3740CL); V_{IN} = 0V(CA-IS3740CH)		I_{DDA}		6.4	9.9	
			I_{DDB}		5.0	7.8	
Supply Current – DC Signal	ENB = V_{DDB}; V_{IN} = 0V (CA-IS3740CL); V_{IN} = V_{DDA} (CA-IS3740CH)		I_{DDA}		1.9	3.2	
			I_{DDB}		4.7	7.4	
	ENB = V_{DDB}; V_{IN} = V_{DDA} (CA-IS3740CL); V_{IN} = 0V(CA-IS3740CH)		I_{DDA}		6.4	9.9	
			I_{DDB}		5.0	7.8	
Supply Current – AC Signal	ENB = V_{DDB}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.2	6.6	
			I_{DDB}		5.0	7.9	
		10Mbps (5MHz)	I_{DDA}		5.0	7.9	
			I_{DDB}		6.8	10.5	
		40Mbps (20MHz)	I_{DDA}		5.4	8.5	
			I_{DDB}		12.8	19.3	
CA-IS3741C							
Supply Current – Outputs disabled	ENA = ENB = 0V; V_{IN} = 0V (CA-IS3741CL); V_{IN} = V_{DDI}[1] (CA-IS3741CH)		I_{DDA}		2.1	3.3	mA
			I_{DDB}		3.9	6.1	
	ENA = ENB = 0V; V_{IN} = V_{DDI} (CA-IS3741CL); V_{IN} = 0V(CA-IS3741CH)		I_{DDA}		6.3	9.8	
			I_{DDB}		5.5	8.6	
Supply Current – DC Signal	ENA = ENB = V_{DDI}; V_{IN} = 0V (CA-IS3741CL); V_{IN} = V_{DDI} (CA-IS3741CH)		I_{DDA}		2.1	3.3	
			I_{DDB}		3.8	6.0	
	ENA = ENB = V_{DDI}; V_{IN} = V_{DDI} (CA-IS3741CL); V_{IN} = 0V(CA-IS3741CH)		I_{DDA}		6.3	9.8	
			I_{DDB}		5.5	8.6	
Supply Current – AC Signal	ENA = ENB = V_{DDI}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.3	6.7	
			I_{DDB}		4.7	7.4	
		10Mbps (5MHz)	I_{DDA}		5.1	7.9	
			I_{DDB}		5.7	9.0	
		40Mbps (20MHz)	I_{DDA}		5.9	9.1	
			I_{DDB}		9.8	15.6	
CA-IS3742C							
Supply Current – Outputs disabled	ENA = ENB = 0V; V_{IN} = 0V (CA-IS3742CL); V_{IN} = V_{DDI}[1] (CA-IS3742CH)		I_{DDA}		3.0	4.8	mA
			I_{DDB}		3.0	4.8	
	ENA = ENB = 0V; V_{IN} = V_{DDI} (CA-IS3742CL); V_{IN} = 0V(CA-IS3742CH)		I_{DDA}		5.8	9.0	
			I_{DDB}		5.8	9.0	
Supply Current – DC Signal	ENA = ENB = V_{DDI}; V_{IN} = 0V (CA-IS3742CL); V_{IN} = V_{DDI} (CA-IS3742CH)		I_{DDA}		3.0	4.8	
			I_{DDB}		3.0	4.8	
	ENA = ENB = V_{DDI}; V_{IN} = V_{DDI} (CA-IS3742CL); V_{IN} = 0V(CA-IS3742CH)		I_{DDA}		5.8	9.0	
			I_{DDB}		5.8	9.0	
Supply Current – AC Signal	ENA = ENB = V_{DDI}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.3	6.7	
			I_{DDB}		4.7	7.3	
		10Mbps (5MHz)	I_{DDA}		5.6	8.7	
			I_{DDB}		6.0	9.3	
		40Mbps (20MHz)	I_{DDA}		8.7	13.4	
			I_{DDB}		9.4	14.4	

Note:
1. V_{DDI} = Input-side supply V_{DD}.

7.9.2 V_{DDA} = V_{DDB} = 3.3V ± 10%, T_A = -40 to 125°C

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3740C							
Supply Current – Outputs disabled	ENB = 0V; V_{IN} = 0V (CA-IS3740CL); V_{IN} = V_{DDA} (CA-IS3740CH)		I_{DDA}		1.7	2.9	mA
			I_{DDB}		4.5	7.0	
	ENB = 0V; V_{IN} = V_{DDA} (CA-IS3740CL); V_{IN} = 0V(CA-IS3740CH)		I_{DDA}		6.3	9.7	
			I_{DDB}		4.8	7.5	
Supply Current – DC Signal	ENB = V_{DDB}; V_{IN} = 0V (CA-IS3740CL); V_{IN} = V_{DDA} (CA-IS3740CH)		I_{DDA}		1.7	2.9	
			I_{DDB}		4.5	7.0	
	ENB = V_{DDB}; V_{IN} = V_{DDA} (CA-IS3740CL); V_{IN} = 0V(CA-IS3740CH)		I_{DDA}		6.3	9.7	
			I_{DDB}		4.8	7.5	
Supply Current – AC Signal	ENB = V_{DDB}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.0	6.3	
			I_{DDB}		4.8	7.5	
		10Mbps (5MHz)	I_{DDA}		4.9	7.6	
			I_{DDB}		5.9	9.1	
		40Mbps (20MHz)	I_{DDA}		5.6	8.8	
			I_{DDB}		9.5	14.7	
CA-IS3741C							
Supply Current – Outputs disabled	ENA = ENB = 0V; V_{IN} = 0V (CA-IS3741CL); V_{IN} = V_{DDI}[1] (CA-IS3741CH)		I_{DDA}		2.0	3.1	mA
			I_{DDB}		3.7	5.8	
	ENA = ENB = 0V; V_{IN} = V_{DDI} (CA-IS3741CL); V_{IN} = 0V(CA-IS3741CH)		I_{DDA}		6.2	9.6	
			I_{DDB}		5.4	8.5	
Supply Current – DC Signal	ENA = ENB = V_{DDI}; V_{IN} = 0V (CA-IS3741CL); V_{IN} = V_{DDI} (CA-IS3741CH)		I_{DDA}		2.0	3.1	
			I_{DDB}		3.7	5.8	
	ENA = ENB = V_{DDI}; V_{IN} = V_{DDI} (CA-IS3741CL); V_{IN} = 0V(CA-IS3741CH)		I_{DDA}		6.3	9.7	
			I_{DDB}		5.4	8.5	
Supply Current – AC Signal	ENA = ENB = V_{DDI}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.1	6.4	
			I_{DDB}		4.6	7.2	
		10Mbps (5MHz)	I_{DDA}		5.0	7.8	
			I_{DDB}		5.3	8.3	
		40Mbps (20MHz)	I_{DDA}		5.2	8.3	
			I_{DDB}		7.2	11.5	
CA-IS3742C							
Supply Current – Outputs disabled	ENA = ENB = 0V; V_{IN} = 0V (CA-IS3742CL); V_{IN} = V_{DDI}[1] (CA-IS3742CH)		I_{DDA}		2.9	4.7	mA
			I_{DDB}		2.9	4.7	
	ENA = ENB = 0V; V_{IN} = V_{DDI} (CA-IS3742CL); V_{IN} = 0V(CA-IS3742CH)		I_{DDA}		5.8	8.9	
			I_{DDB}		5.8	8.9	
Supply Current – DC Signal	ENA = ENB = V_{DDI}; V_{IN} = 0V (CA-IS3742CL); V_{IN} = V_{DDI} (CA-IS3742CH)		I_{DDA}		2.9	4.7	
			I_{DDB}		2.9	4.7	
	ENA = ENB = V_{DDI}; V_{IN} = V_{DDI} (CA-IS3742CL); V_{IN} = 0V(CA-IS3742CH)		I_{DDA}		5.8	8.9	
			I_{DDB}		5.8	8.9	
Supply Current – AC Signal	ENA = ENB = V_{DDI}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		4.2	6.6	
			I_{DDB}		4.3	6.8	
		10Mbps (5MHz)	I_{DDA}		5.1	8.0	
			I_{DDB}		5.2	8.1	
		40Mbps (20MHz)	I_{DDA}		6.0	9.4	
			I_{DDB}		6.4	10.0	

Note:
2. V_{DDI} = Input-side supply V_{DD}.

7.10 Timing Characteristics

7.10.1 V_{DDA} = V_{DDB} = 5V ± 10%, T_A = -40 to 125°C

Parameters			Test conditions	MIN	TYP	MAX	UNIT
DR	Data Rate			0		40	Mbps
PW_{min}	Minimum Pulse Width					20.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time		See Figure 8-1		22.0	35	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$				2.5	10	ns
$t_{sk(o)}$	Channel-to-Channel Output Skew Time[1]		Same-direction channels		1	3	ns
$t_{sk(pp)}$	Part-to-Part Output Skew Time [2]				1	7	ns
t_r	Output Signal Rise Time		See Figure 8-1		2.5	4.8	ns
t_f	Output Signal Fall Time		See Figure 8-1		2.5	4.8	ns
t_{PHZ}	Disable Propagation Delay, High to High Impedance Output		See Figure 8-2		8	12	ns
t_{PLZ}	Disable Propagation Delay, Low to High Impedance Output				8	12	ns
t_{PZH}	Enable Propagation Delay, High Impedance to High Output	CA-IS374xCL			10	15	ns
		CA-IS374xCH			15	22	ns
t_{PZL}	Enable Propagation Delay, High Impedance to Low Output	CA-IS374xCL			10	15	ns
		CA-IS374xCH			15	22	ns
t_{DO}	Default Output Delay Time from Input Power Loss		See Figure 8-3		10	15	ns
t_{SU}	Start-up Time				25	37	µs

Notes:

1. tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

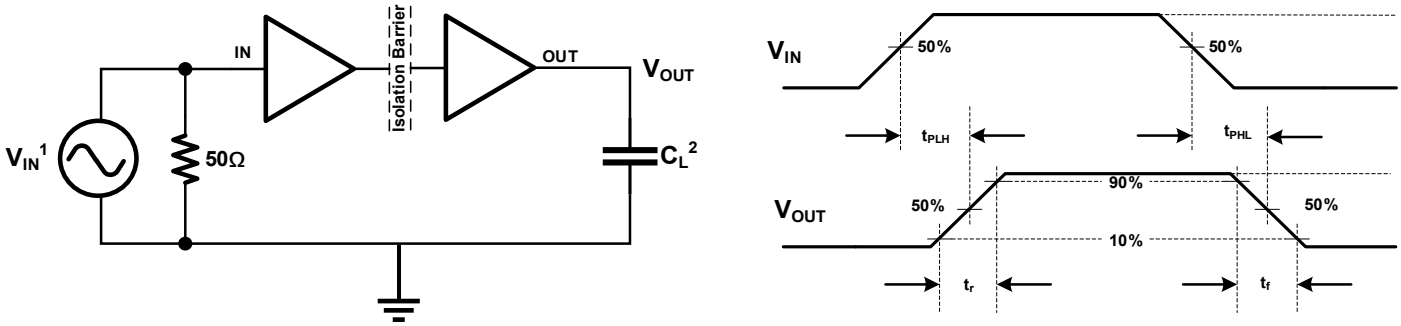
7.10.2 V_{DDA} = V_{DDB} = 3.3V ± 10%, T_A = -40 to 125°C

Parameters			Test conditions	MIN	TYP	MAX	UNIT
DR	Data Rate			0		40	Mbps
PW_{min}	Minimum Pulse Width					20.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time		See Figure 8-1		22.0	35	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$				2.5	10	ns
$t_{sk(o)}$	Channel-to-Channel Output Skew Time[1]		Same-direction channels		1	3	ns
$t_{sk(pp)}$	Part-to-Part Output Skew Time [2]				1	7	ns
t_r	Output Signal Rise Time		See Figure 8-1		2.5	4.8	ns
t_f	Output Signal Fall Time		See Figure 8-1		2.5	4.8	ns
t_{PHZ}	Disable Propagation Delay, High to High Impedance Output		See Figure 8-2		8	12	ns
t_{PLZ}	Disable Propagation Delay, Low to High Impedance Output				8	12	ns
t_{PZH}	Enable Propagation Delay, High Impedance to High Output	CA-IS374xCL			10	15	ns
		CA-IS374xCH			15	22	ns
t_{PZL}	Enable Propagation Delay, High Impedance to Low Output	CA-IS374xCL			10	15	ns
		CA-IS374xCH			15	22	ns
t_{DO}	Default Output Delay Time from Input Power Loss		See Figure 8-3		10	15	ns
t_{SU}	Start-up Time				25	37	µs

Notes:

3. tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
4. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

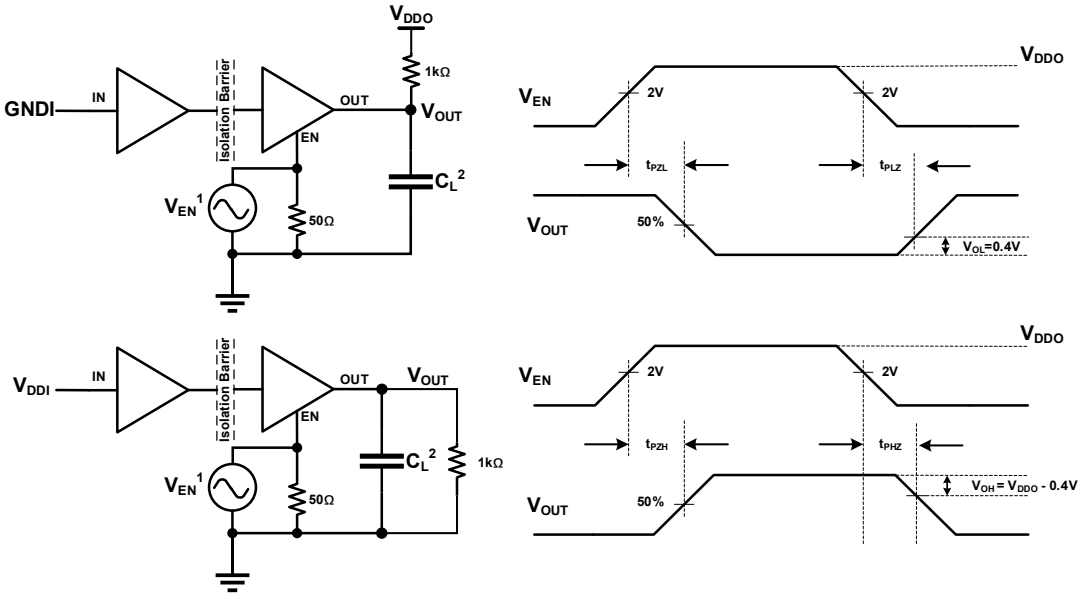
8 Parameter Measurement Information



Note:

1. A square wave generator provides V_{IN} input signal with characteristics: frequency ≤ 100kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_{out} = 50Ω. At the input, 50Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influences the output rising/falling time, it's a key factor in the timing characteristic measurement.

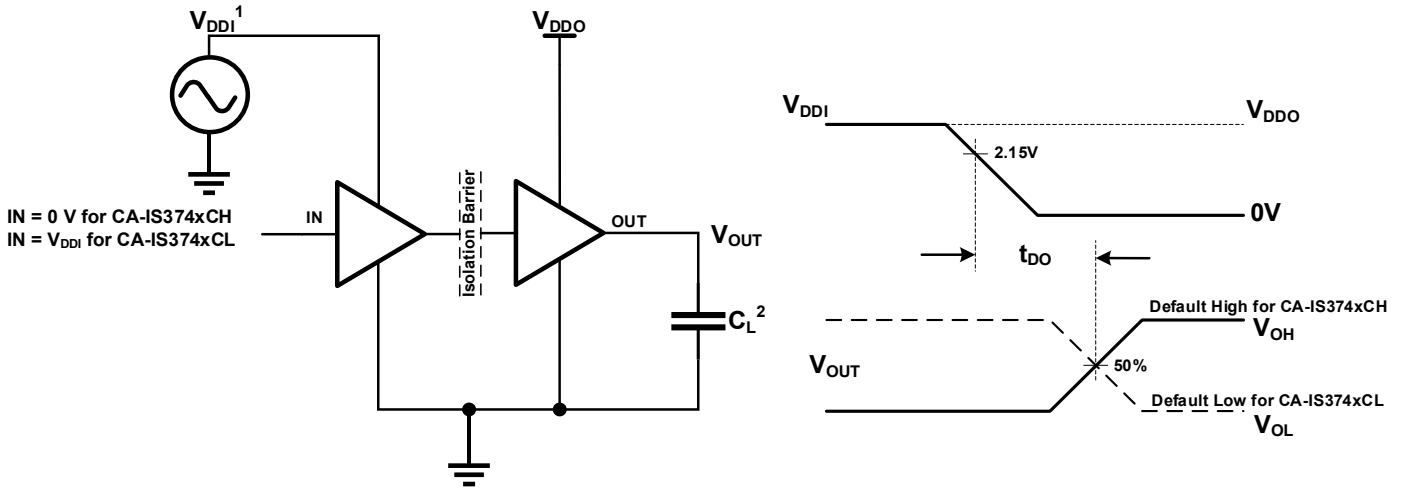
Figure 8-1 Switching Characteristics Test Circuit and Voltage Waveforms



Note:

1. A square wave generator provide V_{IN} input signal with characteristics: frequency ≤10kHz, 50% duty cycle, t_r≤3ns, t_f≤3ns, Z_{out} = 50Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

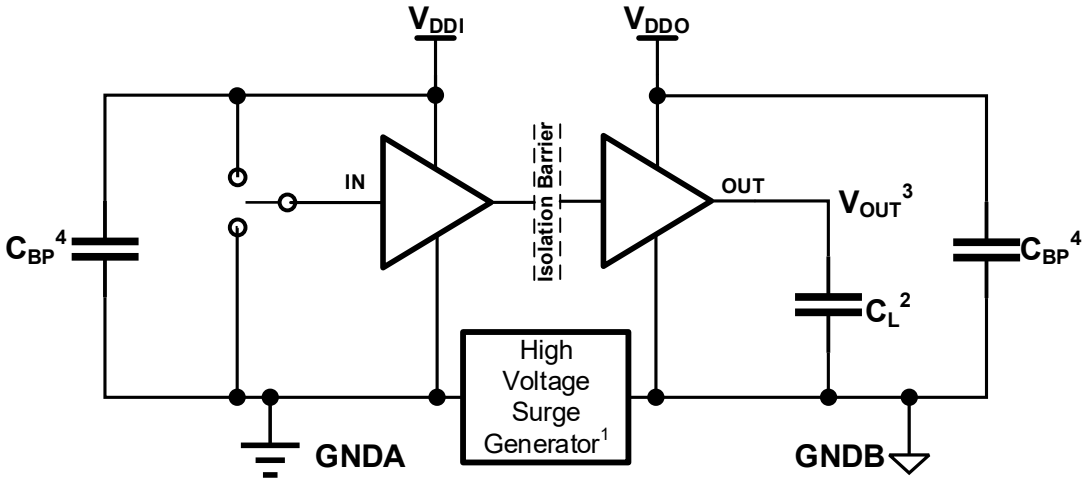
Figure 8-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform



Note:

1. Power supply ramp rate = 10mV/ns.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influences the output rising/falling time, it's a key factor in the timing characteristic measurement.

Figure 8-3. Default Output Delay Time Test Circuit and Voltage Waveforms



Note:

1. The High Voltage Surge Generator generates repetitive surges with > 1kV, < 10ns rise time and fall time to reach common-mode transient noise with > 100kV/μs slew rate.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: the output must remain stable whenever the high voltage surges occur.
4. C_{BP} is bypass capacitor, 0.1μF ~ 1μF.

Figure 8-4. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The CA-IS374xC devices are a family of 4-channel digital galvanic isolators using Chipanalog's full differential capacitive isolation technology. These devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO2 based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal and recovery input signal at output through a buffer stage. With this OOK architecture, the CA-IS374xC family of devices build a robust data transmission path between different power domains, without any special start-up initialization requirements.

These devices also incorporate advanced full differential techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 9-1, shows a functional block diagram of a typical channel; Figure 9-2 shows the operating waveform of a typical channel.

9.2 Functional Block Diagram

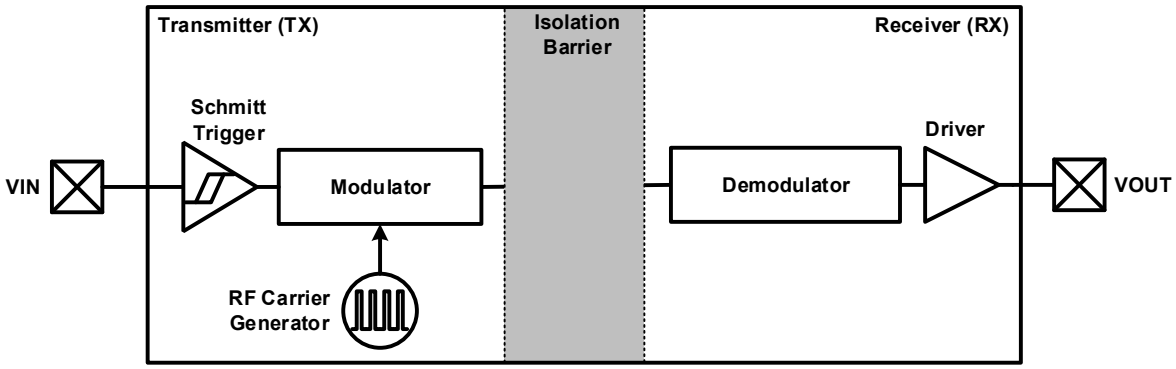


Figure 9-1 Functional Block Diagram of a Single Channel

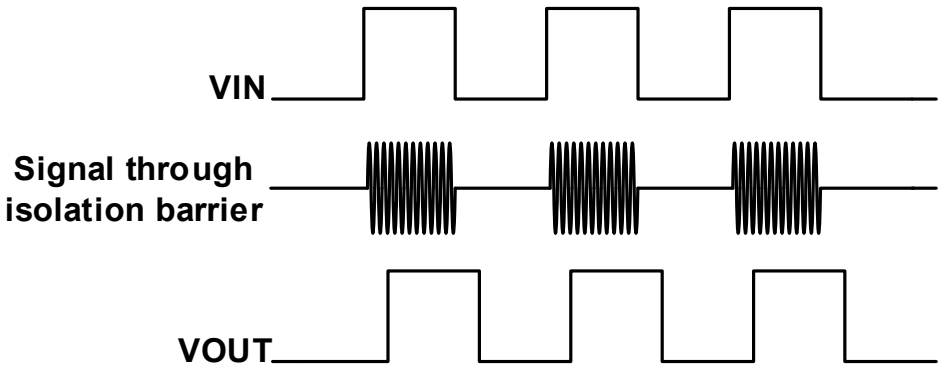


Figure 9-2 Conceptual Operation Waveform of a Single Channel

9.3 Device Operation Modes

Table 9-1 lists the operation modes for the CA-IS374xC devices.

Table 9-1 Operation Mode Table[1]

V_{DDI}[1]	V_{DDO}[1]	INPUT (VIx) [2]	OUTPUT (VOx)	OPERATION
PU	PU	H	H	Normal operation mode: A channel output follows the logic state of the input.
		L	L	
		Open	Default	Default output, fail-safe mode: If a channel input is open, the corresponding channel output goes to the default logic state (Low for CA-IS374xCL and High for CA-IS374xCH)
PD	PU	X	Default	Default output, fail-safe mode: When V_{DDI}[1] is unpowered, the corresponding channel output goes to the default logic state (Low for CA-IS374xCL and High for CA-IS374xCH)
X	PD	X	Undetermined	When V_{DDO}[2] is unpowered, the output states are undetermined.[3]

NOTE:

1. V_{DDI} = Input-side Supply V_{DD}; V_{DDO} = Output-side Supply V_{DD}; PU = Powered up ($V_{DD\_} \geq V_{DD(UVLO+)}$); PD = Powered down ($V_{DD\_} \leq V_{DD(UVLO-)}$); X = Irrelevant; H = High level; L = Low level.
2. A strongly driven input signal can weakly power the floating V_{DDI} through an internal protection diode and cause undetermined output.
3. The outputs are in undetermined state when $V_{DDI} > V_{DD(UVLO+)}$, $V_{DDO} < V_{DD(UVLO-)}$.

Table 9-2 is the truth table with Enable input for the CA-IS374x-Q1 devices.

Table 9-2. Enable Control

PART NUMBER	ENA[1,2]	ENB[1,2]	STATUS
CA-IS3740C	—	H	B-side outputs VO1, VO2, VO3, VO4 are enabled and each output follows the logic state of its input.
	—	L	B-side outputs VO1, VO2, VO3, VO4 are disabled, and go to high impedance state.
CA-IS3741C	H	X	A-side output VO4 is enabled and follows the logic state of its input.
	L	X	A-side output VO4 is disabled and goes to high impedance state.
	X	H	B-side outputs VO1, VO2, VO3 are enabled and each output follows the logic state of its input.
	X	L	B-side outputs VO1, VO2, VO3 are disabled and go to high impedance state.
CA-IS3742C	H	X	A-side output VO3, VO4 are enabled and follows the logic state of its input.
	L	X	A-side output VO3, VO4 are disabled and goes to high impedance state.
	X	H	B-side outputs VO1, VO2 are enabled and each output follows the logic state of its input.
	X	L	B-side outputs VO1, VO2 are disabled and go to high impedance state.

Notes:

1. Enable inputs ENA and ENB can be used to put the respective outputs in high impedance for multi master driving applications, external clock synchronization etc. With internal pull-up resistors, these pins can be connected to logic high or left floating to enable the outputs. If ENA, ENB are unused, it is recommended to connect these pins to a logic level, especially in the noisy environment.
2. X = Irrelevant; H = High level; L = Low level.

10 Application and Implementation

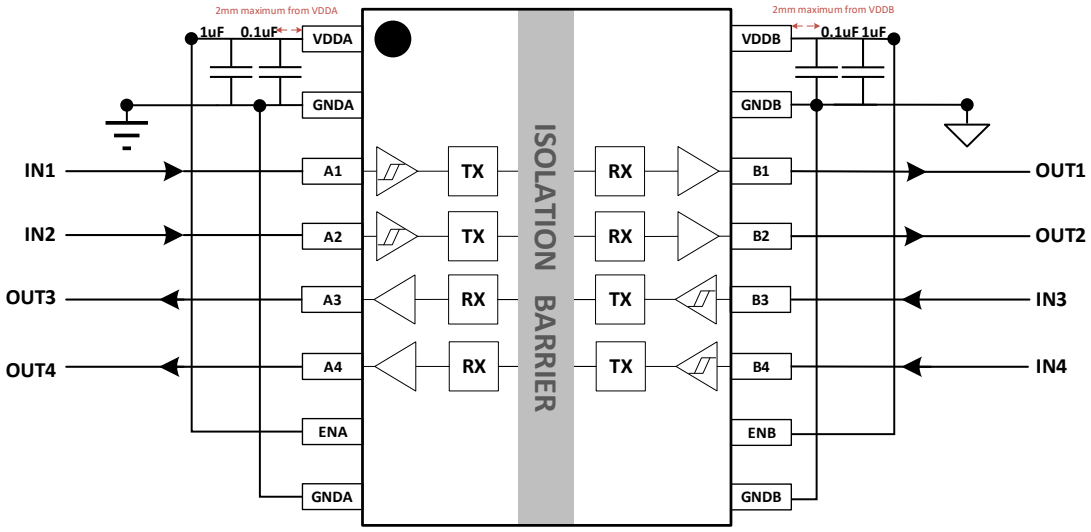


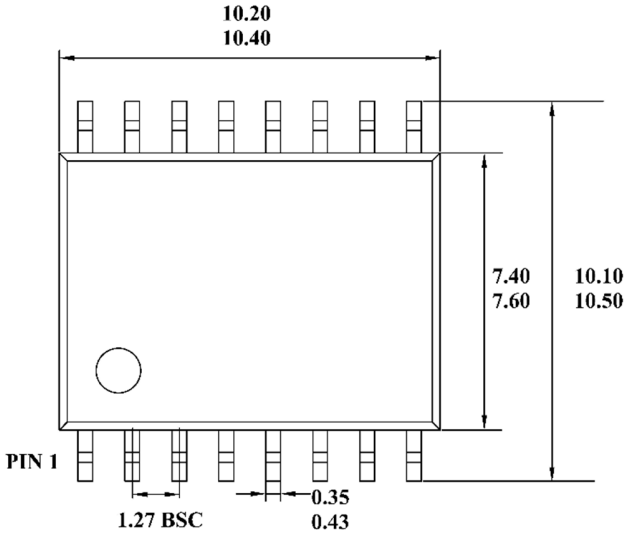
Figure 10-1 Typical Application Circuit of CA-IS3742Cx

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the CA-IS374xC devices only require several external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass VDDA and VDDB pins with 0.1µF to 1µF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible. Figure 10-1 shows typical operating circuit of the CA-IS374xC devices.

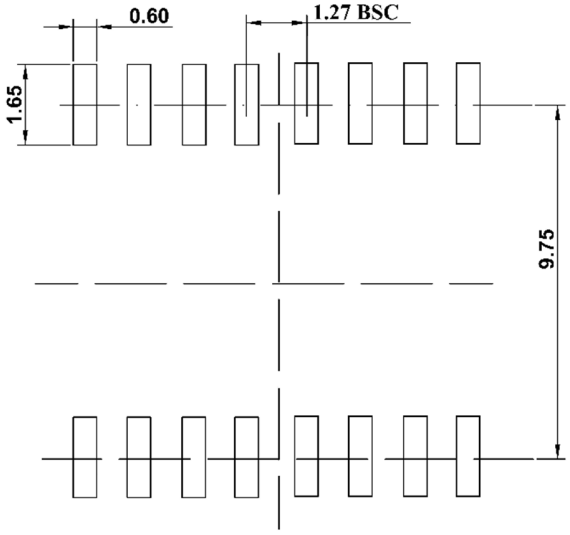
11 Package Information

11.1 SOIC16-WB Package

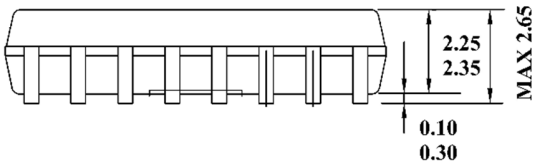
The values for the dimensions are shown in millimeters.



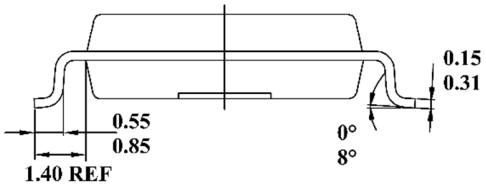
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT SIDE VIEW

12 Soldering Information

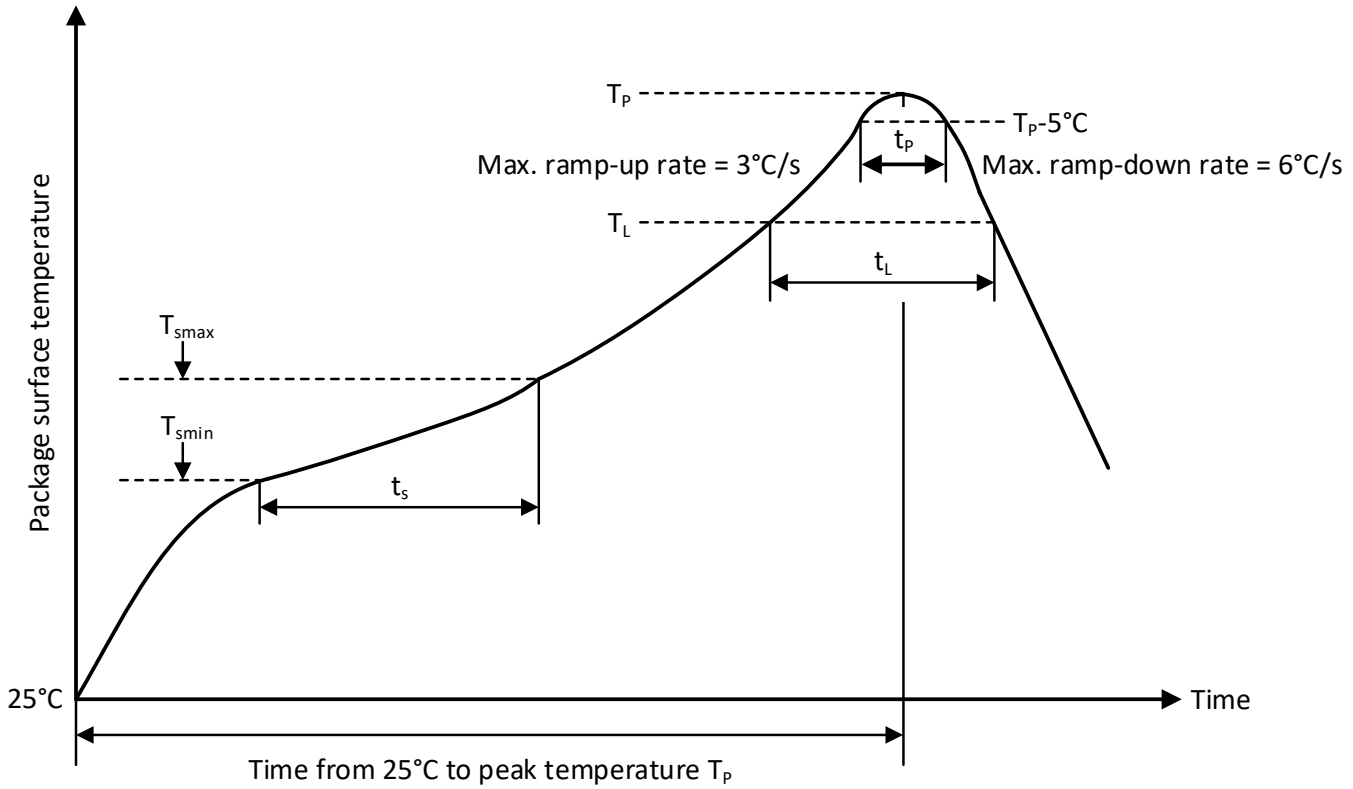


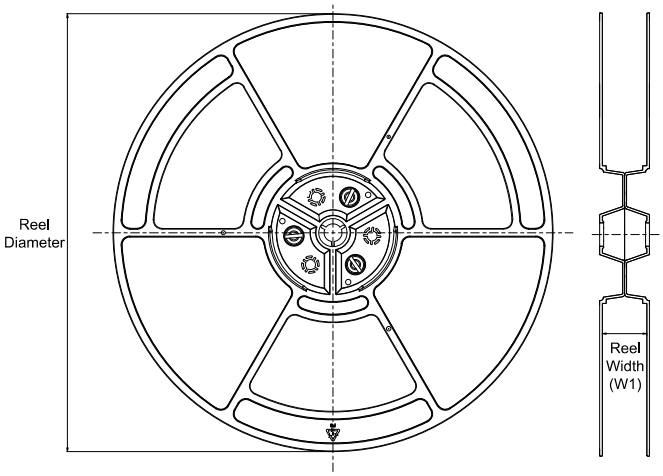
Figure 12-1 Soldering Temperature Curve

Table 12-1 Soldering Temperature Parameters

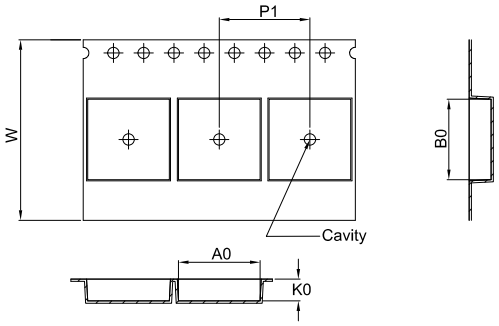
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

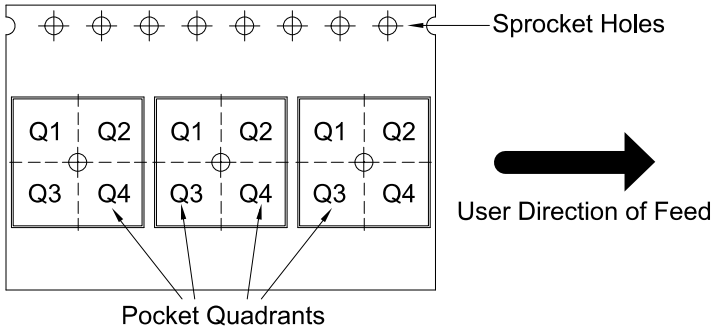


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3740CLW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
CA-IS3740CHW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
CA-IS3741CLW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
CA-IS3741CHW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
CA-IS3742CLW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
CA-IS3742CHW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1

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