CH7218A USB-C and DP 1.4 to HDMI 2.1 Protocol Converter

FEATURES

General

- VESA DisplayPort Specification version 1.4a
- HDMI transmitter supports HDMI specification version 2.1/2.0/1.4b
- HDCP 1.4 and HDCP 2.3 standards
- Supports HDCP repeater mode
- High Dynamic Range (HDR) dynamic / static metadata incorporated
- DTV profile uncompressed high speed digital interface CTA-861-G
- DSC Standard v1.2a decoding and DSC bypass capable
- Video color space including RGB at 6/8/10/12 bpc, YCbCr4:4:4 and YCbCr4:2:2 /4:2:0 at 8/10/12 bpc
- RGB to YCC 4:4:4/4:2:2/4:2:0 and YCC 4:4:4/4:2:2 to YCC 4:2:0 color space conversions implemented
- Digital audio supports up to 8 channel LPCM(16/20/24 bit) with sample rate up to 192kHz, compressed audio formats (AC3,DTS,DTS-HD MA, and Dolby MAT), HBR audio formats with frame rate up to 1536kHz, and 3D audio format with sample rate up to 192kHz
- USB Type-C DisplayPort Alt-Mode to HDMI 2.1/2.0/1.4a protocol converter ready
- Integrated Ra, Rd and Rp resistors for DFP/UFP to identify connection
- Seamless switch between Type-C SBU and DisplayPort AUX Channel
- USB Power Delivery 3.0 on CC communication
- Built-in USB Billboard Class 1.2.2 and USB 2.0 PHY to support DisplayPort Alt-mode
- Embedded Microcontroller, ROM and EDID Buffer
- Firmware update through Chrontel proprietary technologies
- Configurable Power Saving mode and low stand-by current
- RoHS compliant and Halogen free package
- Offered in 68 pin QFN package

Upstream (USB-C / DP)

- USB Type-C port compliant with USB Type-C Cable and Connector Specification revision 2.0
- USB PD 3.0 compliant
- Compliant with DisplayPort Alternate Mode on USB Type C standard
- Compliant with VESA DisplayPort Specification version 1.4 and and Embedded DisplayPort (eDP) Specification version 1.4
- Support up to 4 Main Link Lanes at 1.62Gbps,2.7Gbps (HBR), 5.4Gbps (HBR2) and 8.1Gbps (HBR3) link rate
- Automotive DP input signal detection and Lane swap

GENERAL DESCRIPTION

Chrontel's CH7218A is a low-cost, low-power semiconductor device that translates the DisplayPort signal to HDMI 2.1 through the USB Type-C connector. This innovative USB Type-C based DisplayPort receiver with a high performance DSC decoder, an integrated HDMI 2.1 Transmitter is specially designed to target the USB Type-C to HDMI 2.1 converter, adopter and docking device. Through the CH7218A's advanced decoding / encoding algorithm, the input DisplayPort high-speed serialized multimedia data can be seamlessly converted to HDMI/DVI output.

The CH7218A's DP receiver is compliant with the DisplayPort Specification 1.4 and Embedded DisplayPort (eDP) Specification version 1.4. With sophisticated DisplayPort signal detection and the Lane Swap/AUX polarity inversion logic, the CH7218A supports USB Type-C cable plug orientation switch. With internal HDCP key Integrated, the device supports HDCP 1.4 and 2.3 specifications. In the device's receiver block, which supports four DisplayPort Main Link Lanes input with data rate running at 1.62Gbps, 2.7Gbps, 5.4Gbps or 8.1Gbps, and converted the input signal to HDMI output up to 8Kx4k@60Hz or 4K2K@120Hz in Fixed Rate Link mode. Leveraging the USB Power Delivery control logic, the USB billboard module for USB device indentify and DisplayPort's Link Training routine, the CH7218A is capable of instantly bring up the video display to the HDMI 2.1 TV/Monitor when the initialization process is completed.

The CH7218A also supports up to 8-channel audio input from DP Rx and output from HDMI Tx with sample rate up to 192 KHz. Available audio bandwidth depends on the pixel clock frequency, the video format timing, and whether or not content protection re-synchronization is needed.

With sophisticated MCU and the On Chip Flash, CH7218A support auto-boot and EDID buffer. Leveraging the firmware auto-loaded from the embedded ROM, CH7218A can support DP input detection, HDMI connection detection, and determine to enter into Power saving mode automatically.

supported for compliance with the USB type C cable plug orientation switch
- RGB at 6/8/10/12 bpc, YCbCr4:4:4 and YCbCr4:2:2 /4:2:0 at 8/10/12 bpc input formats supported
- Fast and full Link Training for embedded DisplayPort system
- Support eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
- Support Spread Spectrum Clocking (de-spreading) for EMI reduction
- Forward Error Correction supported
- Adaptive-Sync supported
- Programmable/Adaptive equalizer to compensate for Cable, PCB and/or connector losses
- 1/2/4/8 Slices DSC decoding supported.

Downstream (HDMI)

- HDMI transmitter compliant with HDMI specification version 2.1
- supports 4 Main Link Lane up to 12 Gbps Fixed Rate Link (FRL) data rate for video timing up to 8Kx4K@60Hz or 4K2K@120Hz
- Supports up to HDMI 6Gbps TMDS data rate or 600 MHz TMDS clock for video transport
- RGB at 6/8/10/12 bpc, YCbCr 4:4:4 / 4:2:2 / 4:2:0 at 8/10/12 bpc output formats supported
- Progressive 3D video formats supported
- Variable Refresh Rate supported
- DSC pass-through supported
- SCDC supported on HDMI DDC
- FRL link training supported
- CEC tunneling over AUX supported
- Automatic Low Latency Mode supported
- Graphic test pattern generator integrated

APPLICATION

- Onboard DP to HDMI 2.1 conversion
- USB Type C to HDMI cable/Adapter/Docking Station
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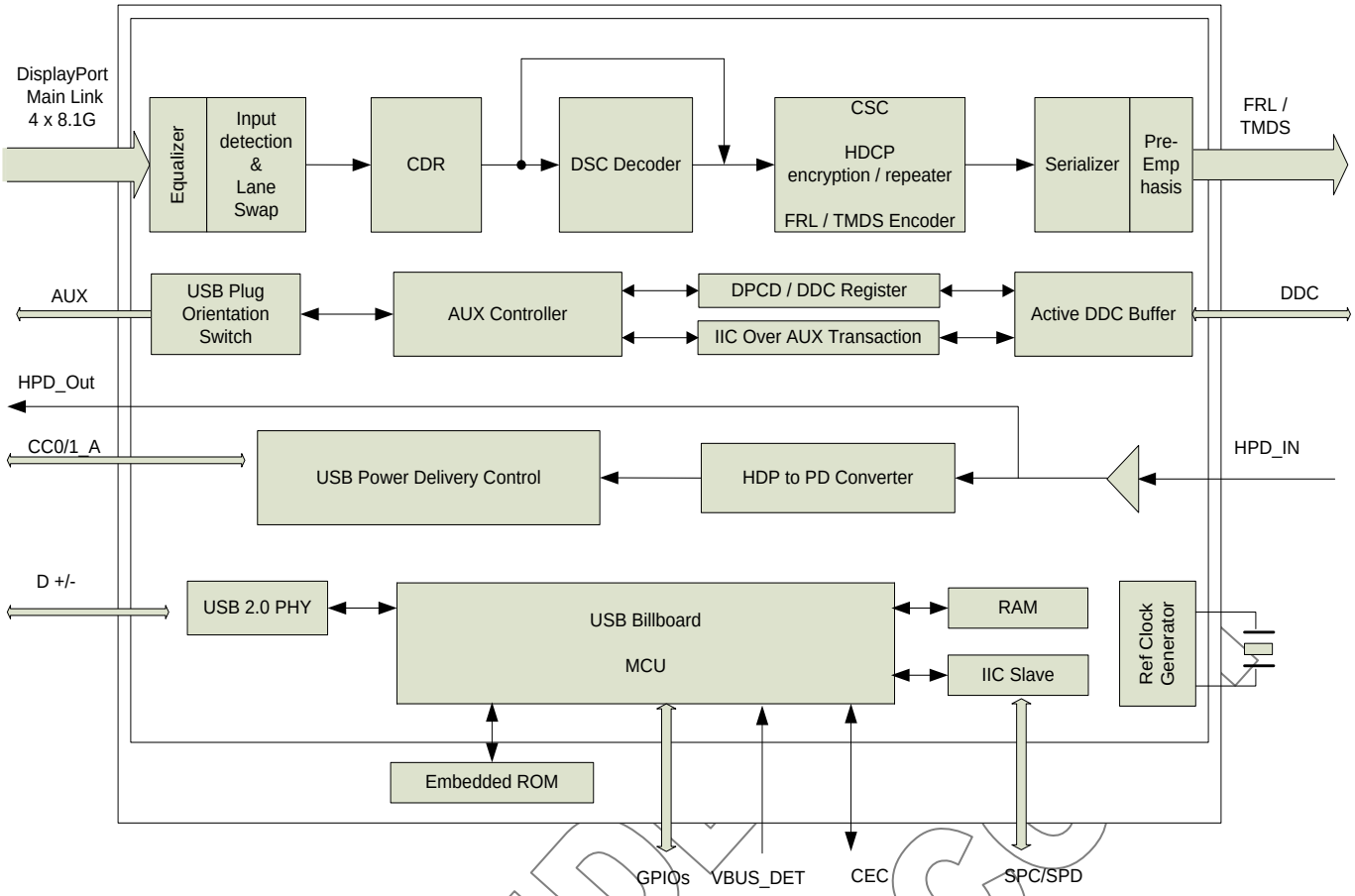

Figure 1: CH7218A Functional Block Diagram

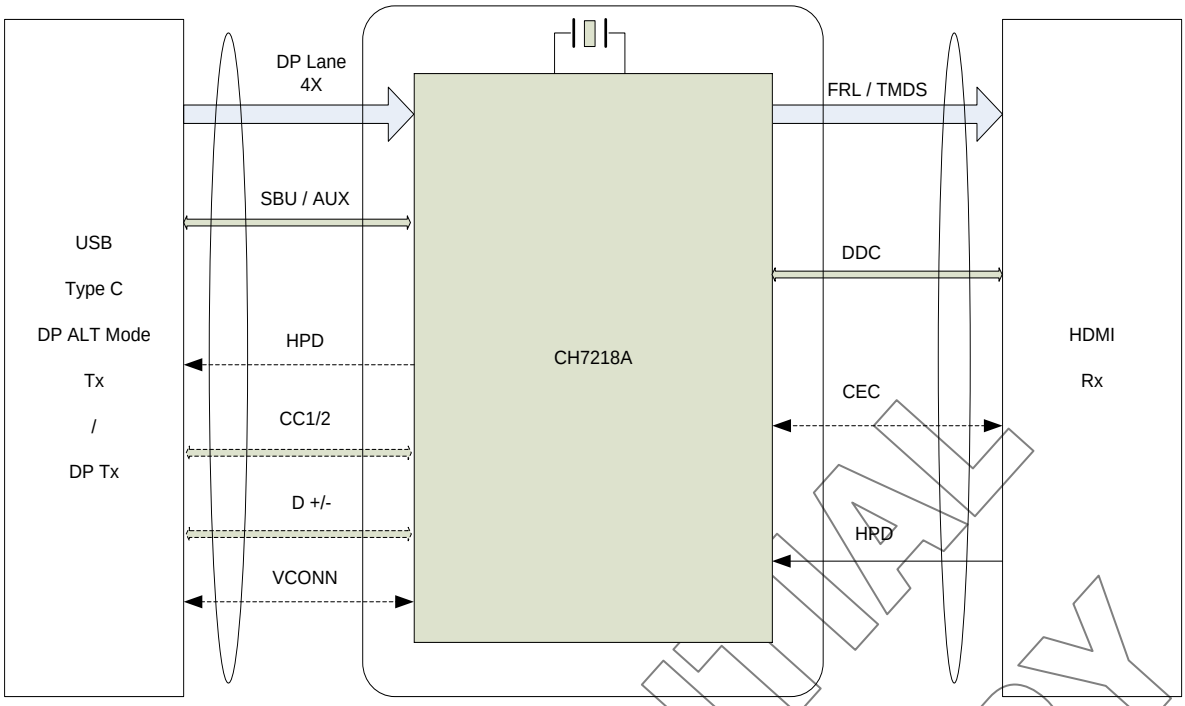

Figure 2: CH7218A Application Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

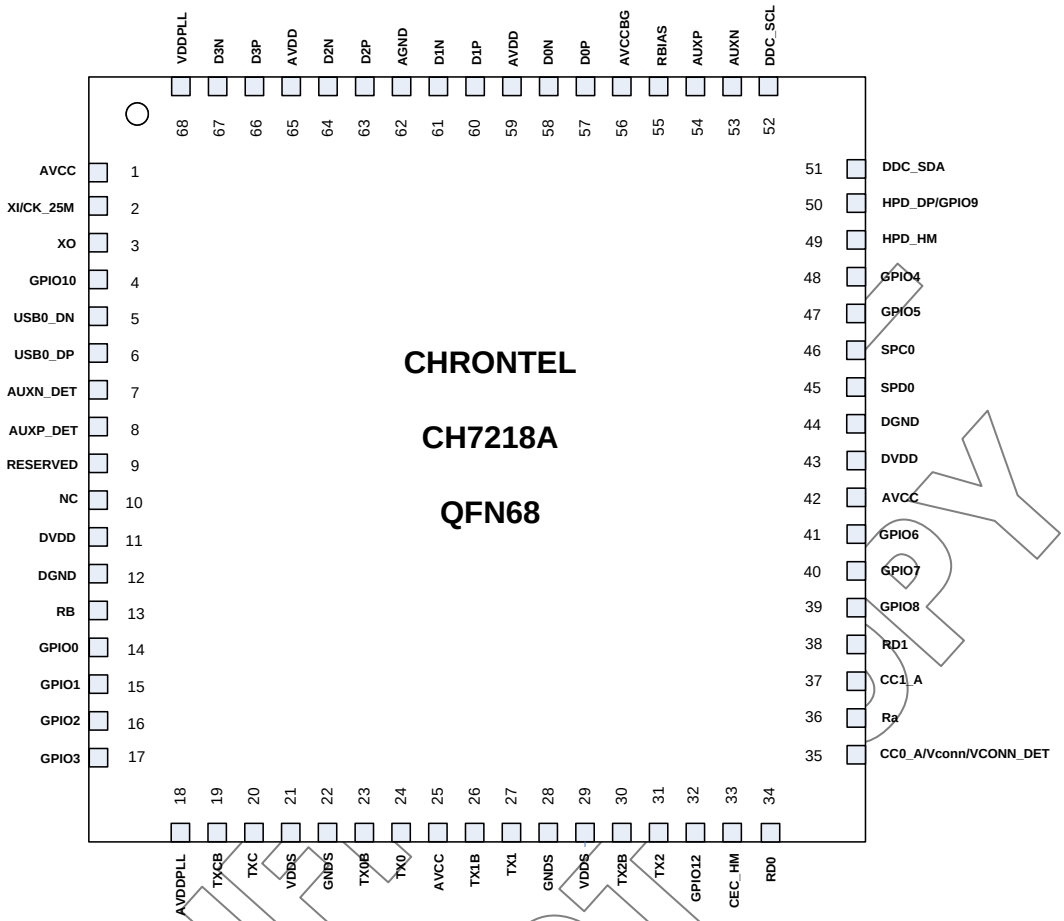

Figure 3: CH7218A 68-Pin QFN Pin Out

1.2 Pin Description

Table 1: 68 QFN Pin Name Descriptions

Pin #	Type	Symbol	Description
2	In	XI/CK_25M	**Crystal Input / External Reference Input** A parallel resonance crystal should be attached between this pin and XO. An external 3.3V CMOS compatible clock also can drive the XI Input
3	Out	XO	**Crystal Output** A parallel resonance crystal should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open
4	In/Out	GPIO10	**General Purpose Input/Output Interface**
5,6	In/Out	USB0_DN/ USB0_DP	**D+/- Input of USB Type C Interface**
7,8	In/Out	AUXN/P_DET	**AUX Channel Connection Detection Pins**
9		RESERVED	**Reserved Pin**
10	NC	NC	**Not Connected**
13	In	RB	**Reset* Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
14~17	In/Out	GPIO[3:0]	**General Purpose Input/Output Interface**
19,20	Out	TXCB/ TXC	**HDMI Clock Outputs** These pins provide the differential clock output for the HDMI
23,24	Out	TX0B/ TX0	**HDMI Data Channel 0 Outputs** These pins provide the TMDS differential outputs for data channel 0
26,27	Out	TX1B/ TX1	**HDMI Data Channel 1 Outputs** These pins provide the TMDS differential outputs for data channel 1
30,31	Out	TX2B/ TX2	**HDMI Data Channel 2 Outputs** These pins provide the TMDS differential outputs for data channel 2
32	In/Out	GPIO12	**General Purpose Input/Output Interface**
33	In/Out	CEC_HM	**CEC pin of HDMI output**
34	In	Rd0	**USB Type-C Dead Battery Rd Resistor** Connect CC0_A to this pin to enable dead battery Rd on CC0_A pin
35	In/Out	CC0_A	**USB Type-C Configure Channel 0 of Port A**
	In	VCONN	**VCONN Input** Connect this pin to VCONN pin of USB Type-C Plug Connector if CH7218A is used in VCONN Power Accessory mode.
	In	VCONN_DET	**USB VCONN Voltage Detection** Voltage input 2.7 ~ 5.5v
36	In	Ra	**Ra Resistor** When used in typeC accessory mode, this pin needs connect to CC0.
37	In/Out	CC1_A	**USB Type-C Configure Channel 1 of Port A**
38	In	Rd1	**USB Type-C Dead Battery Rd Resistor** Connect CC1_A to this pin to enable dead battery Rd on CC1_A pin
39	In/Out	GPIO8	**General Purpose Input/Output Interface**
40	In/Out	GPIO7	**General Purpose Input/Output Interface**
41	In/Out	GPIO6	**General Purpose Input/Output Interface**
45	In/Out	SPD0	**Serial Port Data Input / Output**

			This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required
46	In	SPC0	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required
47	In/Out	GPIO5	**General Purpose Input/Output**
48	In/Out	GPIO4	**General Purpose Input/Output**
49	In	HPD_HM	**HDMI Tx HPD Input**
50	Out	HPD_DP	**DP Rx HPD Output**
	In/Out	GPIO9	**General Purpose Input/Output**
51	In	DDC_SDA	**Serial Port Data to HDMI Receiver** The pin should be connected to data signal of HDMI DDC. This pin requires a pull-up 1.8 kΩ resistor to the desired voltage level
52	Out	DDC_SCL	**Serial Port Clock Output to HDMI Receiver** The pin should be connected to clock signal of HDMI DDC. This pin requires a pull-up 1.8kΩ resistor to the desired voltage level
53,54	In/Out	AUXN/AUXP	**AUX Channel Differential Input/Output** These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
55	In	RBIAS	**External Reference Current Set** This pin sets the external reference current. A 1 kΩ with 1% tolerance resistor should be connected between this pin and ground using short and wide traces
57,58	In	D0P/ D0N	**DP Main Link Differential Lane 0 Input** These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
60,61	In	D1P/ D1N	**DP Main Link Differential Lane 1 Input** These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
63,64	In	D2P/ D2N	**DP Main Link Differential Lane 2 Input** These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
66,67	In	D3P/ D3N	**DP Main Link Differential Lane 3 Input** These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
68	Power	VDDPLL	**PLL Power Supply (1.2V)**
1,25,42,56	Power	AVCC	**Analog Power Supply(3.3V)**
11,43	Power	DVDD	**Digital Core/IO Power Supply (1.2V)**
12,44	Power	DGND	**Digital Ground**
18	Power	AVDDPLL	**PLL Power Supply (1.2V)**
21,29	Power	VDDS	**Serializer Power Supply (1.2V)**
22,28	Power	GNDS	**Ground**
59,65	Power	AVDD	**Analog Power Supply (1.2V)**
62	Power	AGND	**Analog Ground**

2.0 PACKAGE DIMENSION

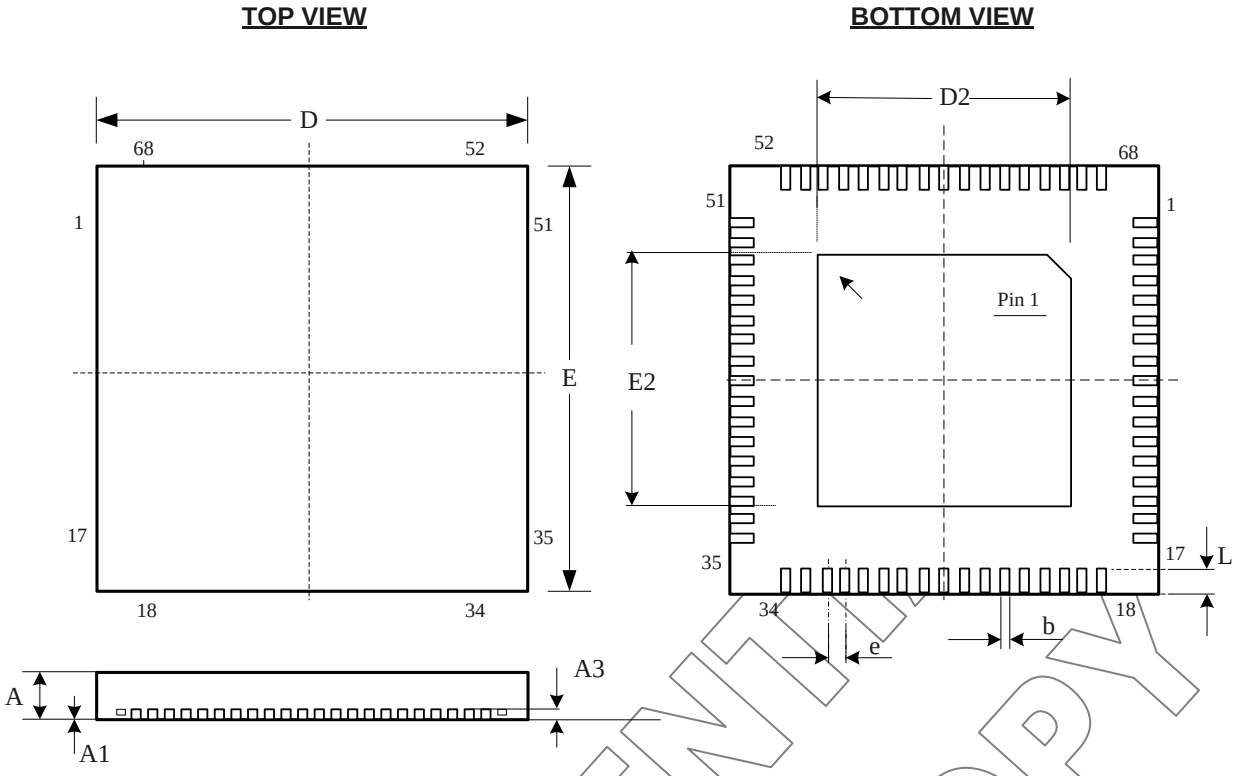

Figure 4: 68 Pin QFN Package (8x8 mm)

Table of Dimensions

No. of Leads		SYMBOL									
68 (8x8 mm)		D	E	D2	E2	e	b	L	A	A1	A3
Milli-meters	MIN	7.90	7.90	6.10	6.10	0.30	0.15	0.35	0.80	0.00	0.20REF
	MAX	8.10	8.10	6.30	6.30	0.50	0.25	0.45	0.90	0.05	

Notes:

1. All dimensions conform to JEDEC standard MO-207.

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ORDERING INFORMATION

Part Number	Package Type	Content Protection	Operating Temperature Range	Minimum Order Quantity
CH7218A-BF	68 QFN, Lead-free	None	Commercial : 0 to 70°C	**260/Tray**
CH7218A-BFK	68 QFN, Lead-free	HDCP 1.4 / 2.3	Commercial : 0 to 70°C	**260/Tray**

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