CH7217A USB Type-C DP Alt Mode to HDMI 2.0 Converter with PD 3.0 Controller

FEATURES

- Compliant with DisplayPort Alternate Mode on USB Type C standard
- Compliant with DisplayPort Specification version 1.4 and Embedded DisplayPort (eDP) Specification version 1.4
- Support up to 4 Main Link Lanes at 1.62Gbps,2.7Gbps (HBR), 5.4Gbps (HBR2), or 8.1Gbps (HBR3) link rate
- Automotive DP input signal detection and Lane swap supported for compliance with the USB type C cable plug orientation switch
- AUX CH polarity inversion supported for USB type C cable plug orientation switch
- Adaptive DisplayPort receiver equalization supported for the compensation of input signal attenuation
- Support Fast and full Link Training
- Support eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
- HDMI transmitter compliant with HDMI specification version 2.0 and DVI specification version 1.0
- HDMI transmitter supports up to 6.0Gbps data rate for video timing of 4Kx2K@60Hz
- SCDC supported on HDMI DDC
- CEC tunneling over AUX is supported
- High-Dynamic-Range (HDR) Static Metadata: HDR10 (SMPTE ST2084), Hybrid Log-Gamma (HLG), Dolby Vision (SMPTE ST2084) are supported
- RGB/YCC444/422 to YCC444/422/420 conversions are supported, deep color depth up to 16 bit
- Progressive 3D video formats supported
- HDCP engine compliant with HDCP 2.2 and HDCP 1.4 specification with internal HDCP Keys
- HDCP 1.4/2.2 repeater supported
- 2 USB Type-C ports integrated compliant with USB Type-C Cable and Connector Specification revision 2.0
- Compliant with USB Power Delivery Specification Revision 3.0, with USB Power Delivery BMC transceiver integrated on USB Type-C ports
- Charge Through function support
- Fast Role Swap support
- SPDIF/IIS input supported with audio sampling rate up to 192KHz
- On-chip Audio Decoder which support 8 channel Audio input from DP Rx and output from HDMI Tx, support LPCM(16/20/24 bit) format with sampling rate up to 192kHz, compressed audio formats (AC3, DTS, DTS-HD MA, and Dolby MAT) and HBR audio formats with frame rate up to 1536kHz
- Integrated Ra, Rd and Rp for USB Type-C
- Embedded MCU to handle the control logic
- Full speed USB billboard module supported with USB 2.0 PHY integrated

GENERAL DESCRIPTION

Chrontel's CH7217A is a low-cost, low-power semiconductor device that translates the DisplayPort signal to HDMI/DVI through the USB Type-C connector. This innovative USB Type-C based DisplayPort receiver with an integrated HDMI Transmitter is specially designed to target the USB Type-C to HDMI converter, adapter and dongle device. Through the CH7217A's advanced decoding / encoding algorithm, the input DisplayPort high-speed serialized multimedia data can be seamlessly converted to HDMI/DVI output.

The CH7217A's DP/eDP receiver is compliant with the DisplayPort Specification 1.4 and Embedded DisplayPort (eDP) Specification version 1.4. With sophisticated DisplayPort signal detection and the Lane Swap/AUX polarity inversion logic, the CH7217A supports USB Type-C cable plug orientation switch. With internal HDCP key Integrated, the device support HDCP 2.2 specifications. In the device's receiver block, which supports four DisplayPort Main Link Lanes input with data rate running at 1.62Gbps, 2.7Gbps, 5.4Gbps or 8.1Gpbs, and converted the input signal to HDMI output up to 4Kx2k@60Hz. Leveraging the USB Power Delivery control logic, the USB billboard module for USB device indentify and DisplayPort's unique source/sink "Link Training" routine, the CH7217A is capable of instantly bring up the video display to the HDMI/DVI TV/Monitor when the initialization process is completed.

The CH7217A also supports up to 8-channel audio input from either DP Rx or SPDIF/IIS port and output from HDMI Tx with sample rate up to 192 KHz. Available audio bandwidth depends on the pixel clock frequency, the video format timing, and whether or not content protection re-synchronization is needed.

With sophisticated MCU and the embedded ROM, CH7217A supports auto-boot and EDID buffer. Leveraging the firmware auto-loaded from the embedded ROM, CH7217A supports DP input detection, HDMI connection detection, and determine to enter into Power saving mode automatically.

- Embedded ROM, integrated EDID Buffer
- IIC Slave, USB 2.0 are available for firmware update
- IIC slave interface are available for debug
- Low power architecture, support Auto Power Saving mode and low stand-by current
- Low power architecture
- RoHS compliant and Halogen free package
- Offered in 68 pin QFN package

APPLICATION

- USB Type C to HDMI 2.0 Adapter/Docking Stations
- USB Type-C Monitor/Projector/TV Display
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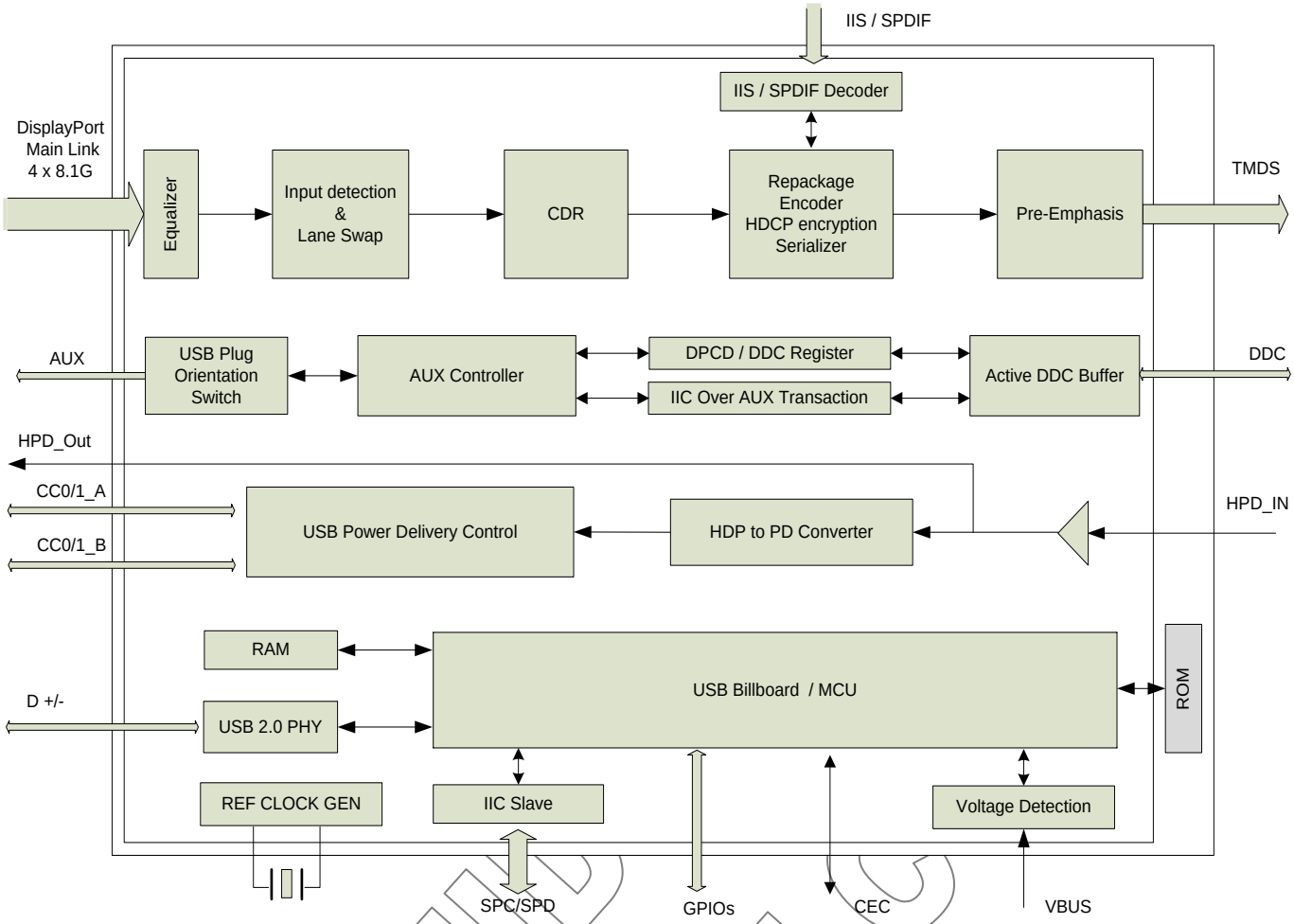

Figure 1: CH7217A Functional Block Diagram

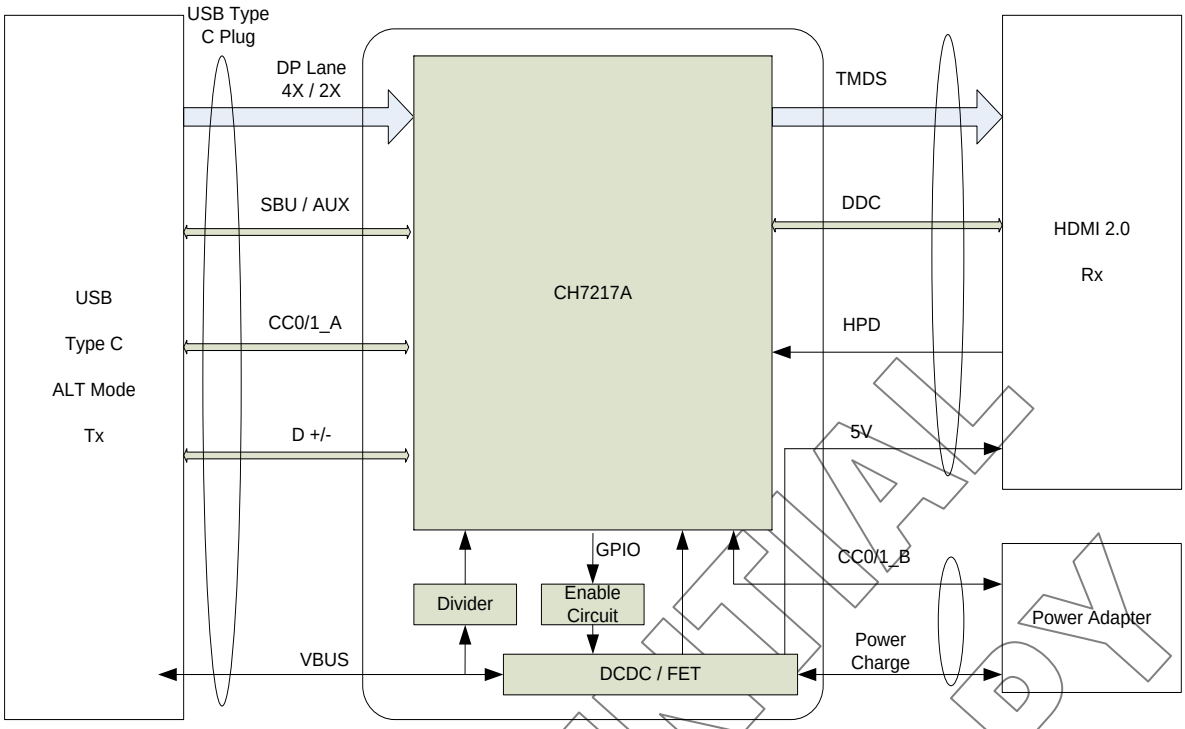

Figure 2: CH7217A USB Type-C to HDMI 2.0 + Power Charge Docking Application Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

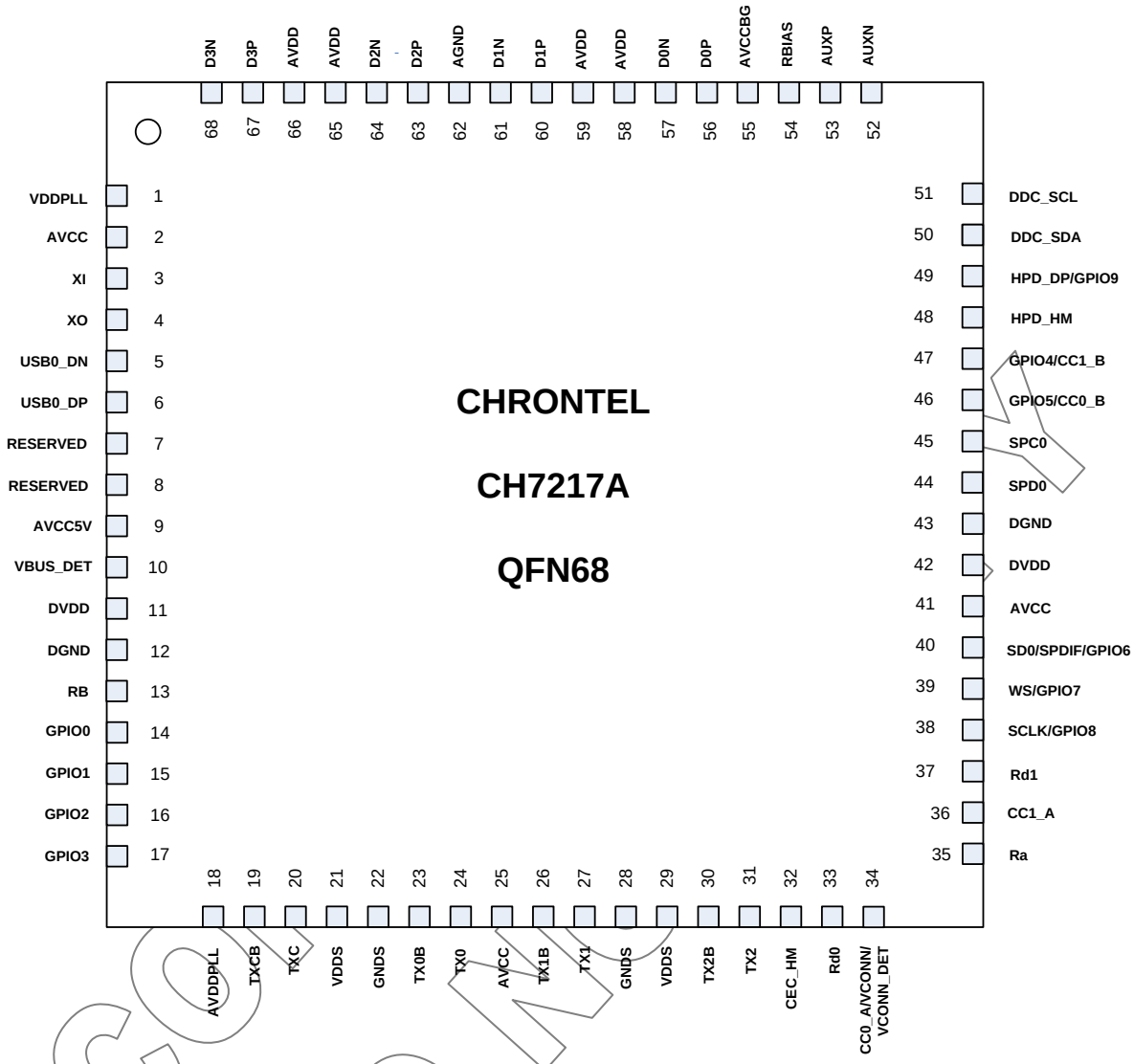

Figure 3: CH7217A 68-Pin QFN Pin Out

1.2 Pin Description

Table 1: 68 QFN Pin Name Descriptions

Pin #	Type	Symbol	Description
3	In	XI	**Crystal Input / External Reference Input** A parallel resonance crystal should be attached between this pin and XO. An external 3.3V CMOS compatible clock also can drive the XI Input
4	Out	XO	**Crystal Output** A parallel resonance crystal should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open
5,6	In/Out	USB_DN/ USB_DP	**D+/- Input of USB Type C Interface**
7,8		RESERVED	**RESERVED Pins**
10	In	VBUS_DET	**USB VBUS Voltage Detection** Voltage input 0 ~ 5V
13	In	RB	**Reset* Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
14~17	In/Out	GPIO[3:0]	**General Purpose Input/Output Interface**
19,20	Out	TXCB/ TXC	**HDMI Clock Outputs** These pins provide the differential clock output for the HDMI
24,25	Out	TX0B/ TX0	**HDMI Data Channel 0 Outputs** These pins provide the TMDS differential outputs for data channel 0
26,27	Out	TX1B/ TX1	**HDMI Data Channel 1 Outputs** These pins provide the TMDS differential outputs for data channel 1
30,31	Out	TX2B/ TX2	**HDMI Data Channel 2 Outputs** These pins provide the TMDS differential outputs for data channel 2
33	In	Rd0	**USB Type-C Dead Battery Rd Resistor** Connect CC0_A to this pin to enable dead battery Rd on CC0_A pin
34	In/Out	CC0_A	**USB Type-C Configure Channel 0**
	In	VCONN	**VCONN Input** Connect this pin to VCONN pin of USB Type-C Plug Connector if CH7217A is used in VCONN Power Accessory mode.
	In	VCONN_DET	**USB VCONN Voltage Detection** Voltage input 2.7 ~ 5.5v
35	In	Ra	**Ra Resistor** When used in typeC accessory mode, this pin needs connect to CC0.
36	In/Out	CC1_A	**USB Type-C Configure Channel 1**
37	In	Rd1	**USB Type-C Dead Battery Rd Resistor** Connect CC1_A to this pin to enable dead battery Rd on CC1_A pin
38	In/Out	GPIO8	**General Purpose Input/Output Interface**
	In	SCLK	**I2S Clock Signal**
39	In/Out	GPIO7	**General Purpose Input/Output Interface**
	In	WS	**I2S Channel Select Signal**
40	In/Out	GPIO6	**General Purpose Input/Output Interface**
	In	SD0	**I2S Data Input**
		SPDIF	**SPDIF Audio Signal Input**
44	In/Out	SPD0	**Serial Port Data Input / Output**

			This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required
45	In	SPC0	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required
46	In/Out	GPIO5	**General Purpose Input/Output**
	In/Out	CC0_B	**USB Type-C Configure Channel 2**
47	In/Out	GPIO4	**General Purpose Input/Output**
	In/Out	CC1_B	**USB Type-C Configure Channel 2**
48	In	HPD_HM	**HDMI Tx HPD Input**
49	Out	HPD_DP	**DP Rx HPD Output**
	In/Out	GPIO9	**General Purpose Input/Output**
50	In	DDC_SDA	**Serial Port Data to HDMI Receiver** The pin should be connected to data signal of HDMI DDC. This pin requires a pull-up 1.8 kΩ resistor to the desired voltage level
51	Out	DDC_SCL	**Serial Port Clock Output to HDMI Receiver** The pin should be connected to clock signal of HDMI DDC. This pin requires a pull-up 1.8kΩ resistor to the desired voltage level
52,53	In/Out	AUXN/AUXP	**AUX Channel Differential Input/Output** These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
54	In	RBIAS	**HDMI Swing Control** This pin sets the swing level of the HDMI outputs. A 1K-ohm with 1% tolerance resistor should be connected between this pin and ground using short and wide traces.
56,57	In	D0P/ D0N	**DP Main Link Differential Lane 0 Input** These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
60,61	In	D1P/ D1N	**DP Main Link Differential Lane 1 Input** These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
63,64	In	D2P/ D2N	**DP Main Link Differential Lane 2 Input** These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
67,68	In	D3P/ D3N	**DP Main Link Differential Lane 3 Input** These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
1	Power	VDDPLL	**PLL Power Supply (1.2V)**
2,25,41,55	Power	AVCC	**Analog Power Supply(3.3V)**
9	Power	AVCC5V	**Analog Power Supply (5V)**
11,42	Power	DVDD	**Digital Core/IO Power Supply (1.2V)**
12,43	Power	DGND	**Digital Ground**
18	Power	AVDDPLL	**PLL Power Supply (1.2V)**
21,29	Power	VDDS	**Serializer Power Supply (1.2V)**
22,28	Power	GNDS	**Ground**
58,59,65,66	Power	AVDD	**Analog Power Supply (1.2V)**
62	Power	AGND	**Analog Ground**

2.0 PACKAGE DIMENSION

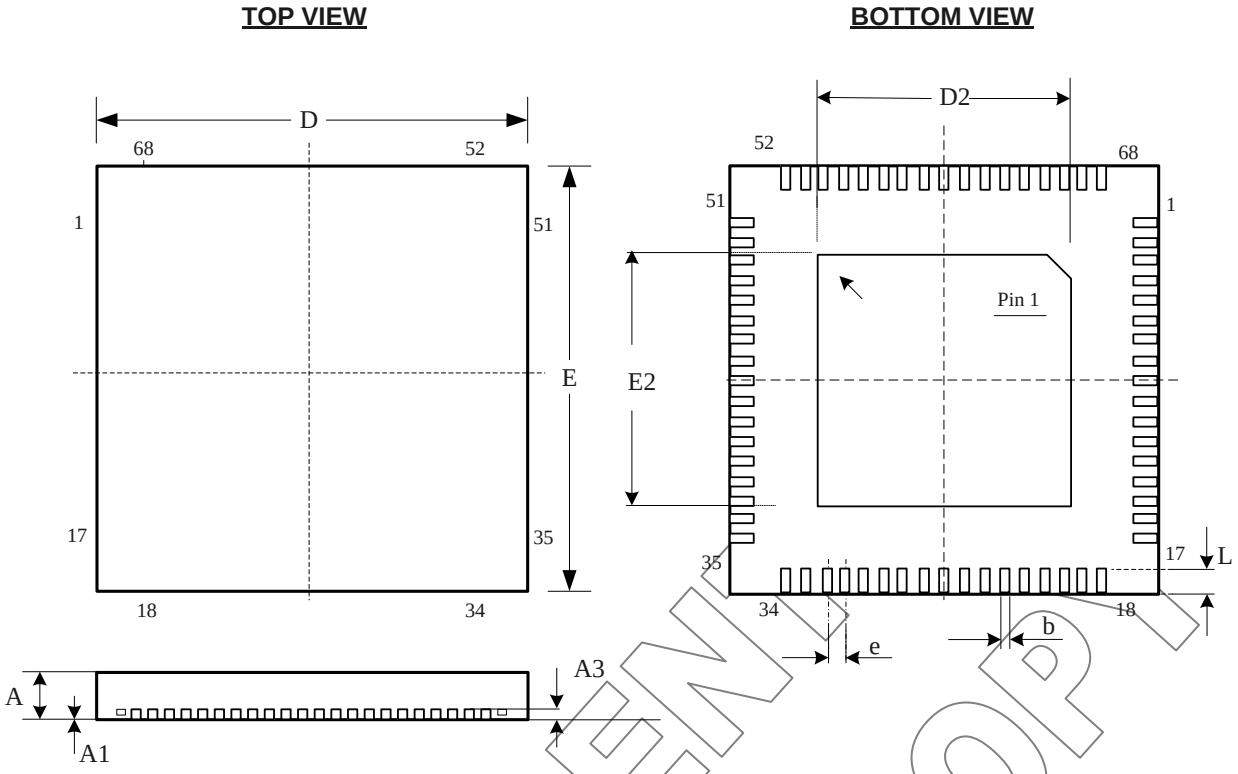

Figure 4: 68 Pin QFN Package (8x8 mm)

Table of Dimensions

No. of Leads		SYMBOL									
68 (8x8 mm)		D	E	D2	E2	e	b	L	A	A1	A3
Milli-meters	MIN	7.90	7.90	6.10	6.10	0.30	0.15	0.35	0.80	0.00	0.20REF
	MAX	8.10	8.10	6.30	6.30	0.50	0.25	0.45	0.90	0.05	

Notes:

1. All dimensions conform to JEDEC standard MO-207.

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ORDERING INFORMATION			
Part Number	**Package Type**	**Operating Temperature Range**	**Minimum Order Quantity**
CH7217A-BF	68 QFN, Lead-free	Commercial : 0 to 70°C	**260/Tray**

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