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## CH7530A DP++ to HDMI/DVI Level Shifter

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### FEATURES

- Compliant with DisplayPort Dual mode Specification version 1.1
- HDMI output is compliant with HDMI specification version 1.4b and DVI specification version 1.0
- HDMI output supports up to 300 MHz TMDS clock for video transport with resolution up to 4Kx2K@30Hz or 1920x1080@120Hz
- IIC-over-AUX transaction supported
- DDC buffer and related control register integrated
- HDMI Identifier supported
- Single 3.3V power supply
- 5V HDMI power supply output supported with over 50mA current output capability
- Programmable equalizer
- Programmable Pre-Emphasis on output driver supported
- CEC isolation switch supported
- Power saving mode supported
- Low power architecture
- Anti-Back Drive design on sink-side pins
- RoHS compliant and Halogen free package
- HBM 8KV (DP ++ main link pairs pass 5KV)
- Crystal free
- Offered in 40-Pin QFN Package (5 x 5 mm)

### GENERAL DESCRIPTIONS

Chrontel's CH7530A is a low-cost, low-power semiconductor device that translates the DisplayPort dual mode signal to HDMI/DVI signal. This innovative device, which integrates programmable equalizer, high speed TMDS level shifter and IIC to AUX translator, is specially designed to target the DP++ to HDMI/DVI adaptor device, docking station and PC market segments.

The CH7530A is compliant with the DisplayPort dual mode standard specification version 1.1. With sophisticated equalizer and high-speed TMDS level shifter integrated, the device's TMDS signal output is compliant with HDMI specification version 1.4b and DVI specification version 1.0, and supports video resolution up to 4Kx2K@30Hz or 1920x1080@120Hz for 3D applications.

The CH7530A also integrates the HDMI identifier, IIC over AUX translator and the related DDC control registers, which enables the programmable HDMI or DVI output and supports both DDC and AUX signaling on the upstream DisplayPort connector. With step-up regulator integrated, CH7530A supports 5V power supply output for HDMI/DVI configuration.

### Application

- DP++ to HDMI/DVI type 2 Cable Adaptor
- Docking Station
- Notebook/Ultrabook/AIO

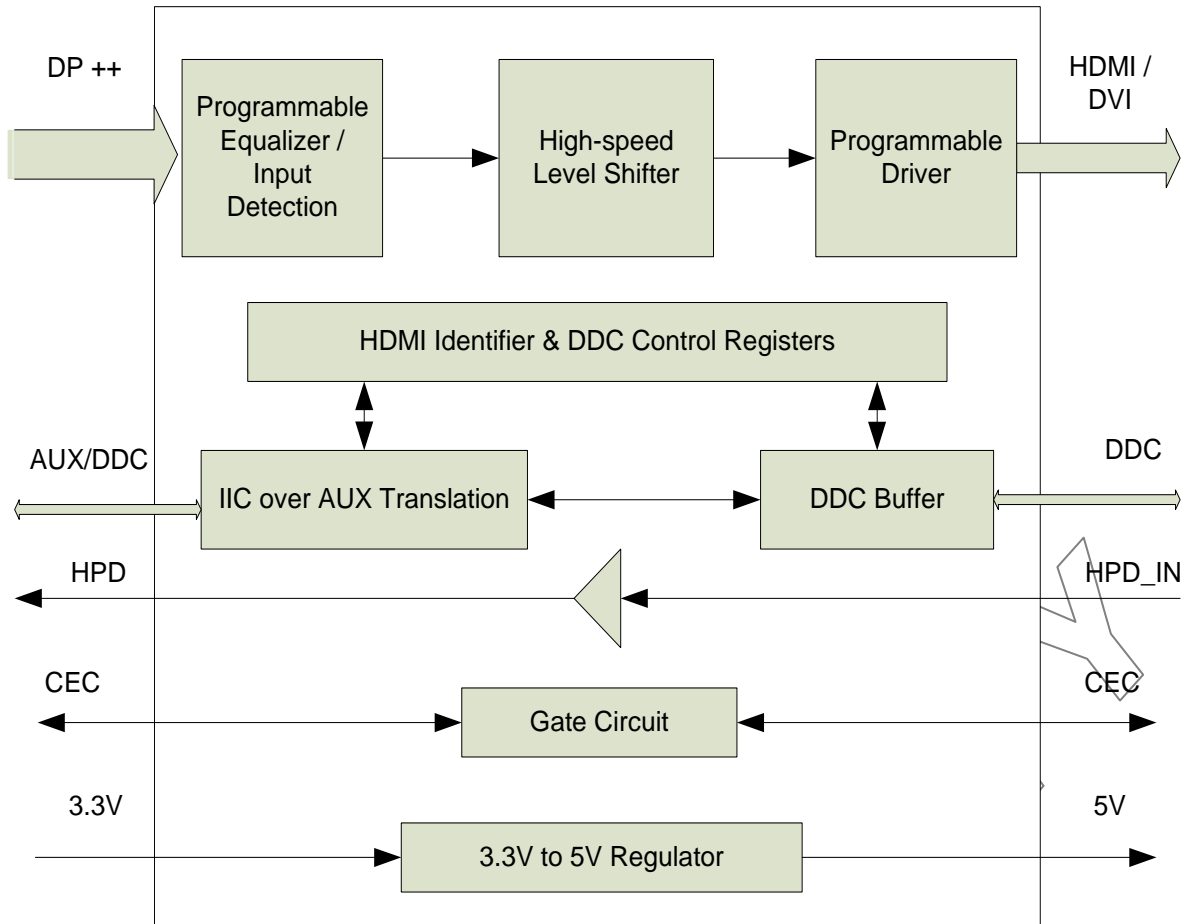


Figure 1: CH7530A Functional Block Diagram

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1.0 PIN-OUT

1.1 Package Diagram

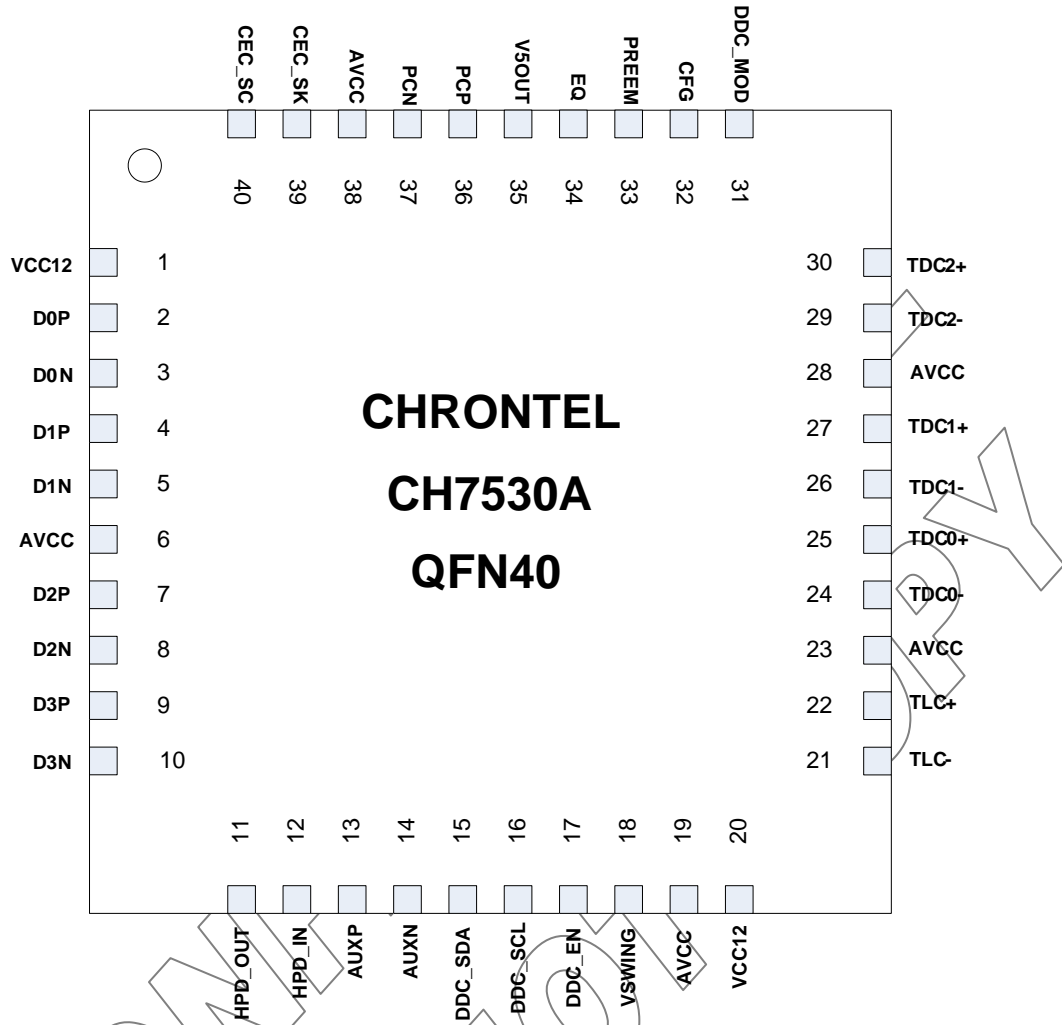


Figure 2: CH7530A 40-Pin QFN Pin Out

1.2 Pin Description

Table 1: CH7530A QFN 40-Pin Descriptions

Pin #	Type	Symbol	Description
2,3,4,5, 7,8,9,10	In	D[3:0]P/N	<b>DP Dual Mode Main Link Differential Line Input</b> These pins accept four AC-coupled differential pairs signals from the DisplayPort transmitter.
11	Out	HPD_OUT	<b>DP Dual Mode Receiver Hot Plug Output</b>
12	In	HPD_IN	<b>HDMI/DVI Transmitter Hot Plug Input</b>
13,14	In/Out	AUXP, AUXN	<b>AUX Channel Differential Input/Output</b> These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
15	In/Out	DDC_SDA	<b>Serial Port Data to HDMI/DVI Receiver</b> The pin should be connected to data signal of HDMI DDC. This pin requires a pull-up 2 kΩ resistor to the desired voltage level
16	Out	DDC_SCL	<b>Serial Port Clock Output to HDMI/DVI Receiver</b> The pin should be connected to clock signal of HDMI DDC. This pin requires a pull-up 2 kΩ resistor to the desired voltage level
17	In	DDC_EN	<b>Enables the DDC buffer and level shifter</b> When DDC_EN = LOW, buffer/level shifter is disabled. When DDC_EN = HIGH, buffer and level shifter are enabled To prevent the back drive from sink via DDC channel. This pin requires a pull-up kΩ resistor to AVCC
18	Out	VSWING	<b>HDMI/DVI Swing Control</b> This pin sets the swing level of the HDMI/DVI outputs. A 11.5kΩ with 1% tolerance resistor should be connected between this pin and TGND using short and wide traces.
21,22	Out	TLC-,TLC+	<b>HDMI/DVI Clock Outputs</b> These pins provide the differential clock output for the HDMI/DVI.
24,25	Out	TDC0-,TDC0+	<b>HDMI/DVI Data Channel 0 Outputs</b> These pins provide the DVI differential outputs for data channel 0
26,27	Out	TDC1-,TDC1+	<b>HDMI/DVI Data Channel 1 Outputs</b> These pins provide the DVI differential outputs for data channel 1
29,30	Out	TDC2-,TDC2+	<b>HDMI/DVI Data Channel 2 Outputs</b> These pins provide the DVI differential outputs for data channel 2
31	In	DDC_MOD	<b>DDC buffer selection</b> This pin can be board-strapped to one of four decode values: short to AVCC, 22kΩ resistor to AVCC, open-circuit, 22kΩ resistor to AVSS <sup>[1]</sup>
32	In	CFG	<b>HDMI/DVI selection</b> HIGH for HDMI, LOW for DVI
33	In	PREEM	<b>Pre-emphasis Setting</b> This pin can be board-strapped to one of five decode values: short to AVSS, 22kΩ resistor to AVSS, open-circuit, 22kΩ resistor to AVCC, short to AVCC <sup>[2]</sup>
34	In	EQ	<b>Programmable Equalizer Setting</b> Equalizer setting. This pin can be board-strapped to one of five decode values: short to AVSS, 22kΩ resistor to AVSS, open-circuit, 22kΩ resistor to AVCC, short to AVCC <sup>[3]</sup>
35	Out	V5OUT	<b>5V Power Supply Output</b> 5V regulated output from the integrated voltage regulator
36	In	PCP	<b>Positive terminal for the Power regulator external capacitor</b>
37	In	PCN	<b>Negative terminal for the Power regulator external capacitor</b>
39	In/Out	CEC_SK	<b>CEC Pin to HDMI Sink</b>

40	In/Out	CEC_SC	<b>CEC Pin to DP dual mode Source</b>
1,20	Power	VCC12	<b>Analog Power Supply (1.2V) with internal LDO</b>
6,19,23,28,38	Power	AVCC	<b>Analog Power Supply (3.3V)</b>
Thermal Pad	Power	AVSS	<b>Analog Ground</b>

Notes:

1. This pin provides DDC buffer configuration, the details are as follow:

**Table 2: Pin DDC\_MOD Configuration**

Options	Short to AVCC	22k to AVCC	OPEN CIRCUIT	22k or short to AVSS
<b>DDC buffer</b>	Active buffer	Passive buffer	Active buffer	Passive buffer
<b>PD_LDO</b>	0	0	1	1

2. **Table 3: Driver settings**

Options	Short to AVCC	22k to AVCC	OPEN CIRCUIT	22k to AVSS	Short to AVSS
<b>Driver Settings</b>	0dB	3dB	5dB	7dB	10dB

3. **Table 4: Equalizer settings**

Options	Short to AVCC	22k to AVCC	OPEN CIRCUIT	22k to AVSS	Short to AVSS
<b>EQ Settings</b>	1dB	4dB	7dB	10dB	13dB

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2.0 PACKAGE DIMENSIONS

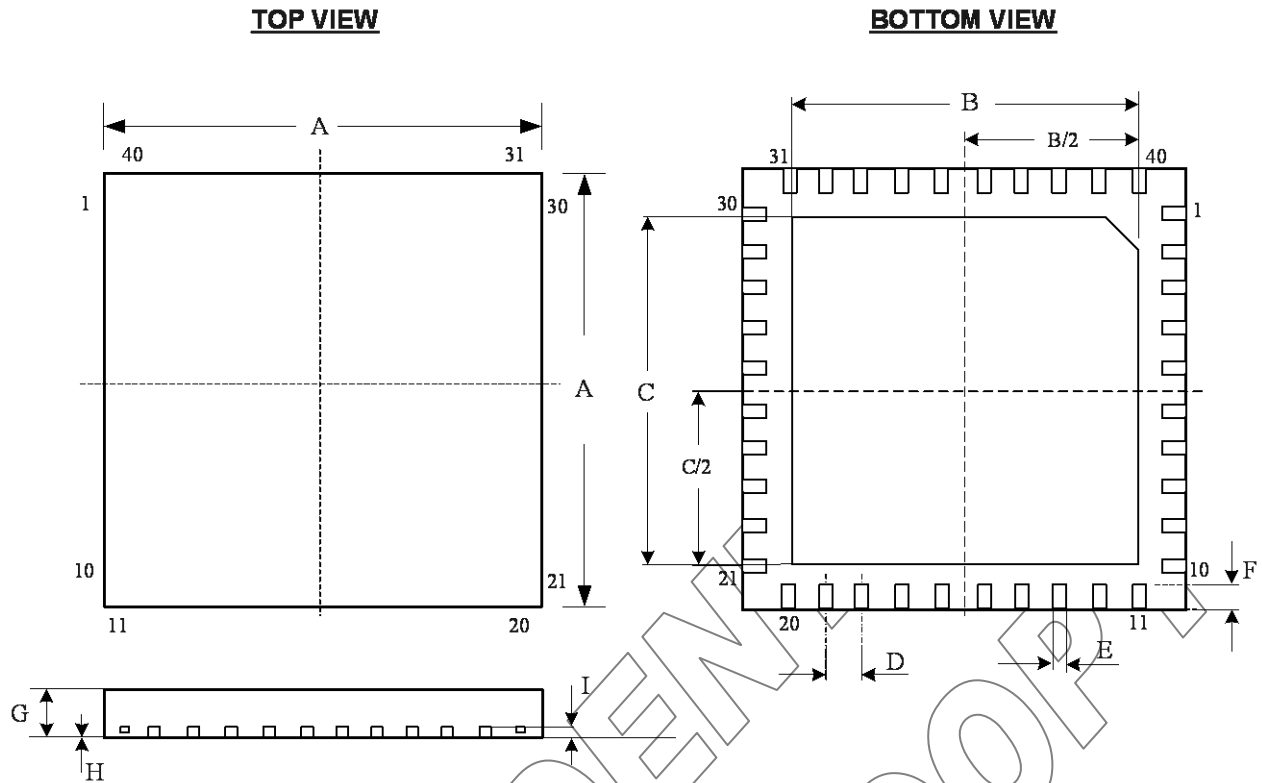


Figure 3: 40 Pin QFN Package

Table 5: Table of Dimensions

No. of Leads		SYMBOL								
40 (5 X 5 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	4.90	3.20	3.20	0.4	0.15	0.35	0.70	0	0.203
	MAX	5.10	3.40	3.40		0.25	0.45	0.80	0.05	REF

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

### 3.0 REVISION HISTORY

Rev. #	Date	Section	Description
0.1	02/18/2014	All	Initial Draft for CH7530A RevA
0.2	10/28/2014	Feature List 1.1, 1.2 2.0	Update the feature list Update the pin out and the description information Update the package dimensions
0.3	03/18/2015	1.2	Update the pin out description
0.4	03/30/2016	Feature List	Update the feature list
0.5	08/18/2016	1.2	Update the description of Vswing
0.6	08/23/2016	Feature 1.2	Update the feature list Update the description of Vswing, DDC_MOD, PREEM and EQ
1.0	07/18/2017	2.0	Update the package dimensions

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<b>ORDERING INFORMATION</b>			
<b>Part Number</b>	<b>Package Type</b>	<b>Operating Temperature Range</b>	<b>Minimum Order Quantity</b>
CH7530A-BF	40 QFN, Lead-free	Commercial : 0 to 70°C	490/Tray

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