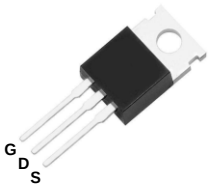
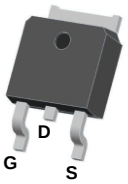
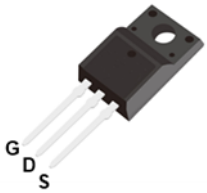
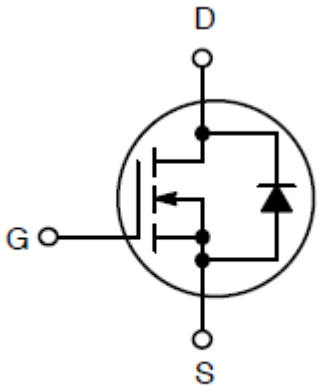
CPP65R600T4, CPD65R600T4
CPB65R600T4, CPA65R600T4

N-channel 650V, 0.5Ω typ.,
Super Junction MOSFET T4 in TO-220, TO-252, TO-263 and TO-220F

Datasheet - production data

1. Descriptions

TO-220	TO-252
	
TO-263	**TO-220F**
	
N-Channel MOSFET	
	
POWER MOSFET	

Key Performance Parameters

Parameters	Value	Unit
BV_{DSS}	650	V
$R_{DS(on),max}$	0.6	Ω
$Q_{g,typ}$	15	nC
$I_{D,pulse}$	24	A
E_{AS}	81	mJ

Features

• Extremely low losses due to very low FOM Rdson*Qg and Eoss.
• Very high commutation ruggedness.
• Qualified for industrial grade applications according to JEDEC.

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for Adapter, LCD TV, Lighting, and UPS.

Type/Ordering Code	Package	Marking	Related Links
CPP65R600T4	TO-220	65R600T4	See Appendix A
CPD65R600T4	TO-252		
CPB65R600T4	TO-263		
CPA65R600T4	TO-220F		

Contents

2. Maximum Ratings

at T_j = 25°C, unless otherwise specified

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
I_D	Continuous drain current[1]	- -	- -	8 5	A	T_C=25°C T_C=100°C
$I_{D,pulse}$	Pulsed drain current	-	-	24	A	T_C=25°C
E_{AS}	Avalanche energy, single pulse[2]	-	-	81	mJ	I_D=1.5A; V_{DD}=50V
I_{AR}	Avalanche current, repetitive	-	-	1.5	A	-
dv/dt	MOSFET dv/dt ruggedness	-	-	50	V/ns	V_{DS}=0...520V
V_{GS}	Gate source voltage	-30	-	30	V	static; AC (f>1 Hz)
P_{tot}	Power dissipation (Non FullPAK) TO-220, TO-252, TO-263	-	-	62.5	W	T_C=25°C
P_{tot}	Power dissipation (FullPAK) TO-220F	-	-	25.5	W	T_C=25°C
T_j, T_{stg}	Operating and storage temperature	-55	-	150	°C	-
I_S	Continuous diode forward current	-	-	8	A	T_C=25°C
$I_{S,pulse}$	Diode pulse current[1]	-	-	24	A	T_C=25°C
dv/dt	Reverse diode dv/dt[3]	-	-	15	V/ns	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C
di_f/dt	Maximum diode commutation speed[3]	-	-	500	A/µs	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C

1) Pulse width t_p limited by T_j,max.
2) V_{DD}=50V, R_G=25Ω, Starting T_j=25°C.
3) V_{DClink}=400V; $V_{DS,peak}$<$V_{(BR)DSS}$; identical low side and high side switch with identical R_G.

3. Thermal Characteristics

Table 2. Thermal Characteristics (Non FullPAK) TO-220, TO-252, TO-263

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
R_{thJC}	Thermal resistance, junction - case	-	-	2	°C/W	T_C = 25°C
R_{thJA}	Thermal resistance, junction - ambient	-	-	62	°C/W	T_C = 25°C
T_{sold}	Soldering temperature, wavesoldering only allowed at leads	-	-	260	°C	Lead Temperature (Soldering, 10 sec)

Table 3. Thermal Characteristics (FullPAK) TO-220F

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
R_{thJC}	Thermal resistance, junction - case	-	-	4.9	°C/W	T_C = 25°C
R_{thJA}	Thermal resistance, junction - ambient	-	-	49	°C/W	T_C = 25°C
T_{sold}	Soldering temperature, wavesoldering only allowed at leads	-	-	260	°C	Lead Temperature (Soldering, 10 sec)

4. Electrical Characteristics

at T_j = 25°C, unless otherwise specified

Table 4. Static Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
$V_{(BR)DSS}$	Drain-source breakdown voltage	650	-	-	V	V_{GS}=0V, I_D=250μA
$V_{(GS)th}$	Gate threshold voltage	2.0	-	4.0	V	V_{DS}=V_{GS}, I_D=250μA
I_{DSS}	Zero gate voltage drain current	-	-	1 10	μA	V_{DS}=650V, V_{GS}=0V, T_j=25°C V_{DS}=650V, V_{GS}=0V, T_j=150°C
I_{GSS}	Gate-source leakage current	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0V
$R_{DS(on)}$	Drain-source on-state resistance	-	0.5	0.6	Ω	V_{GS}=10V, I_D=3.5A, T_j=25°C
R_G	Gate resistance	-	3.6	-	Ω	V_{DD}=0V,V_{GS}=0V,F=1MHz

Table 5. Dynamic Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
C_{iss}	Input capacitance	-	370	-	pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
C_{oss}	Output capacitance	-	23	-	pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
C_{rss}	Reverse transfer capacitance	-	1.3	-	pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
$C_{o(er)}$	Effective output capacitance, energy related[1)]	-	16	-	pF	V_{GS}=0V, V_{DS}=0 to 400V
$C_{o(tr)}$	Effective output capacitance, time related[2)]	-	87	-	pF	V_{GS}=0V, V_{DS}=0 to 400V
$t_{d(on)}$	Turn-on delay time	-	18	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=4A
t_r	Rise time	-	12	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=4A
$t_{d(off)}$	Turn-off delay time	-	50	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=4A
t_f	Fall time	-	16	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=4A

Table 6. Gate Charge Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
Q_{gs}	Gate to source charge	-	2.4	-	nC	V_{DD}=480V, I_D=4A, V_{GS}=0 to 10V
Q_{gd}	Gate to drain charge	-	9	-	nC	V_{DD}=480V, I_D=4A, V_{GS}=0 to 10V
Q_g	Gate charge total	-	15	-	nC	V_{DD}=480V, I_D=4A, V_{GS}=0 to 10V
$V_{plateau}$	Gate plateau voltage	-	6	-	V	V_{DD}=480V, I_D=4A, V_{GS}=0 to 10V

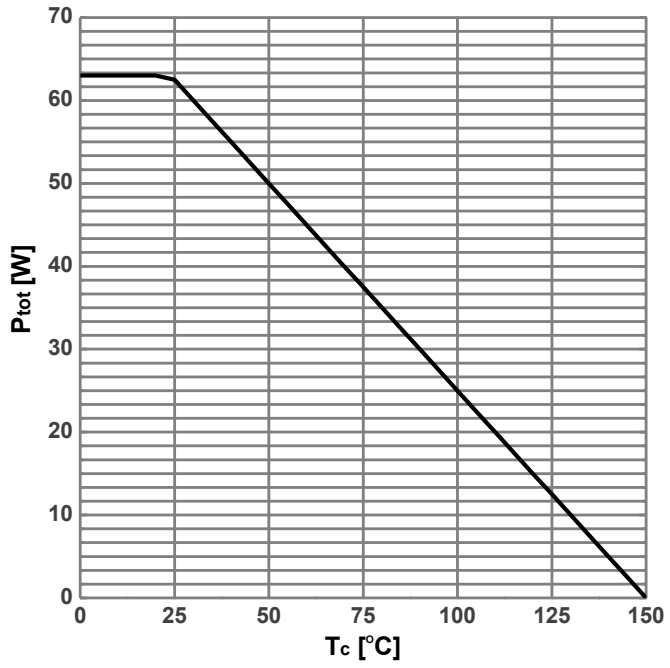
1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.
2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V.

Table 7. Reverse Diode Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{SD}	Diode forward voltage	-	0.86	-	V	V_{GS}=0V, I_F=4A, T_f=25°C
t_{rr}	Reverse recovery time	-	200	-	ns	V_R=400V, I_F=4A, di_F/dt=100A/μs
Q_{rr}	Reverse recovery charge	-	1.25	-	μC	V_R=400V, I_F=4A, di_F/dt=100A/μs
I_{rrm}	Peak reverse recovery current	-	14	-	A	V_R=400V, I_F=4A, di_F/dt=100A/μs

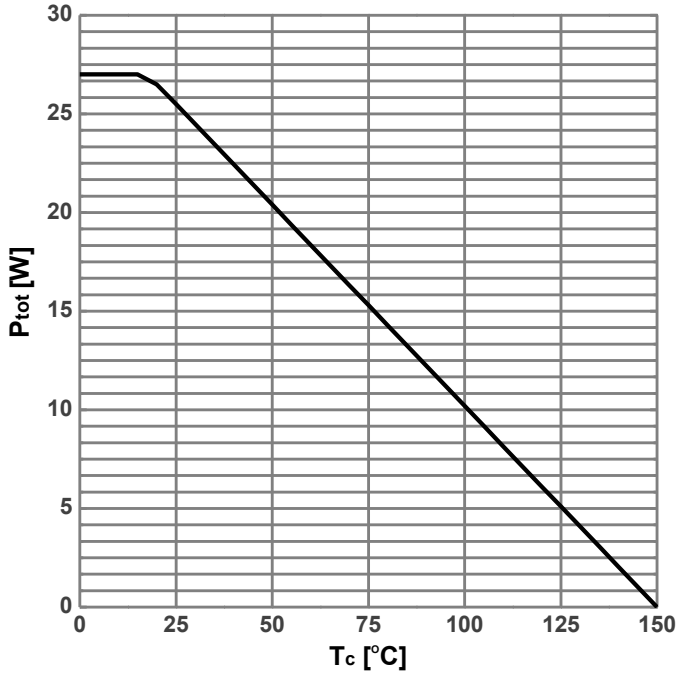
5. Electrical Characteristics Diagrams

Diagram 1: Power dissipation (Non FullPAK)



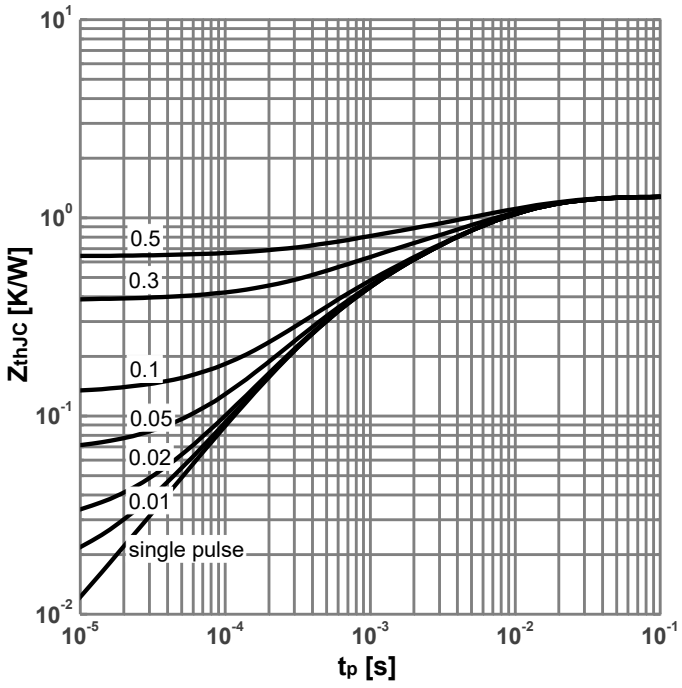
$P_{tot}=f(T_C)$

Diagram 2: Power dissipation (FullPAK)



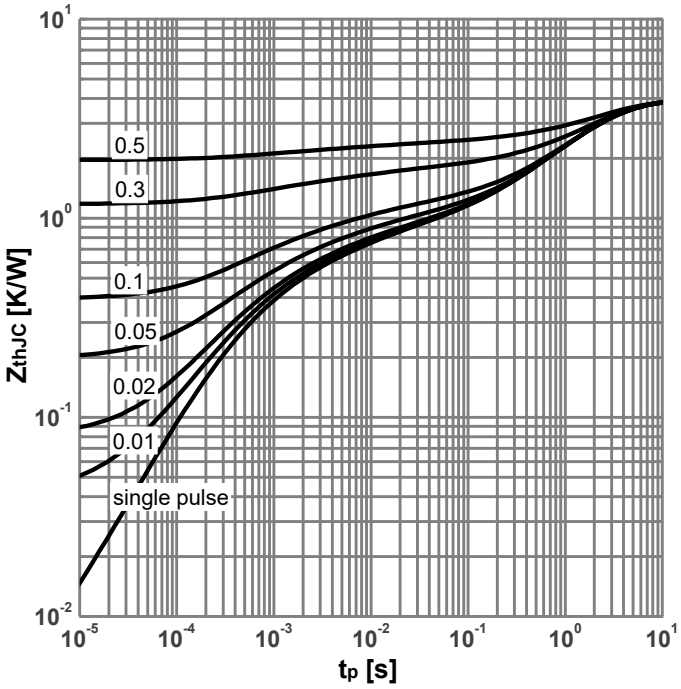
$P_{tot}=f(T_C)$

Diagram 3: Max. transient thermal impedance (Non FullPAK)



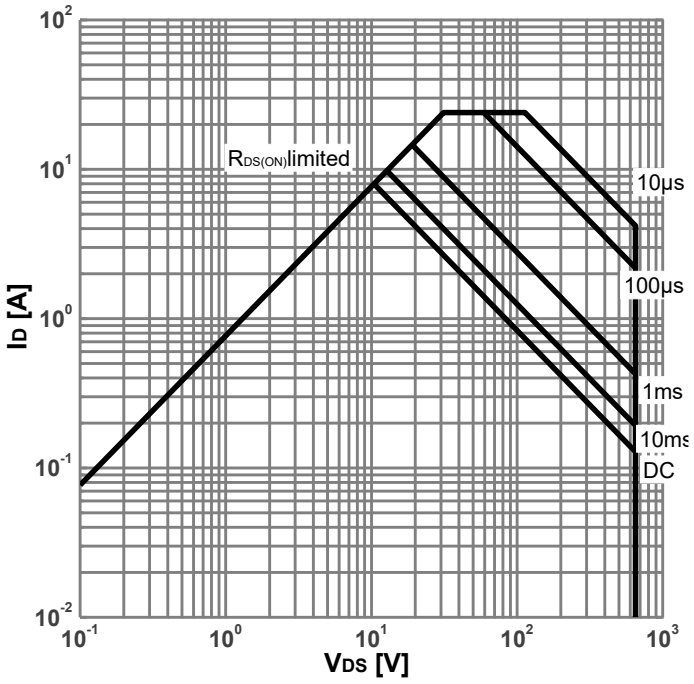
$Z_{thJC}=f(t_p)$; parameter: D= t_p/T

Diagram 4: Max. transient thermal impedance (FullPAK)



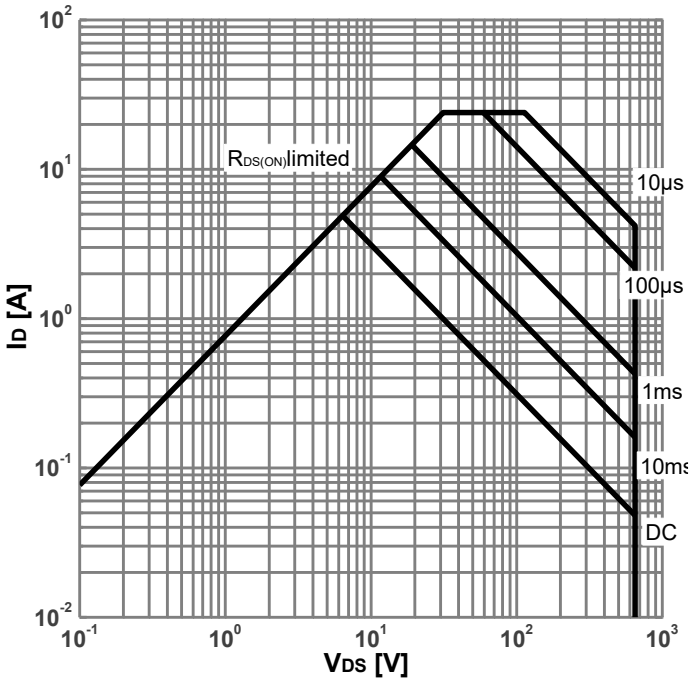
$Z_{thJC}=f(t_p)$; parameter: D= t_p/T

Diagram 5: Safe operating area (Non FullPAK)



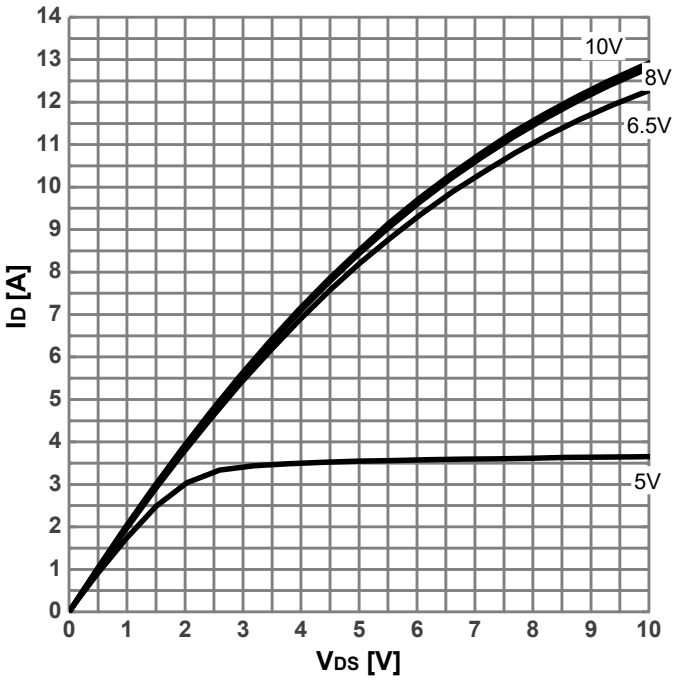
I_D=f(V_{DS}); Tj=25°C; D=0; parameter: t_p

Diagram 6: Safe operating area (FullPAK)



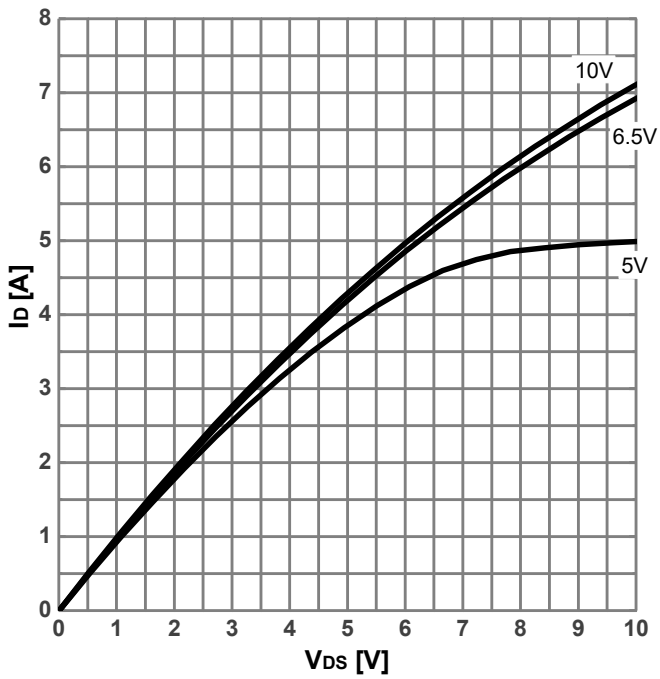
I_D=f(V_{DS}); Tj=25°C; D=0; parameter: t_p

Diagram 7: Typ. output characteristics



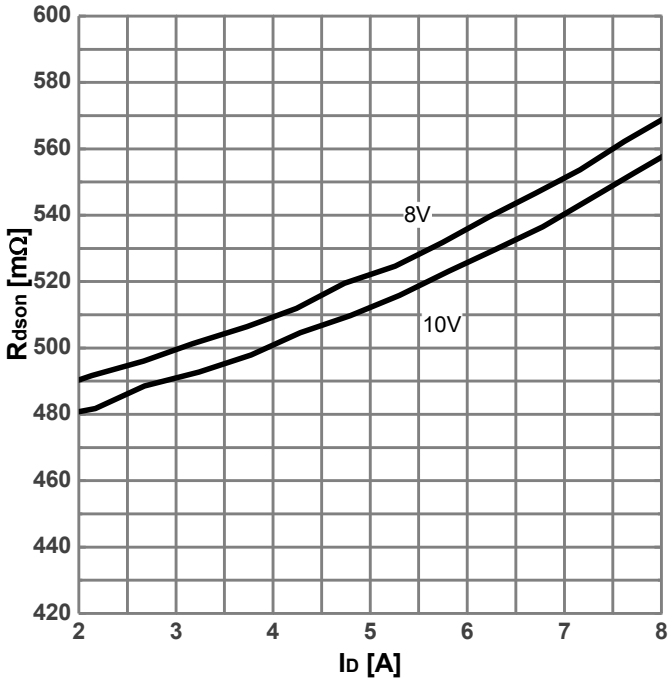
I_D=f(V_{DS}); Tj=25°C; parameter: V_{GS}

Diagram 8: Typ. output characteristics



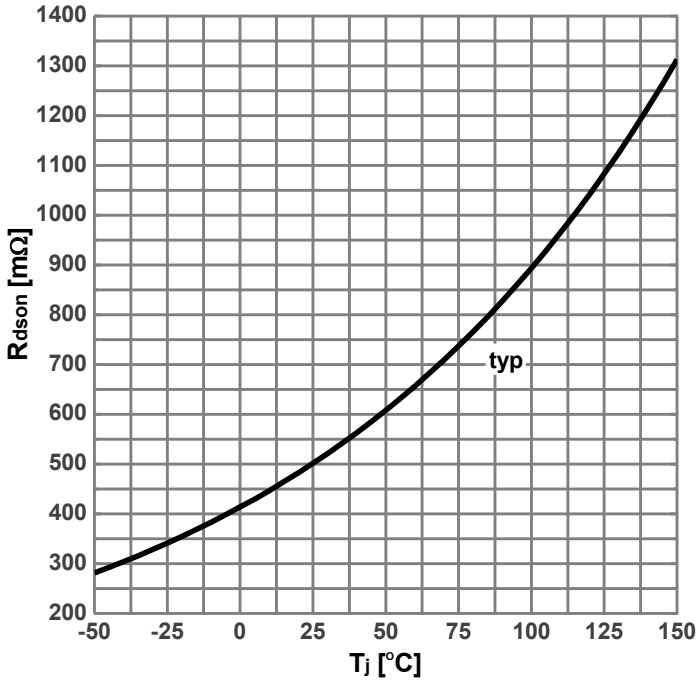
I_D=f(V_{DS}); Tj=125°C; parameter: V_{GS}

Diagram 9: Typ. drain-source on-state resistance



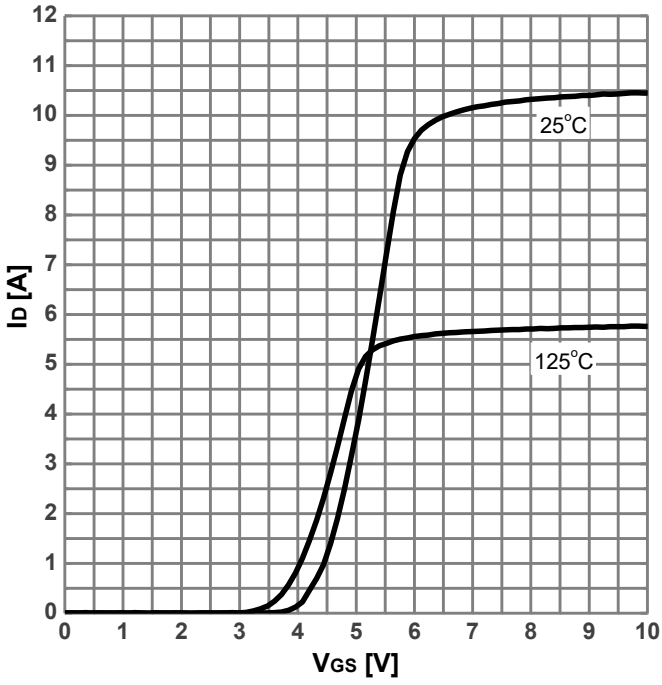
$R_{DS}(on)=f(I_D)$; $Tj=25°C$; parameter: V_{GS}

Diagram 10: drain-source on-state resistance



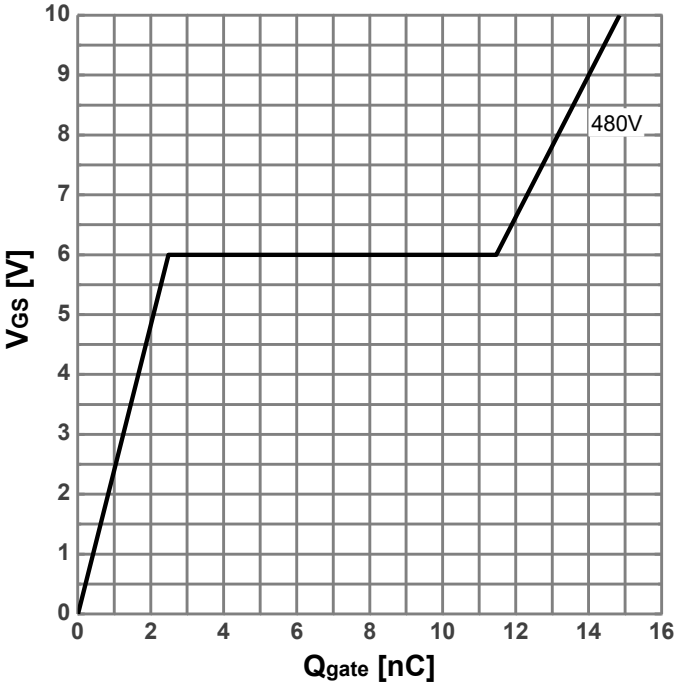
$R_{DS}(on)=f(T_j)$; $I_D=3.5A$; $V_{GS}=10V$

Diagram 11: Typ. transfer characteristics



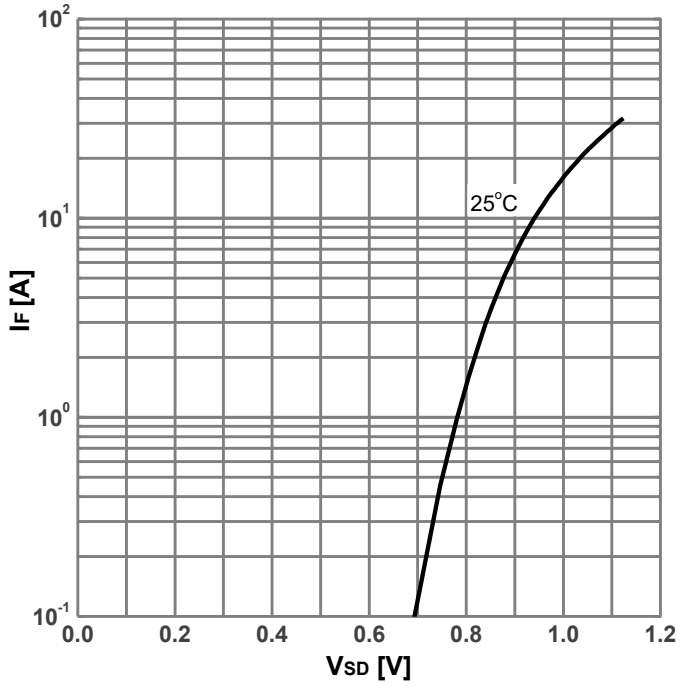
$I_D=f(V_{GS})$; $V_{DS}=20V$; parameter: T_j

Diagram 12: Typ. gate charge



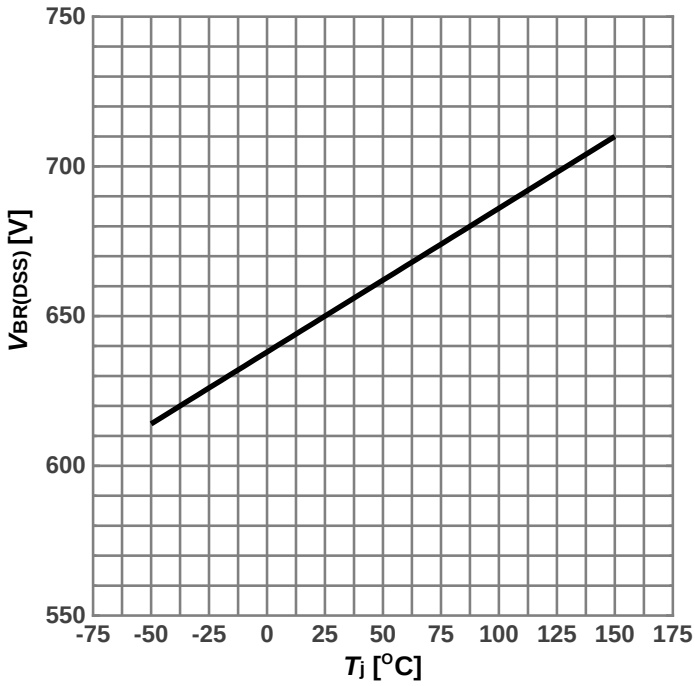
$V_{GS}=f(Q_{gate})$; $I_D=4A$ pulsed; $V_{DS}=480V$

Diagram 13: Forward characteristics of reverse diode



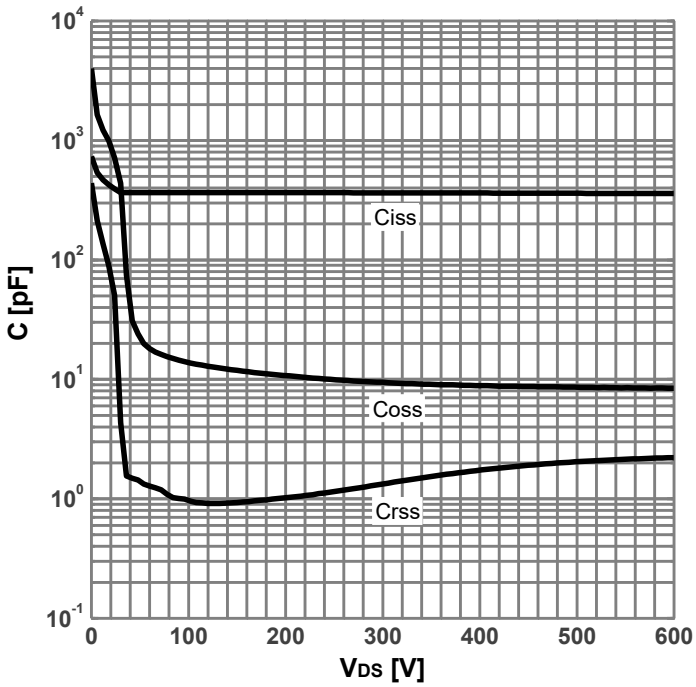
$I_F=f(V_{SD})$; parameter: T_j

Diagram 14: Drain-source breakdown voltage



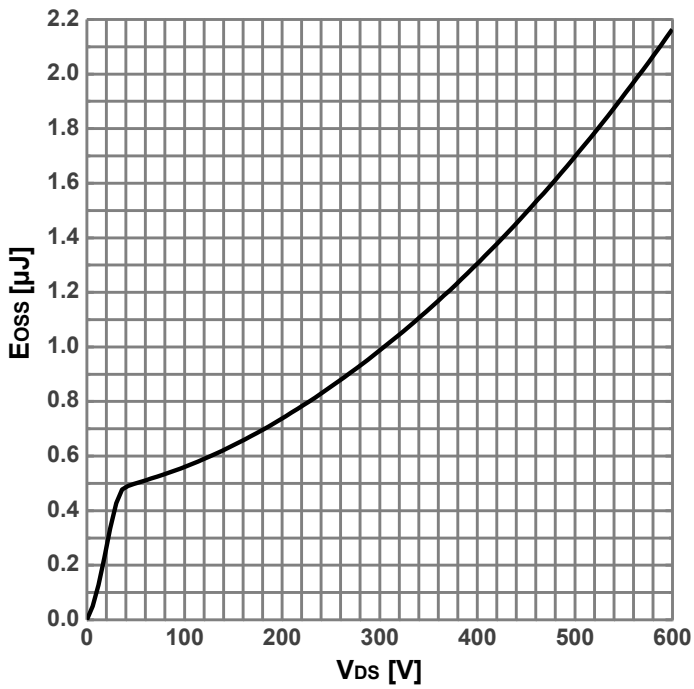
$V_{BR(DSS)}=f(T_j)$; I_D=250µA

Diagram 15: Typ. capacitances



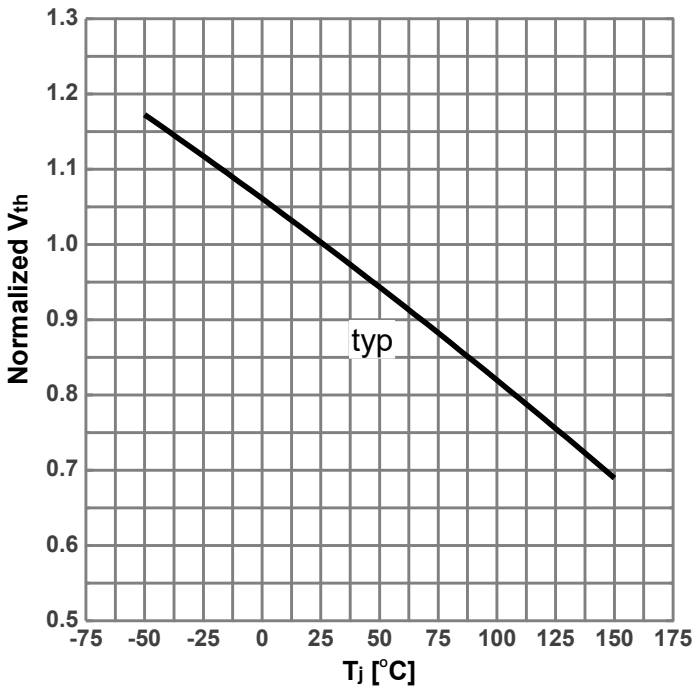
$C=f(V_{DS})$; V_{GS}=0V; f=1MHz

Diagram 16: Typ. Coss stored energy



$E_{OSS}=f(V_{DS})$

Diagram 17: Gate threshold voltage vs. Junction temperature



V_{th}=f(T_j); I_D=250μA

6. Test Circuits

Table 8. Diode Characteristics

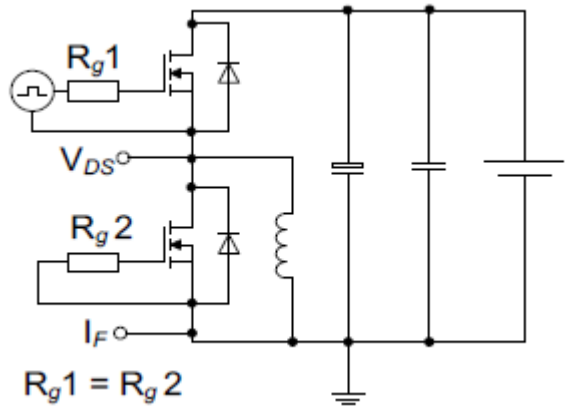
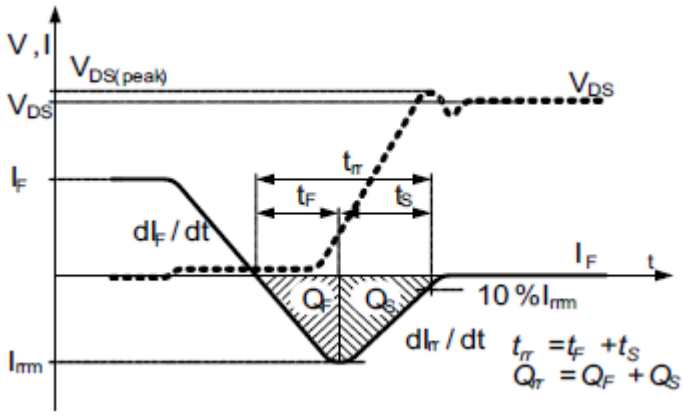
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9. Switching Times

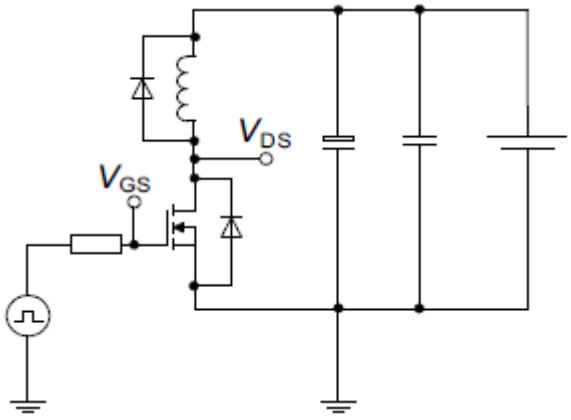
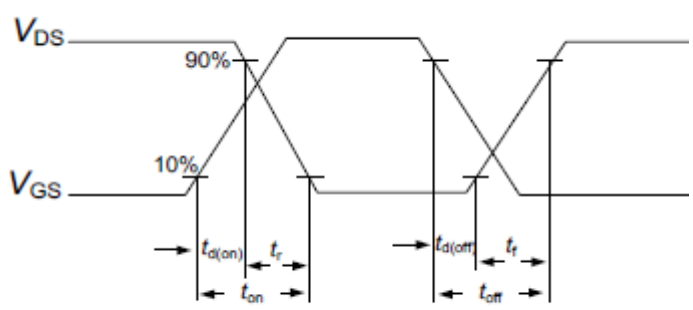
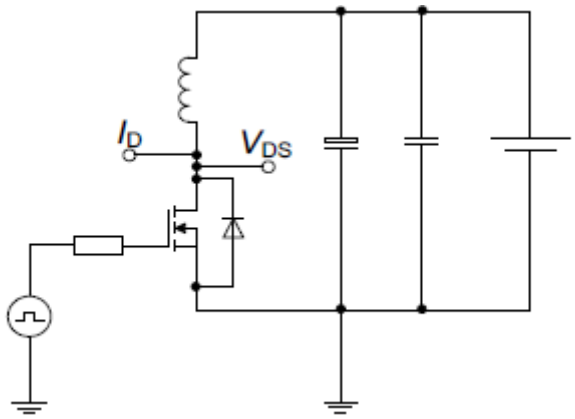
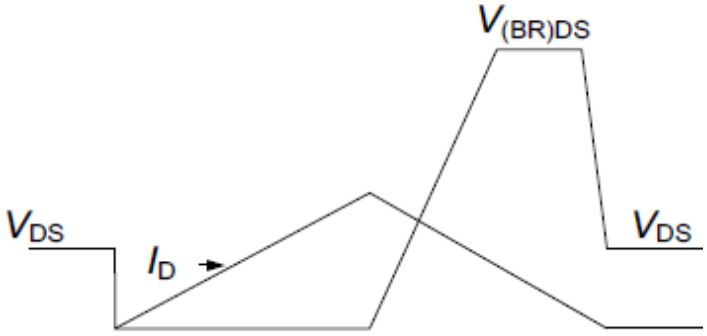
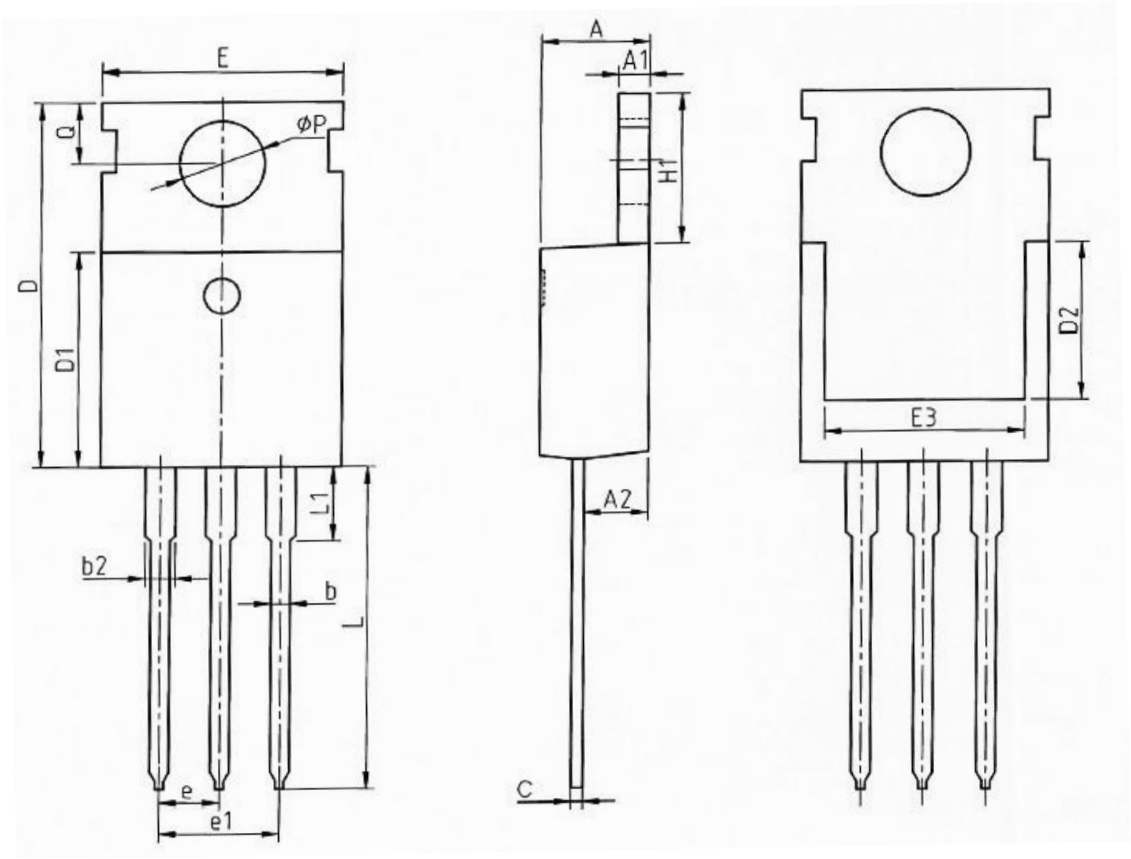
Switching times test circuit for inductive load	Switching times waveform
	

Table 10. Unclamped Inductive Load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

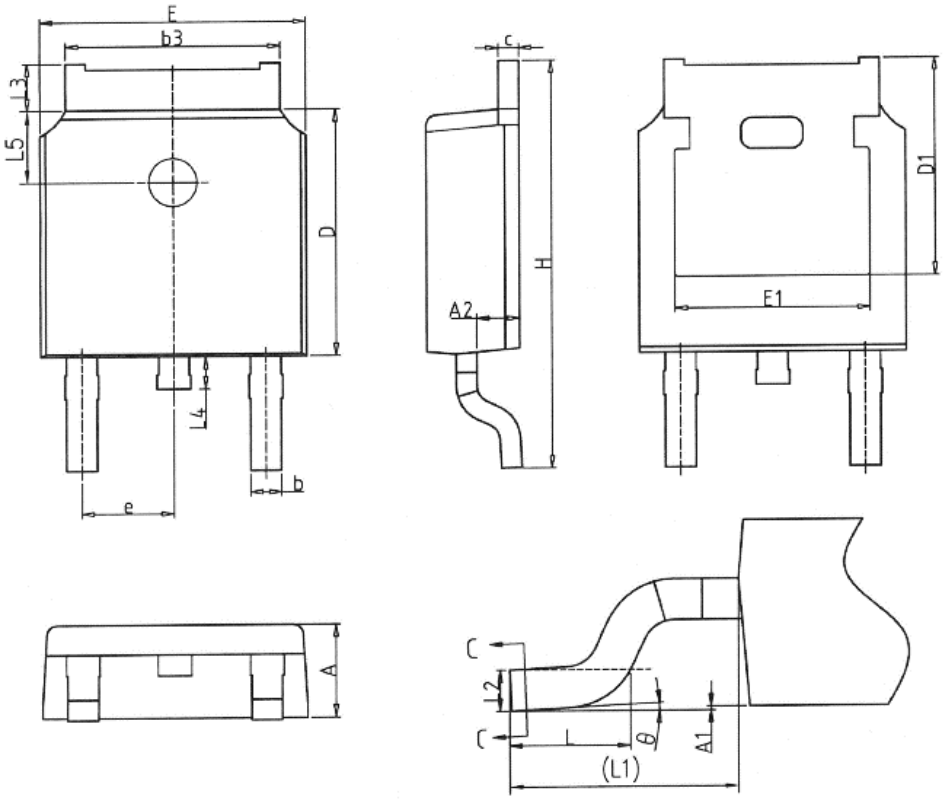
7. Package Outlines

Figure 1 Outline TO-220 Dimensions in mm



Dimensions In Millimeters		
Symbol	**Min**	**Max**
A	4.37	4.70
A1	1.25	1.40
A2	2.20	2.60
b	0.70	0.95
b2	1.17	1.47
c	0.45	0.60
D	15.10	16.10
D1	8.80	9.40
D2	5.50	-
E	9.70	10.30
E3	7.00	-
e	2.54BSC	
e1	5.08BSC	
H1	6.25	6.85
L	12.75	13.80
L1	-	3.40
ΦP	3.40	3.80
Q	2.60	3.00

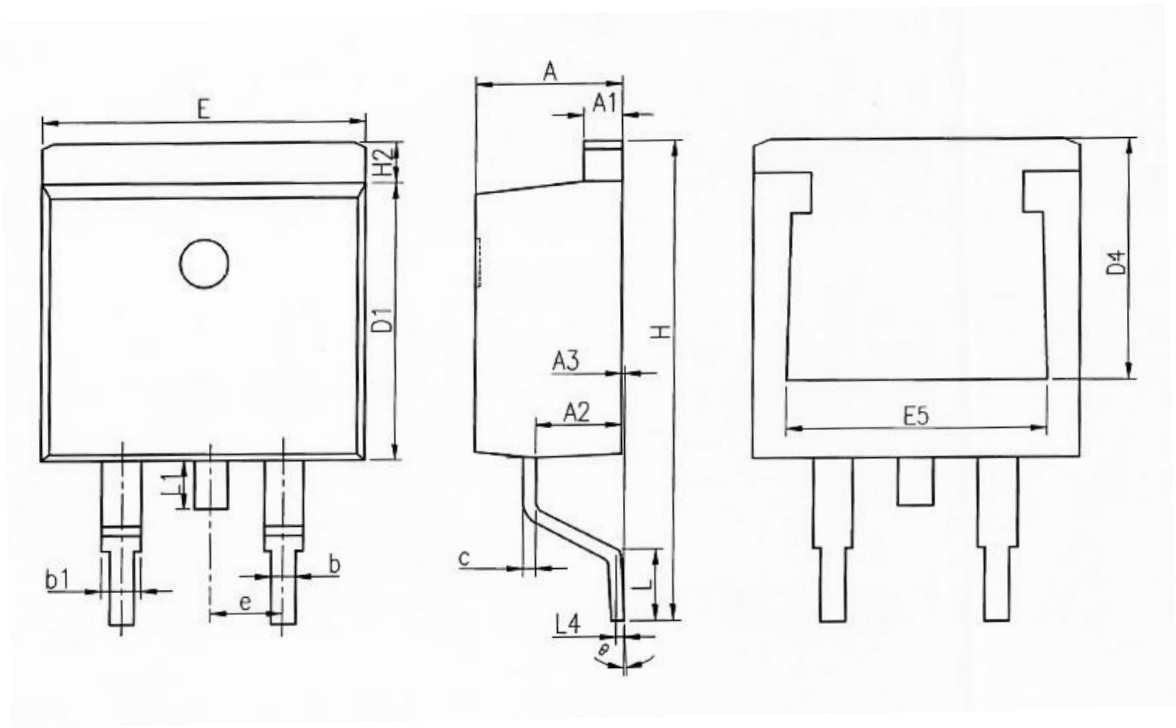
Figure 2 Outline TO-252 Dimensions in mm



NOTES
1.ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AA,
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

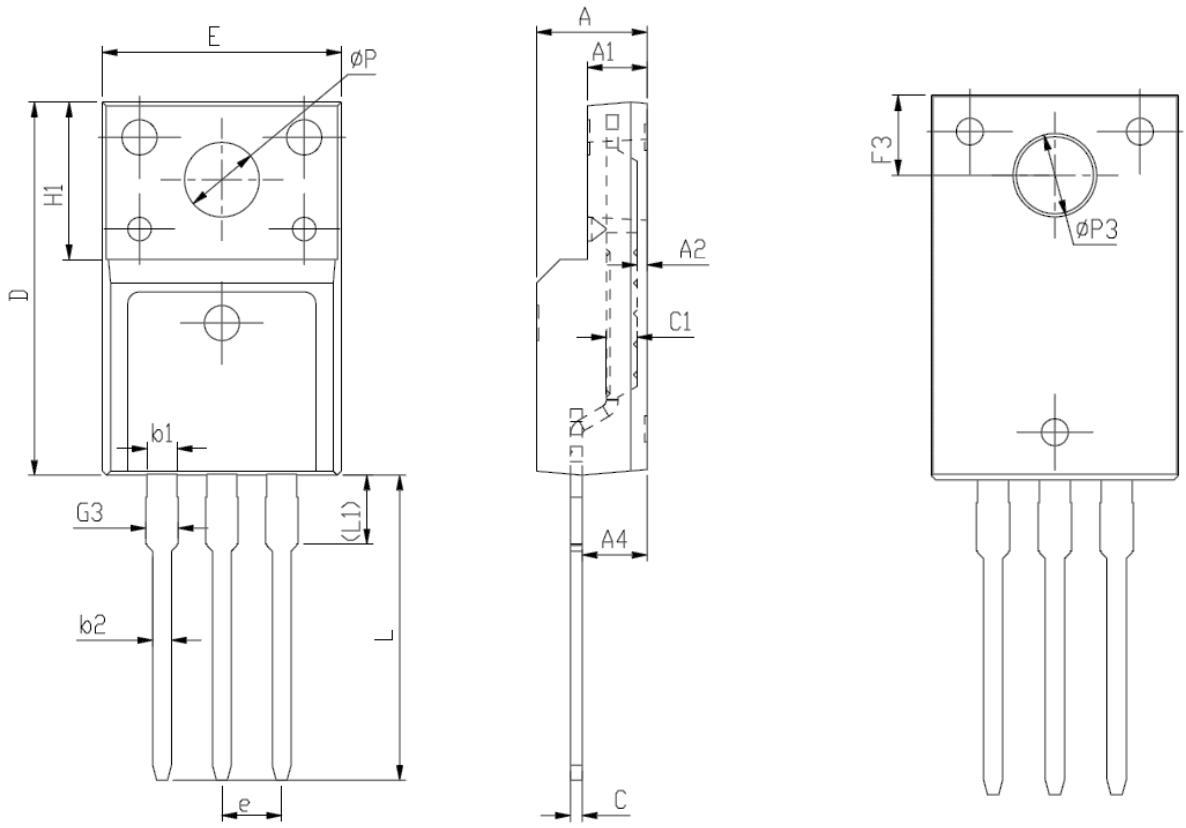
Dimensions In Millimeters		
Symbol	**Min**	**Max**
A	2.20	2.38
A1	0.00	0.20
A2	0.97	1.17
b	0.68	0.90
b3	5.20	5.46
c	0.43	0.61
D	5.98	6.22
D1	5.30REF	
E	6.40	6.73
E1	4.63	-
c	2.286BSC	
H	9.40	10.50
L	1.38	1.75
L1	2.60REF	
L2	0.51BSC	
L3	0.88	1.28
L4	0.50	1.00
L5	1.65	1.95
θ	0°	8°

Figure 3 Outline TO-263 Dimensions in mm



Dimensions In Millimeters		
Symbol	**Min**	**Max**
A	4.37	4.77
A1	1.22	1.42
A2	2.49	2.89
A3	0.00	0.25
b	0.70	0.96
b1	1.17	1.47
c	0.30	0.53
D1	8.50	8.90
D4	6.60	-
E	9.86	10.36
E5	7.06	-
c	2.54BSC	
H	14.70	15.50
H2	1.07	1.47
L	2.00	2.60
L1	1.40	1.70
L4	0.25BSC	
θ	0°	9°

Figure 4 Outline TO-220 FullPAK Dimensions in mm



Dimensions In Millimeters		
Symbol	**Min**	**Max**
E	9.96	10.36
A	4.50	4.90
A1	2.34	2.74
A2	0.30	0.60
A4	2.56	2.96
c	0.40	0.65
c1	1.20	1.35
D	15.57	16.17
H1	6.70REF	
e	2.54BSC	
L	12.68	13.28
L1	3.03	3.43
ΦP	3.03	3.38
ΦP3	3.15	3.65
F3	3.15	3.45
G3	1.25	1.55
b1	1.18	1.43
b2	0.70	0.95

8. Appendix

CoolSemi Webpage: www.coolsemi.com.

单击下面可查看定价，库存，交付和生命周期等信息

>>CoolSemi