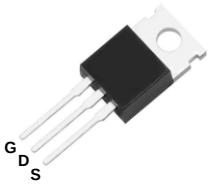
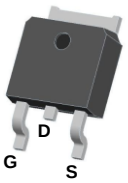
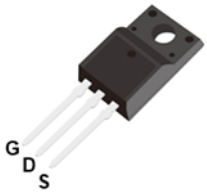
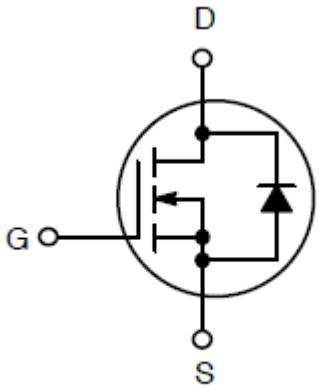
CPP65R380T4, CPD65R380T4
CPB65R380T4, CPA65R380T4

N-channel 650V, 0.34Ω typ.,
Super Junction MOSFET T4 in TO-220, TO-252, TO-263 and TO-220F

Datasheet - production data

1. Descriptions

TO-220	TO-252
	
TO-263	**TO-220F**
	
N-Channel MOSFET	
 POWER MOSFET	

Key Performance Parameters

Parameters	Value	Unit
BV_{DSS}	650	V
$R_{DS(on),max}$	0.38	Ω
$Q_{g,typ}$	23.5	nC
$I_{D,pulse}$	31	A
E_{AS}	225	mJ

Features

• Extremely low losses due to very low FOM Rdson*Qg and Eoss.
• Very high commutation ruggedness.
• Qualified for industrial grade applications according to JEDEC.

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for Adapter, LCD TV, Lighting, and UPS.

Type/Ordering Code	Package	Marking	Related Links
CPP65R380T4	TO-220	65R380T4	See Appendix A
CPD65R380T4	TO-252		
CPB65R380T4	TO-263		
CPA65R380T4	TO-220F		

Contents

2. Maximum Ratings

at T_j = 25°C, unless otherwise specified

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{DS}	Drain-source voltage[1]	-	-	650	V	V_{GS}=0V, I_D=250μA
I_D	Continuous drain current[2]	- -	- -	10.5 4.7	A	T_C=25°C T_C=125°C
$I_{D,pulse}$	Pulsed drain current	-	-	31	A	T_C=25°C
E_{AS}	Avalanche energy, single pulse[3]	-	-	225	mJ	I_D=3A; V_{DD} =50V
I_{AR}	Avalanche current, repetitive	-	-	3	A	-
dv/dt	MOSFET dv/dt ruggedness	-	-	50	V/ns	V_{DS} =0...520V
V_{GS}	Gate source voltage	-30	-	30	V	static; AC (f>1 Hz)
P_{tot}	Power dissipation (Non FullPAK) TO-220, TO-252, TO-263	-	-	104.2	W	T_C=25°C
P_{tot}	Power dissipation (FullPAK) TO-220F	-	-	32	W	T_C=25°C
T_j, T_{stg}	Operating and storage temperature	-55	-	150	°C	-
I_S	Continuous diode forward current	-	-	10.5	A	T_C=25°C
$I_{S,pulse}$	Diode pulse current[2]	-	-	31	A	T_C=25°C
dv/dt	Reverse diode dv/dt[4]	-	-	15	V/ns	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C
di_f/dt	Maximum diode commutation speed[4]	-	-	500	A/μs	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C

1) Limited by T_j max. Maximum duty cycle D=0.75.
2) Pulse width t_p limited by T_j,max.
3) V_{DD}=50V, R_G=25Ω, Starting T_j=25°C.
4) V_{DClink}=400V; $V_{DS,peak}$<$V_{(BR)DSS}$; identical low side and high side switch with identical R_G.

3. Thermal Characteristics

Table 2. Thermal Characteristics (Non FullPAK) TO-220, TO-252, TO-263

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
R_{thJC}	Thermal resistance, junction - case	-	-	1.2	°C/W	T_C = 25°C
R_{thJA}	Thermal resistance, junction - ambient	-	-	62	°C/W	T_C = 25°C
T_{sold}	Soldering temperature, wavesoldering only allowed at leads	-	-	260	°C	Lead Temperature (Soldering, 10 sec)

Table 3. Thermal Characteristics (FullPAK) TO-220F

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
R_{thJC}	Thermal resistance, junction - case	-	-	3.9	°C/W	T_C = 25°C
R_{thJA}	Thermal resistance, junction - ambient	-	-	62.5	°C/W	T_C = 25°C
T_{sold}	Soldering temperature, wavesoldering only allowed at leads	-	-	260	°C	Lead Temperature (Soldering, 10 sec)

4. Electrical Characteristics

at T_j = 25°C, unless otherwise specified

Table 4. Static Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
$V_{(BR)DSS}$	Drain-source breakdown voltage	650	-	-	V	V_{GS}=0V, I_D=250μA
$V_{(GS)th}$	Gate threshold voltage	2.0	-	4.0	V	V_{DS}=V_{GS}, I_D=250μA
I_{DSS}	Zero gate voltage drain current	-	-	1	μA	V_{DS}=650V, V_{GS}=0V, T_j=25°C
I_{GSS}	Gate-source leakage current	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0V
$R_{DS(on)}$	Drain-source on-state resistance	-	0.34	0.38	Ω	V_{GS}=10V, I_D=5.5A, T_j=25°C
R_G	Gate resistance	-	4	-	Ω	V_{DD}=0V,V_{GS}=0V,F=1MHz

Table 5. Dynamic Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
C_{iss}	Input capacitance	-	630	-	pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
C_{oss}	Output capacitance	-	33	-	pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
C_{rss}	Reverse transfer capacitance	-	1.4	-	pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
$C_{o(er)}$	Effective output capacitance, energy related[1)]	-	25	-	pF	V_{GS}=0V, V_{DS}=0 to 400V
$C_{o(tr)}$	Effective output capacitance, time related[2)]	-	128	-	pF	V_{GS}=0V, V_{DS}=0 to 400V
$t_{d(on)}$	Turn-on delay time	-	57	-	ns	V_{DD}=480V, V_{GS}=10V, I_D=5A
t_r	Rise time	-	30	-	ns	V_{DD}=480V, V_{GS}=10V, I_D=5A
$t_{d(off)}$	Turn-off delay time	-	73	-	ns	V_{DD}=480V, V_{GS}=10V, I_D=5A
t_f	Fall time	-	15	-	ns	V_{DD}=480V, V_{GS}=10V, I_D=5A

Table 6. Gate Charge Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
Q_{gs}	Gate to source charge	-	2.5	-	nC	V_{DD}=480V, I_D=5A, V_{GS}=0 to 10V
Q_{gd}	Gate to drain charge	-	9	-	nC	V_{DD}=480V, I_D=5A, V_{GS}=0 to 10V
Q_g	Gate charge total	-	23.5	-	nC	V_{DD}=480V, I_D=5A, V_{GS}=0 to 10V
$V_{plateau}$	Gate plateau voltage	-	5	-	V	V_{DD}=480V, I_D=5A, V_{GS}=0 to 10V

1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.
2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V.

Table 7. Reverse Diode Characteristics

Symbol	Parameter	Values			Unit	Test Condition
		Min.	Typ.	Max.		
V_{SD}	Diode forward voltage	-	0.85	-	V	V_{GS}=0V, I_F=5.5A, T_f=25°C
t_{rr}	Reverse recovery time	-	210	-	ns	V_R=480V, I_F=5A, di_F/dt=100A/μs
Q_{rr}	Reverse recovery charge	-	1.29	-	μC	V_R=480V, I_F=5A, di_F/dt=100A/μs
I_{rrm}	Peak reverse recovery current	-	16	-	A	V_R=480V, I_F=5A, di_F/dt=100A/μs

5. Electrical Characteristics Diagrams

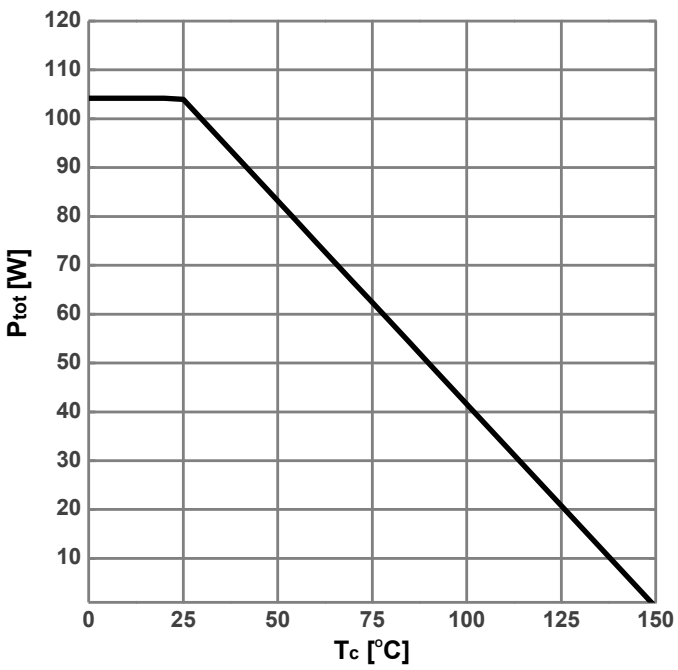
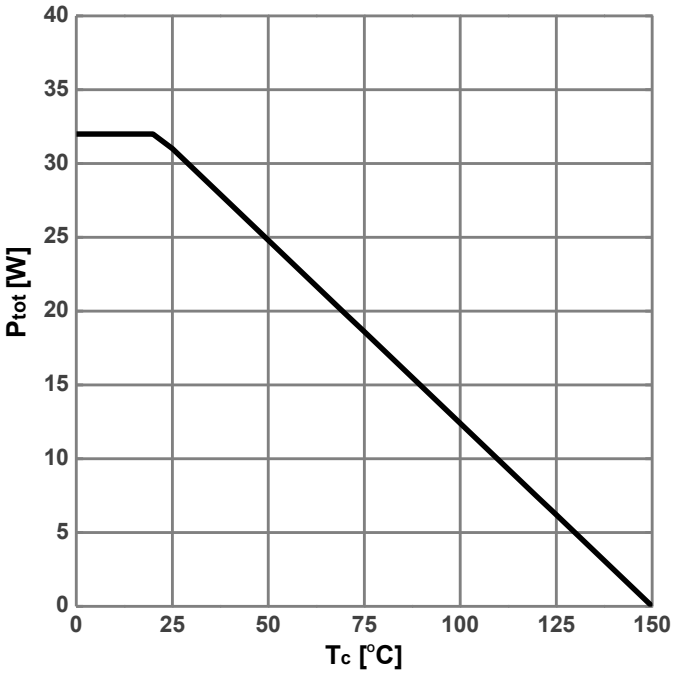
Diagram 1: Power dissipation (Non FullPAK)	Diagram 2: Power dissipation (FullPAK)
	
P_{tot}=f(T_C)	P_{tot}=f(T_C)

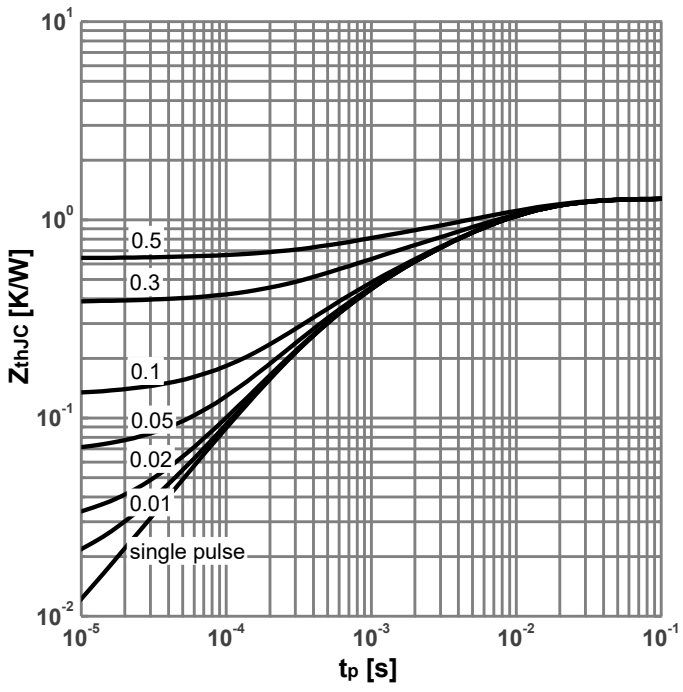
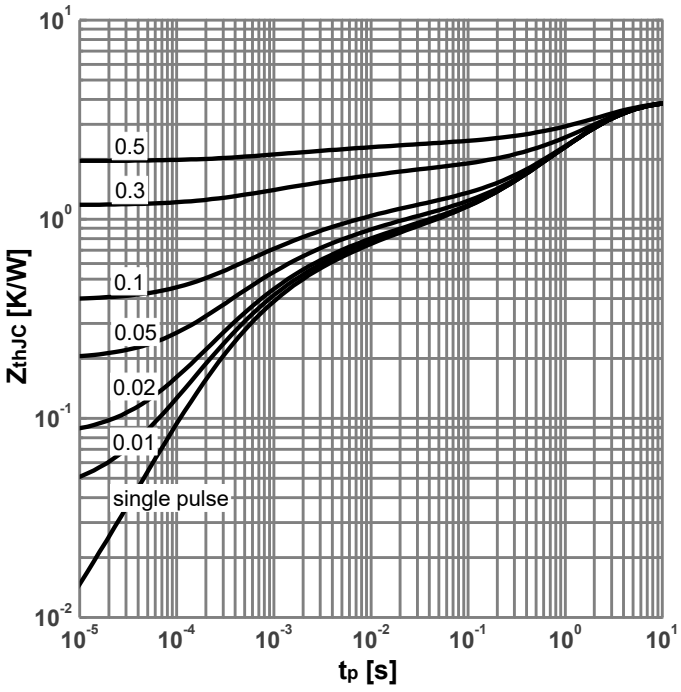
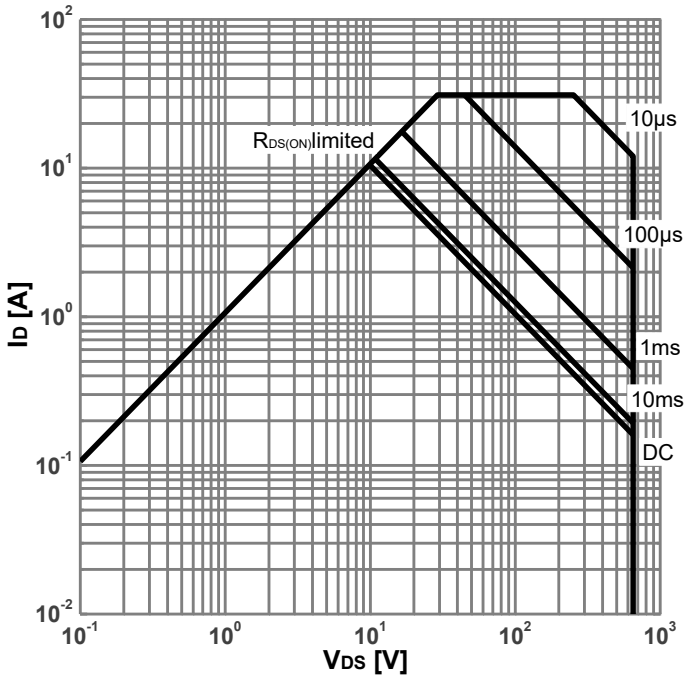
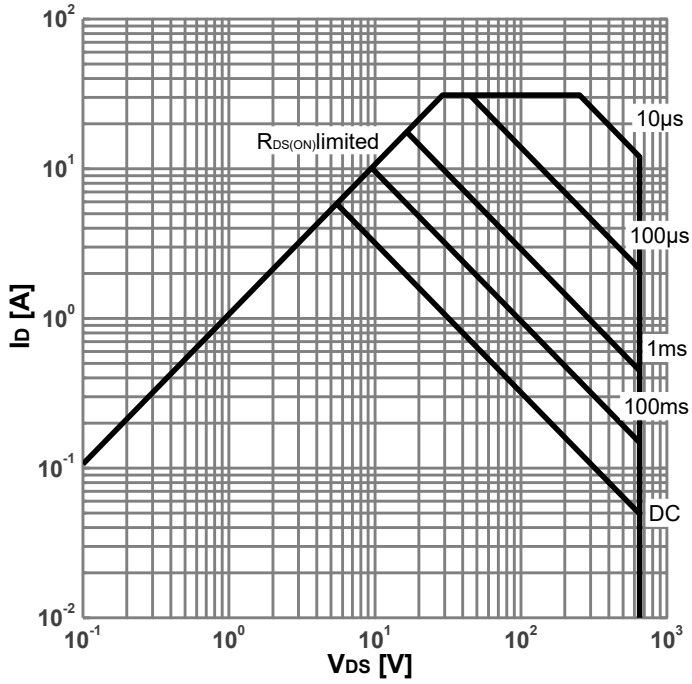
Diagram 3: Max. transient thermal impedance (Non FullPAK)	Diagram 4: Max. transient thermal impedance (FullPAK)
	
Z_{thJC}=f(t_p); parameter: D= t_p/T	Z_{thJC}=f(t_p); parameter: D= t_p/T

Diagram 5: Safe operating area (Non FullPAK)



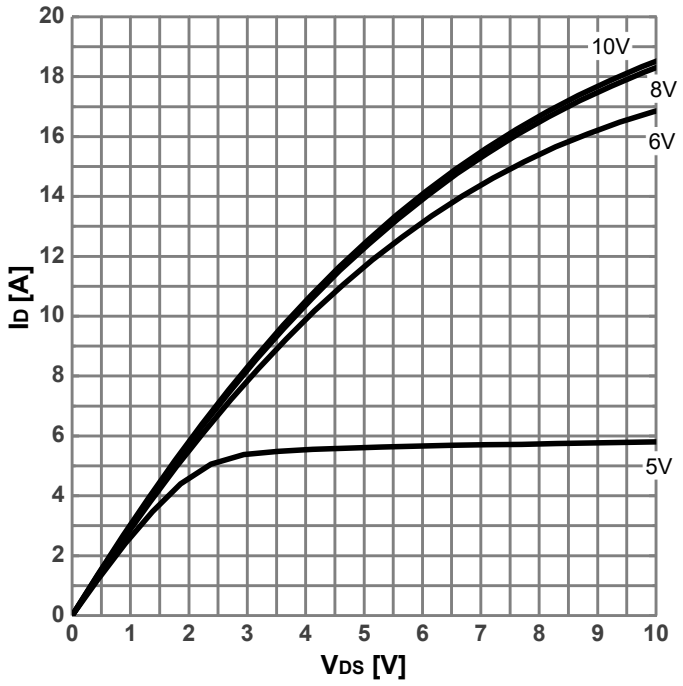
I_D=f(V_{DS}); Tj=25°C; D=0; parameter: t_p

Diagram 6: Safe operating area (FullPAK)



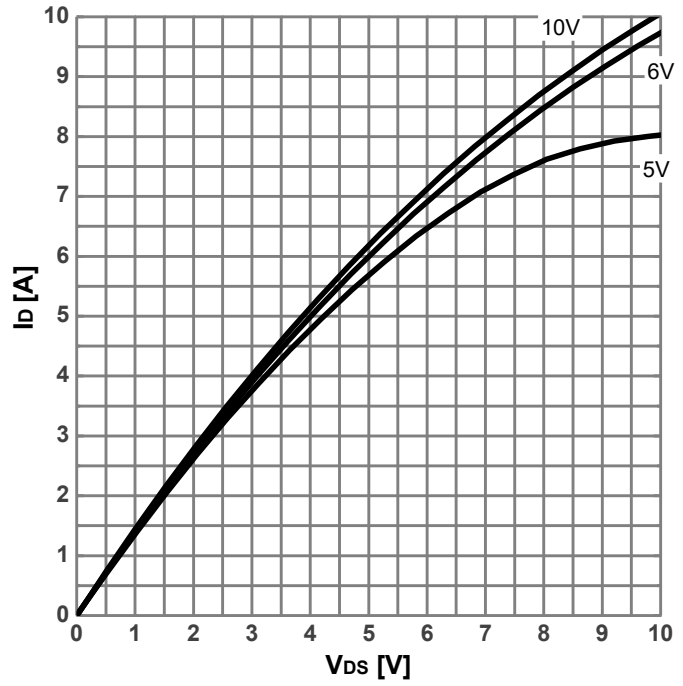
I_D=f(V_{DS}); Tj=25°C; D=0; parameter: t_p

Diagram 7: Typ. output characteristics



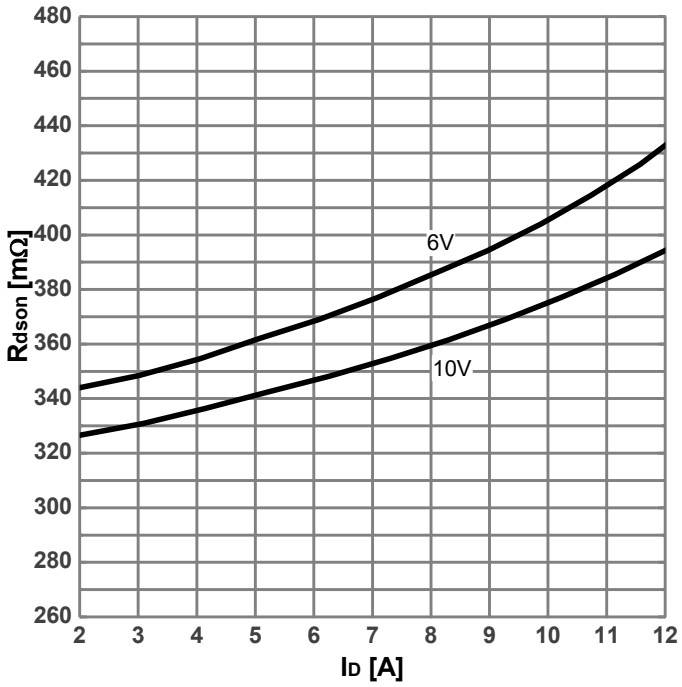
I_D=f(V_{DS}); Tj=25°C; parameter: V_{GS}

Diagram 8: Typ. output characteristics



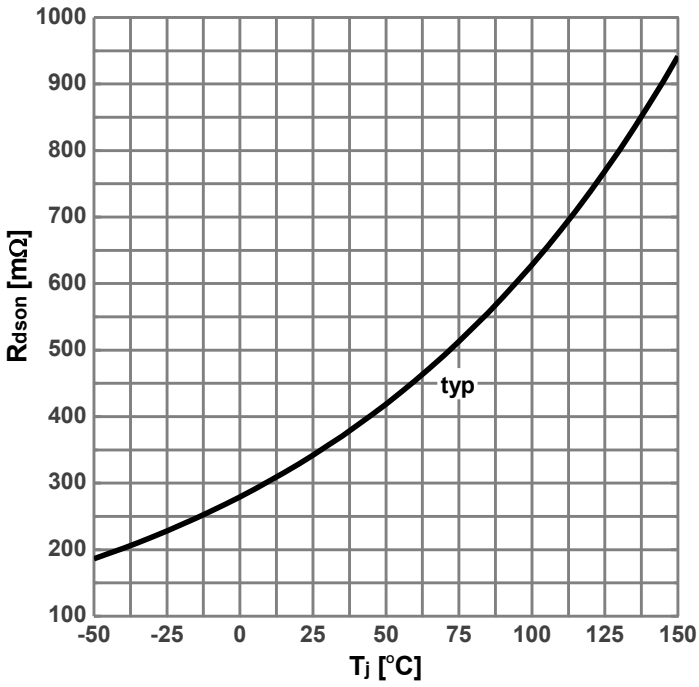
I_D=f(V_{DS}); Tj=125°C; parameter: V_{GS}

Diagram 9: Typ. drain-source on-state resistance



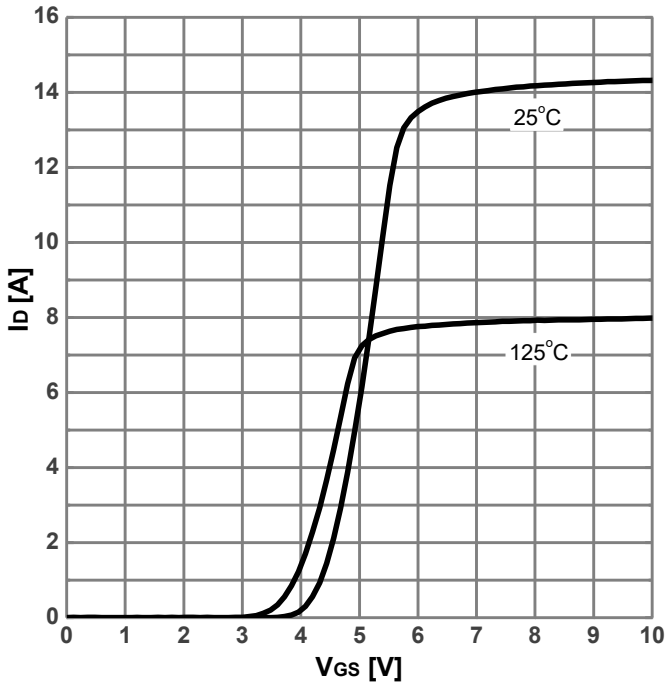
$R_{DS}(on)=f(I_D)$; $Tj=25°C$; parameter: V_{GS}

Diagram 10: drain-source on-state resistance



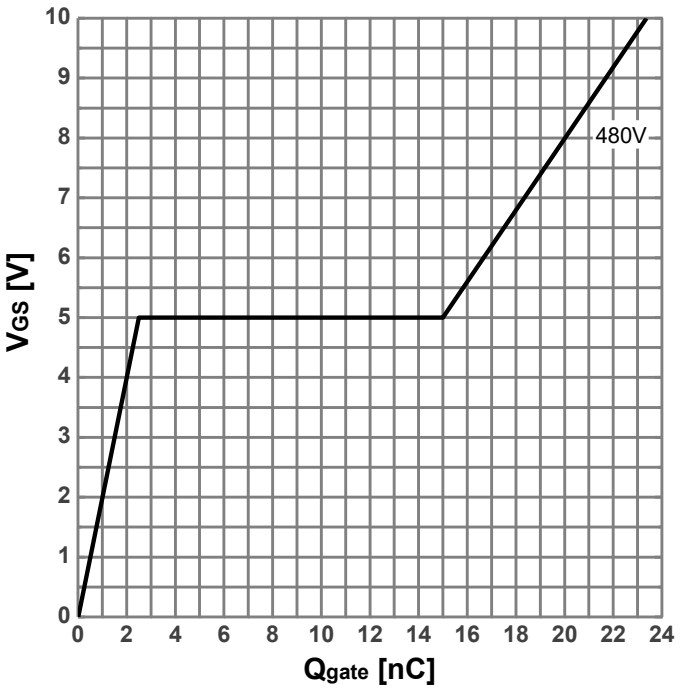
$R_{DS}(on)=f(T_j)$; $I_D=5.5A$; $V_{GS}=10V$

Diagram 11: Typ. transfer characteristics



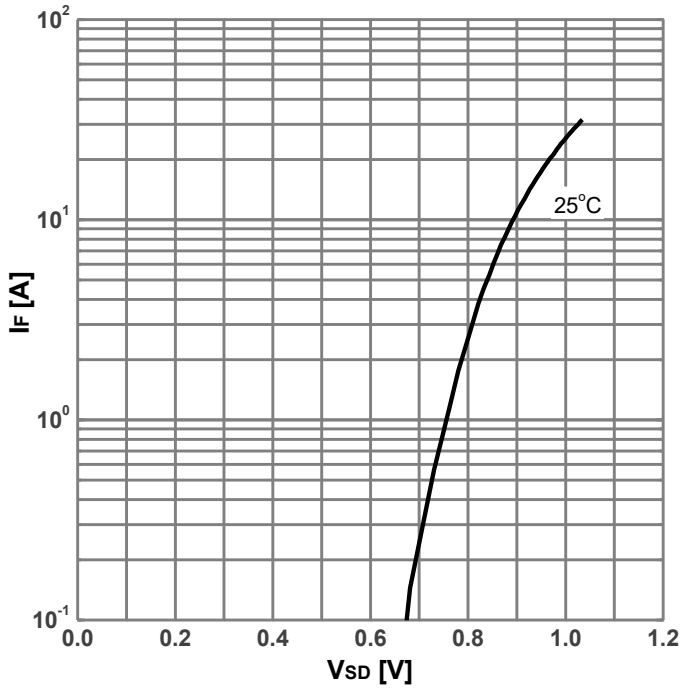
$I_D=f(V_{GS})$; $V_{DS}=20V$; parameter: T_j

Diagram 12: Typ. gate charge



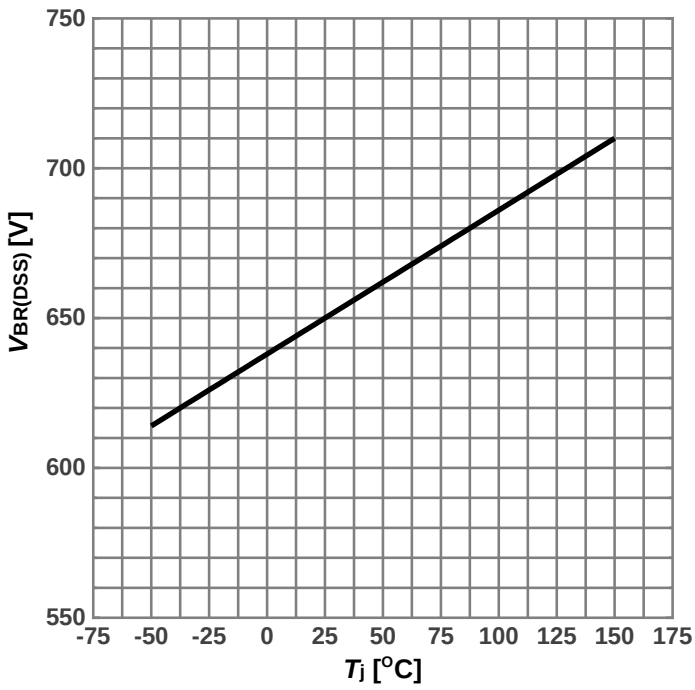
$V_{GS}=f(Q_{gate})$; $I_D=5A$ pulsed; $V_{DS}=480V$

Diagram 13: Forward characteristics of reverse diode



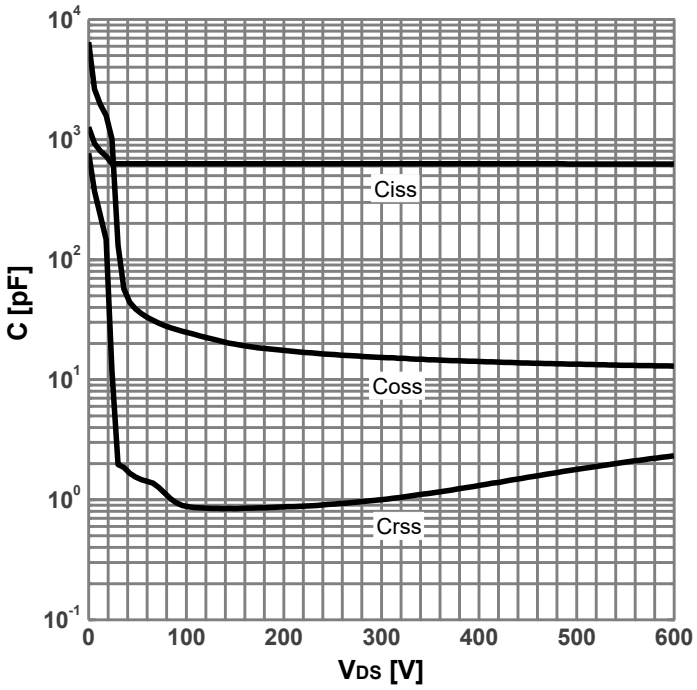
$I_F=f(V_{SD})$; parameter: T_j

Diagram 14: Drain-source breakdown voltage



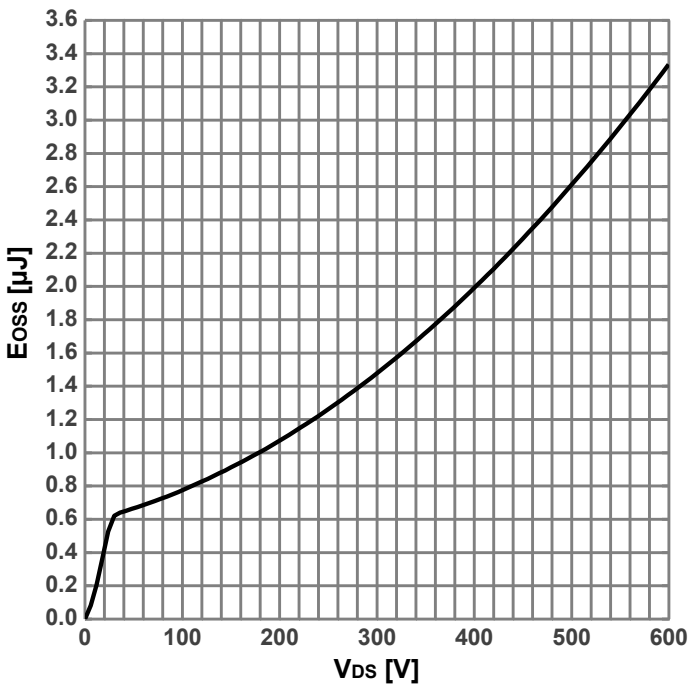
$V_{BR(DSS)}=f(T_j)$; I_D=250µA

Diagram 15: Typ. capacitances



$C=f(V_{DS})$; V_{GS}=0V; f=1MHz

Diagram 16: Typ. Coss stored energy



$E_{OSS}=f(V_{DS})$

6. Test Circuits

Table 8. Diode Characteristics

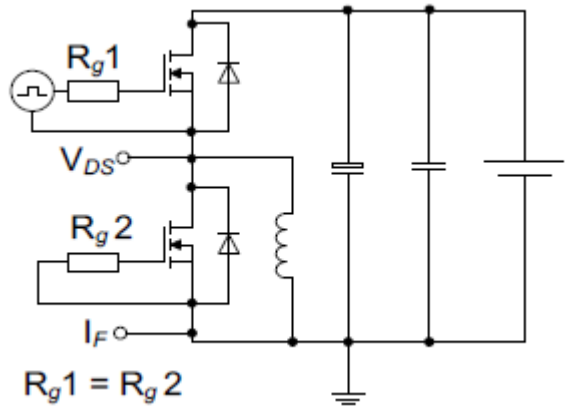
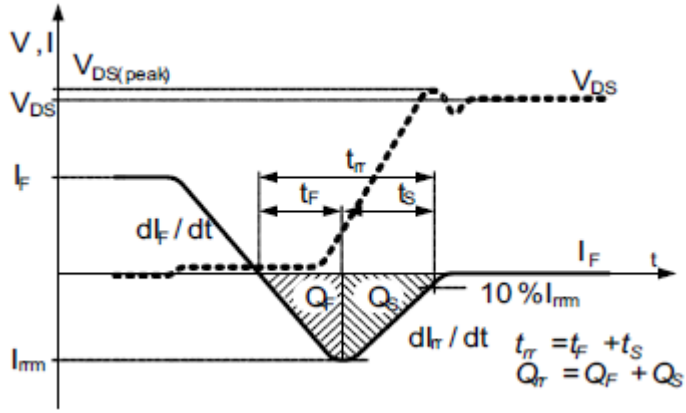
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9. Switching Times

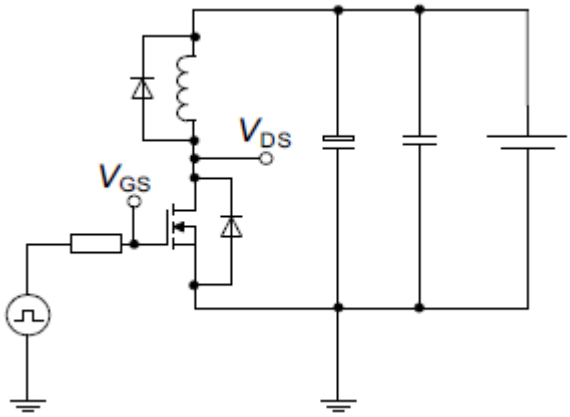
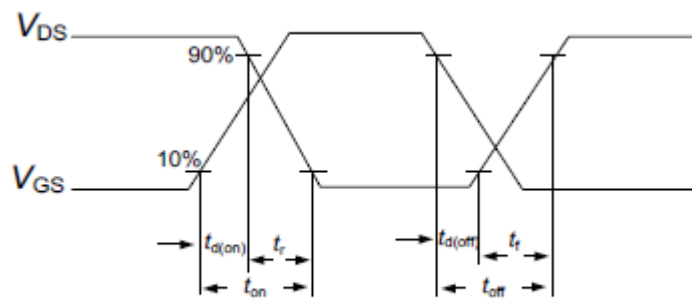
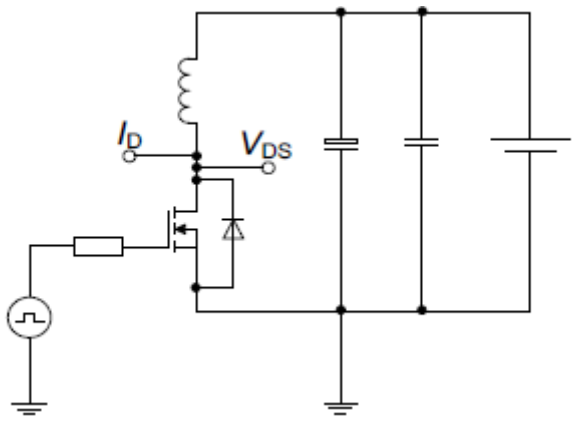
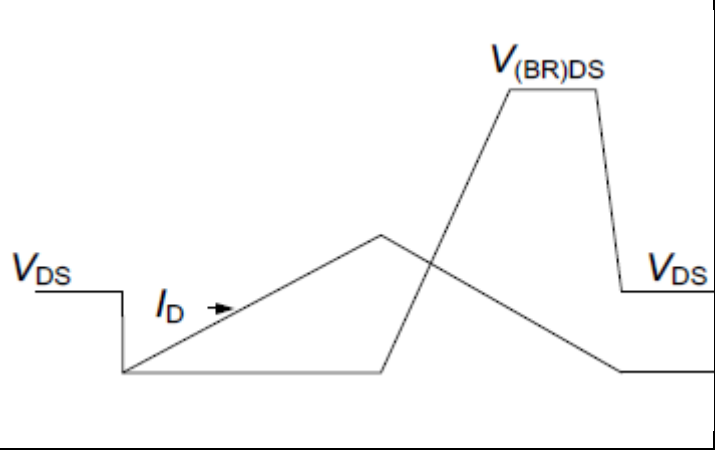
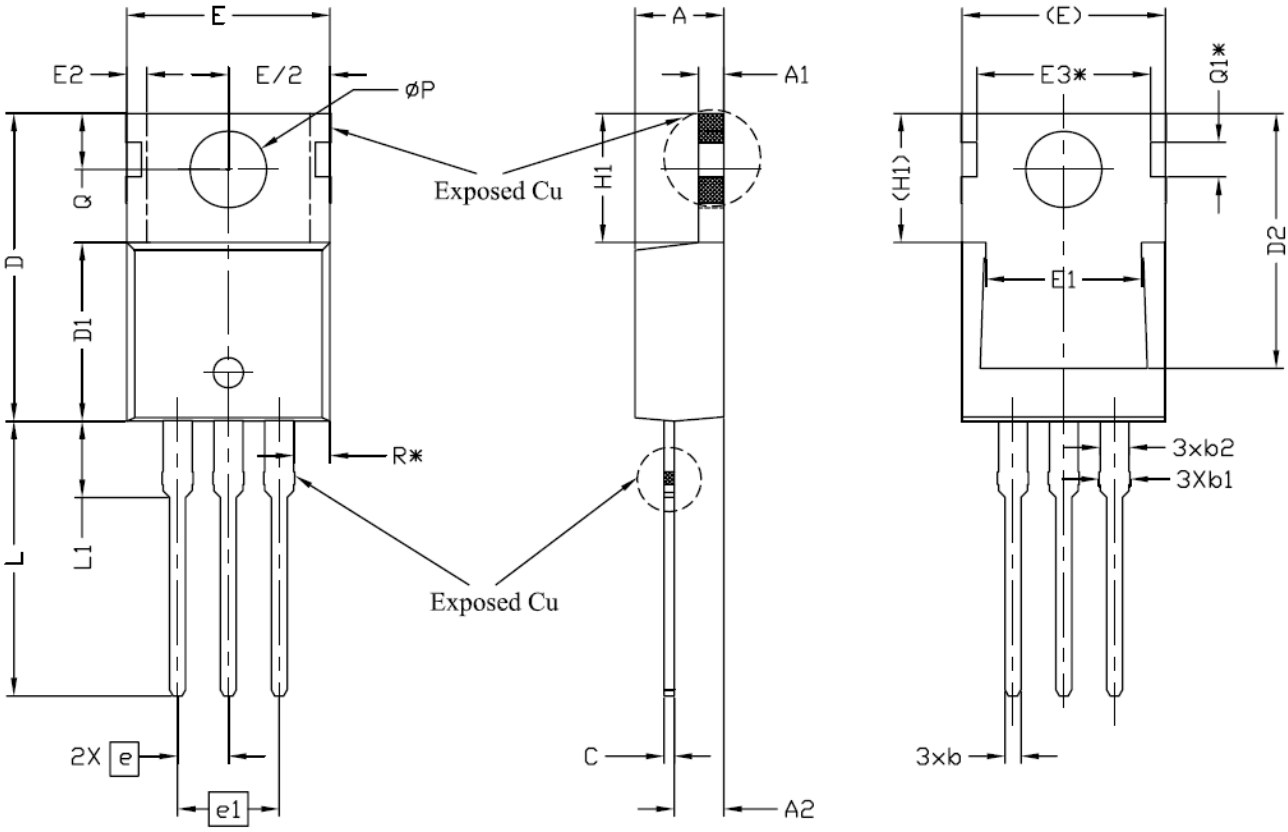
Switching times test circuit for inductive load	Switching times waveform
	

Table 10. Unclamped Inductive Load

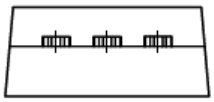
Unclamped inductive load test circuit	Unclamped inductive waveform
	

7. Package Outlines

Figure 1 Outline TO-220 Dimensions in mm

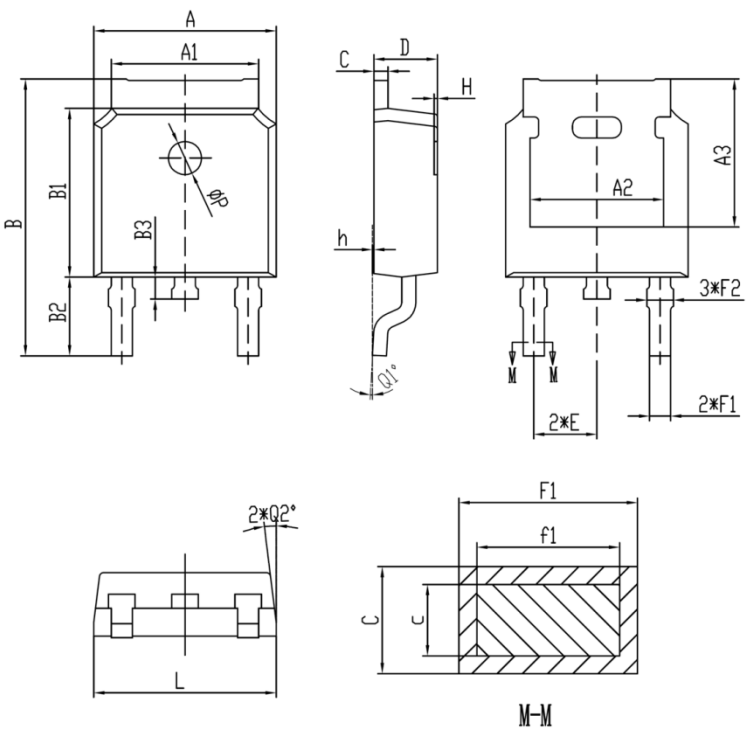


SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.24	4.44	4.64	
A1	1.15	1.27	1.40	
A2	2.30	2.48	2.70	
b	0.70	0.80	0.90	
b1	1.20	1.55	1.75	
b2	1.20	1.45	1.70	
c	0.40	0.50	0.60	
D	14.70	15.37	16.00	4
D1	8.82	8.92	9.02	
D2	12.43	12.73	12.83	5
E	9.96	10.16	10.36	4,5
E1	6.86	7.77	8.89	5
E2	-	-	0.76	6
E3*	8.70REF.			
e	2.54BSC			
e1	5.08BSC			
H1	6.30	6.45	6.60	5,6
L	13.47	13.72	13.97	
L1	3.60	3.80	4.00	
ØP	3.75	3.84	3.93	
Q	2.60	2.80	3.00	
Q1*	1.73REF.			
R*	1.82REF.			



Note:
1. Package Reference: JEDEC TO220, Variation AB.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side. These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
5. Thermal Pad Contour Optional Within Dimensions E, H1, D2 & E1.
6. Dimension E2 & H1 Define A Zone Where Stamping And Singulation Irregularities Are Allowed.
7. "*" is reference .

Figure 2 Outline TO-252 Dimensions in mm

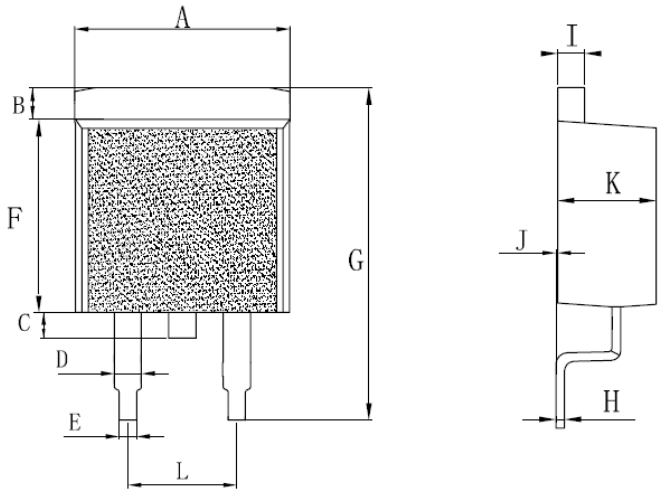


SYMBOL	MIN	NOM	MAX
A	6.50	6.60	6.70
A1	5.16	5.31	5.46
A2		4.83 REF	
A3		5.30 REF	
B	9.77	9.97	10.17
B1	6.00	6.10	6.20
B2	2.60	2.80	3.00
B3	0.70	0.80	0.90
C	0.41	—	0.61
c	0.40	0.50	0.60
D	2.20	2.30	2.40
E	2.186	2.286	2.386
F1	0.67	—	0.87
f1	0.66	0.76	0.86
F2	0.76	0.86	0.96
H	0.00	—	0.30
h	0.00	—	0.15
L	6.50	6.60	6.70
øP	1.10	1.20	1.30
Q1°	0°	—	8°
Q2°	6°	7°	8°

Figure 3 Outline TO-263Dimensions in mm

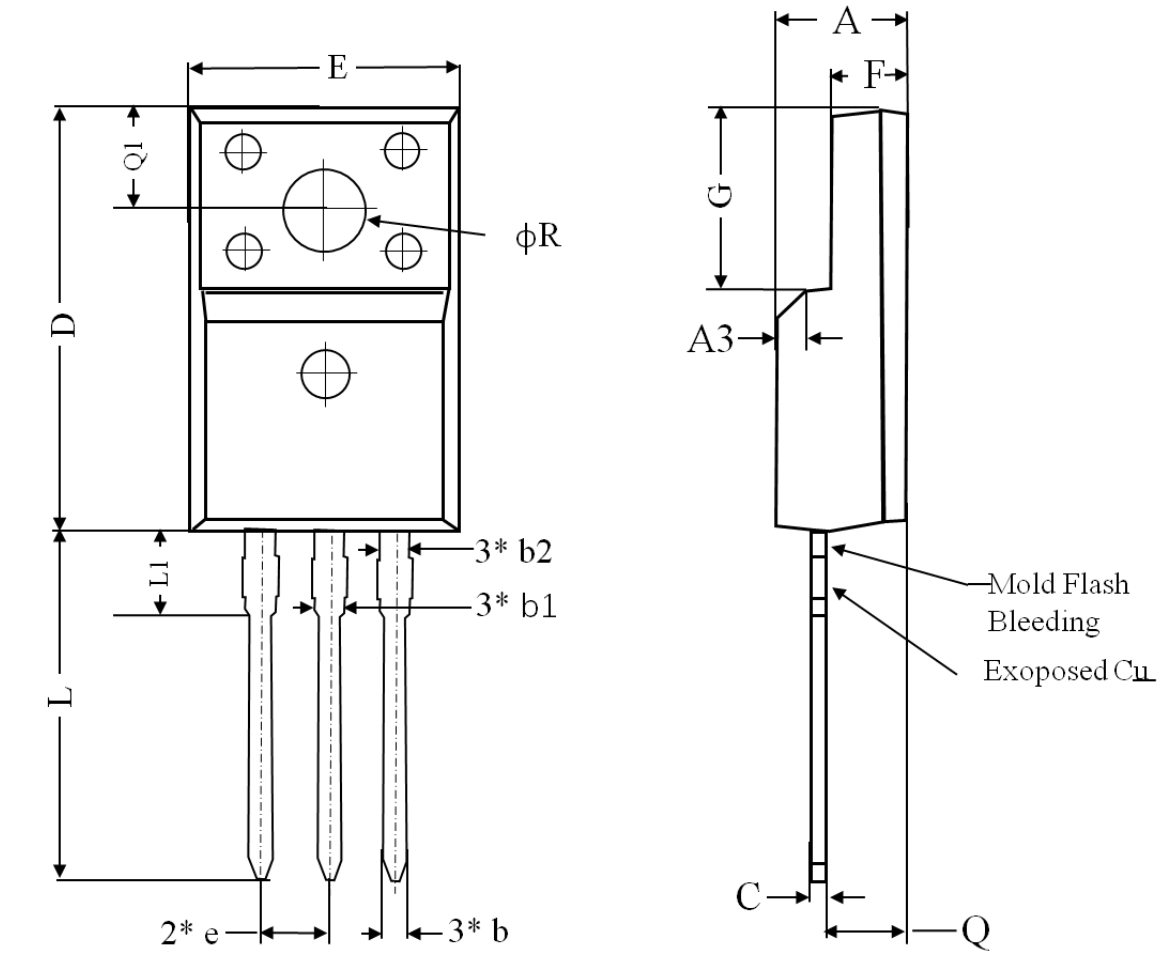
PACKAGE OUTLINE DIMENSIONS

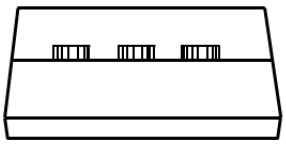
TO-263



DIM.	Unit(mm)		Unit(inch)	
	Min	Max	Min	Max
A	9.7	10.4	0.381	0.409
B	1.31	1.62	0.051	0.063
C	0.65	1.22	0.025	0.048
D	1.15	1.36	0.045	0.053
E	0.62	0.95	0.024	0.037
F	8.75	9.32	0.344	0.366
G	14.75	15.8	0.580	0.622
H	0.32	0.48	0.012	0.018
I	1.18	1.36	0.046	0.053
J	0	0.15	0	0.005
K	4.38	4.86	0.172	0.191
L	4.85	5.23	0.190	0.205

Figure 4 Outline TO-220 FullPAK Dimensions in mm





Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash And Burrs Mold Flash Should Be less Than 6 Mil.

SYMBOL	DIMENSIONS		
	Min.	Nom.	Max.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e		2.54	
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Φr	3.08	3.18	3.28

8. Appendix

CoolSemi Webpage: www.coolsemi.com.

单击下面可查看定价，库存，交付和生命周期等信息

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