CQS03DP16

30V Dual P-CHANNEL MOSFET

Product Summary

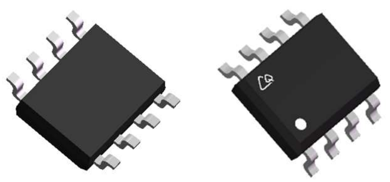
V(BR)DSS	RDS(ON) max	ID max
-30V	<16mΩ @ VGS = -10V	-10A
	<19mΩ @ VGS = -4.5V	

Description and Applications

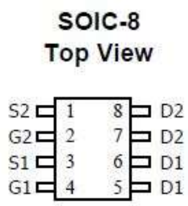
The CQS03DP16 uses advanced trench technology to provide excellent RDS(ON). This device is suitable for use as a load switch or other general applications.

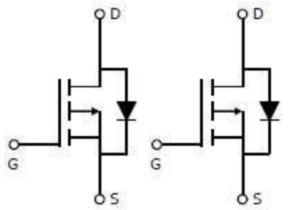
RoHS and Halogen-Free Compliant.

View and Internal Schematic Diagram



SO8





Internal Schematic

Marking Information

SO8

PN=03DP16
F=Fab location
A=Assembly location
Y=Year
W=Week
LT=Lot sequence

Ordering Information

Part Number	Case	Packaging
CQS03DP16	SO8	3,000/Tape & Reel

Maximum Ratings (@TA = +25°C unless otherwise specified.)

Parameters		Symbol	Max	Units
Drain-Source Voltage		VDSS	-30	V
Gate-Source Voltage		VGSS	±20	V
Continuous Drain Current	TA = +25°C TA = +70°C	ID	-10 -7.9	A
Pulsed Drain Current C		IDM	-40	A
Power Dissipation B	TA = +25°C TA = +70°C	PD	2.5 1.6	W
Operating and Storage Temperature Range		TJ, TG	-55 to+150	°C

Thermal Characteristics

Characteristic		Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient A	t ≤ 10s	$R_{\theta JA}$	37	49	°C/W
Maximum Junction-to-Ambient A D	Steady-State		62	78	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	16	24	°C/W

Electrical Characteristics (@TA = +25°C unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BVDSS	Drain-Source Breakdown Voltage	ID=-250µA, VGS=0V	-30			V
IDSS	Zero Gate Voltage Drain Current	VDS=-30V, VGS=0V			-1	µA
		TJ=55℃			-5	
IGSS	Gate-Body leakage current	VDS=0V, VGS= ±20V			±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS ID=-250µA	-1.1	-1.6	-2.1	V
RDS(ON)	Static Drain-Source On-Resistance	VGS=-10V, ID=-9A		11.8	16	mΩ
		TJ=125℃		16.5	23	
		VGS=-4.5V, ID=-9A		15	21.5	mΩ
gFS	Forward Transconductance	VDS=-5V, ID=-9A		39		S
VSD	Diode Forward Voltage	IS=-4.1A,VGS=0V		-0.77	-1	V
IS	Maximum Body-Diode Continuous Current				-3.2	A
DYNAMIC PARAMETERS						
Ciss	Input Capacitance	VGS=0V, VDS=-15V, f=1MHz		1769		pF
Coss	Output Capacitance			234		pF
Crss	Reverse Transfer Capacitance			205		pF
Rg	Gate resistance	VGS=0V, VDS=0V, f=1MHz		4.3	9	Ω
SWITCHING PARAMETERS						
Qg(10V)	Total Gate Charge	VGS=-10V, VDS=-15V, ID=-9A		36.8		nC
Qgs	Gate Source Charge			6.5		nC
Qgd	Gate Drain Charge			7.2		nC
tD(on)	Turn-On Delay Time	VGS=-10V, VDS=-15V, RL=1.67Ω, RGEN=3Ω		8		ns
tr	Turn-On Rise Time			42.8		ns
tD(off)	Turn-Off Delay Time			49.5		ns
tf	Turn-Off Fall Time			63		ns
trr	Body Diode Reverse Recovery Time	IF=-9.0A, dI/dt=100A/µs		15		ns
Qrr	Body Diode Reverse Recovery Charge	IF=-9.0A, dI/dt=100A/µs		5		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on $1in^2$ FR-4 board with 1oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on $1in^2$ FR-4 board with 1oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERIS

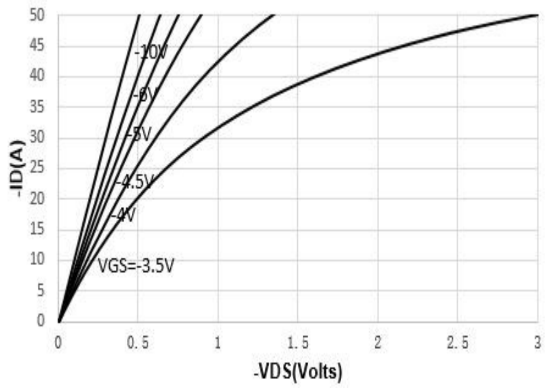


Figure 1： On-Region Characteristics (Note E)

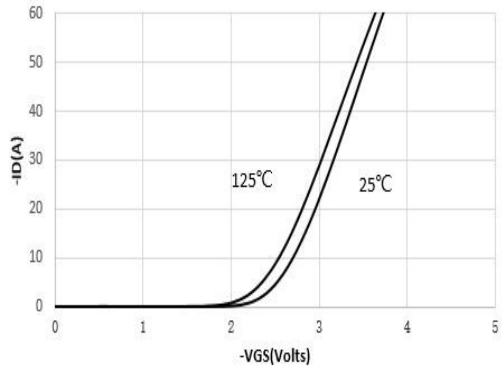


Figure 2 Transfer Characteristics (Note E)

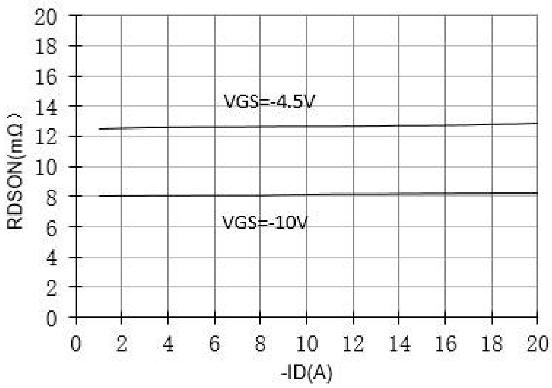


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

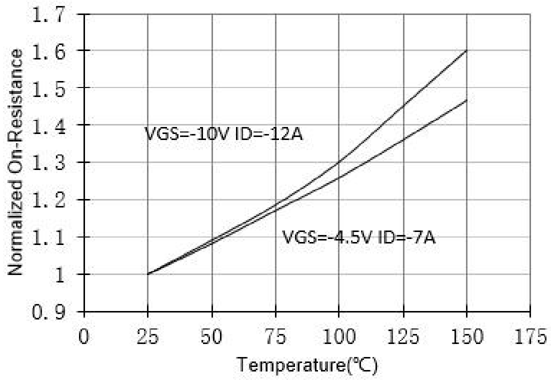


Figure 4: On-Resistance vs. Junction Temperature (Note E)

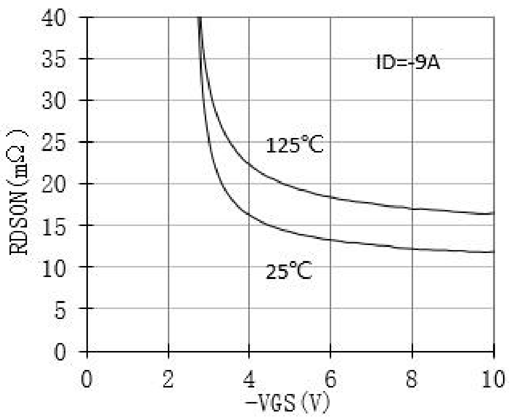


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

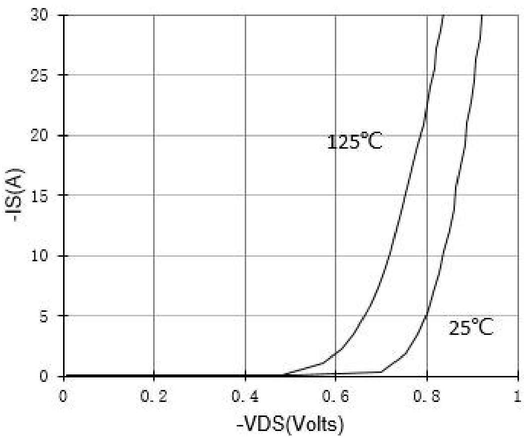


Figure 6: Body-Diode Characteristics (Note E)

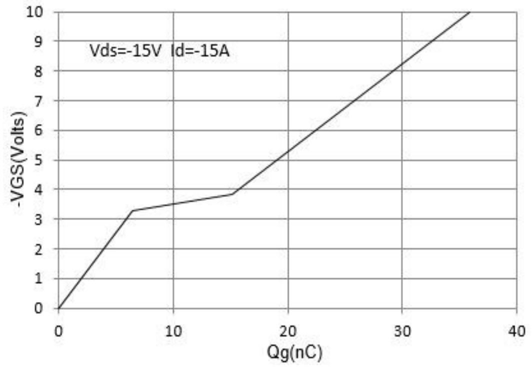


Figure 7: Gate-Charge Characteristics

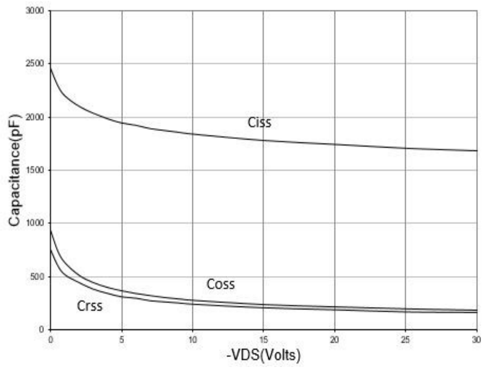


Figure 8: Capacitance Characteristics

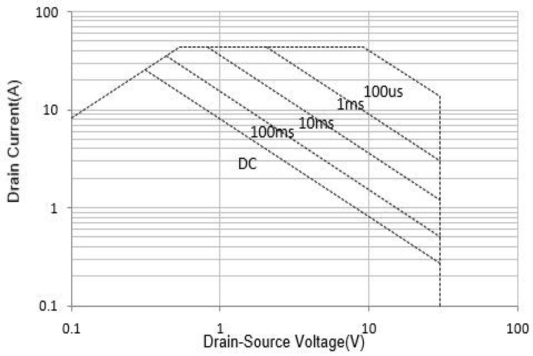


Figure 9: Maximum Forward Biased Safe Operating Area

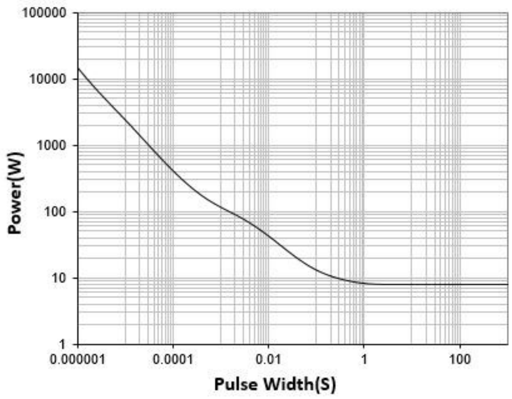


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

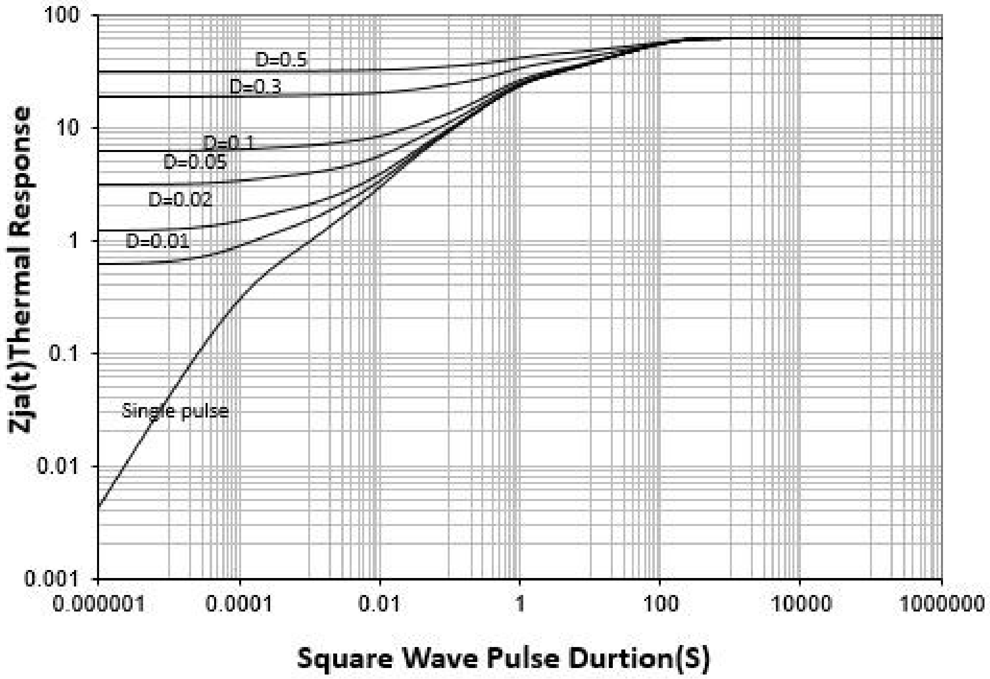


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

单击下面可查看定价，库存，交付和生命周期等信息

[>>CQAOS]