CQAOS 重庆万国

Green Product

CQD609C

40V Complementary Enhance MOSFET

Product Summary

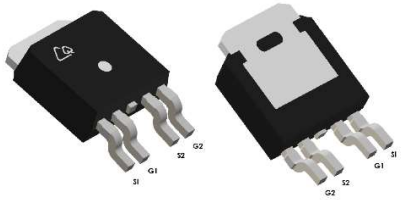
V(BR)DSS		RDS(ON) max	ID
N-MOS	40V	<30mΩ, VGS=10V <40mΩ, VGS=4.5V	12A
P-MOS	-40V	<43mΩ, VGS=-10V <57mΩ, VGS=-4.5V	12A

Description and Applications

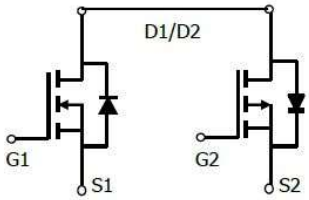
The CQD609C uses trench power MOS technology to provide excellent RDS(ON) and low gate charge. The complementary MOSFETs may be used in H-bridge, inverters and other applications.

RoHS and Halogen-Free Compliant.

View and Internal Schematic Diagram



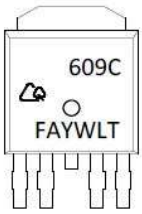
TO252-4L



Internal Schematic

Marking Information

TO252-4L



NOTE:
LOGO - CQAOS
609C- Part number coder
F - Fab location code
A - Assembly location code
Y - Year code
W - Week code
L&T - Assembly lot code

Ordering Information

Part Number	Case	Packaging
CQD609C	TO252-4L	2,500/Tape & Reel

Maximum Ratings (@TA = +25°C unless otherwise specified.)

Parameters		Symbol	Max(N-MOS)	Max(P-MOS)	Units
Drain-Source Voltage		VDS	40	-40	V
Gate-Source Voltage		VGS	20	-20	V
Continuous Drain Current G	TA=25℃ TA=100℃	ID	12 12	-12 -12	A
Pulsed Drain Current C		IDM	40	-30	A
Power Dissipation B	TA=25℃ TA=100℃	PD	18.7 9.3	30 15	W
Operating and Storage Temperature Range		TJ,TSTG	-55 to +175	-55 to +175	℃

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N-MOS Thermal Characteristics

Characteristic		Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	16.7	25	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		40	50	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta Jc}$	6.7	8	°C/W

N-MOS Electrical Characteristics (@TA = +25°C unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	ID=250μA, VGS=0V	40			V
IDSS	Zero Gate Voltage Drain Current	VDS=40V, VGS=0V			1	μA
		TJ=55℃			5	
I_{GSS}	Gate-Body leakage current	VDS=0V, VGS= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	VDS=VGS ID=250μA	1	1.7	2.2	V
RDS(ON)	Static Drain-Source On-Resistance	VGS=10V, ID=12A		24.5	30	mΩ
		TJ=125℃		40	46	
		VGS=4.5V, ID=8A		30	40	mΩ
gFS	Forward Trans conductance	VDS=5V, ID=12A		25.5		S
V_{SD}	Diode Forward Voltage	IS=1A,VGS=0V		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				12	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	VGS=0V, VDS=15V, f=1MHz		535		pF
C_{oss}	Output Capacitance			46		pF
C_{rss}	Reverse Transfer Capacitance			36		pF
R_g	Gate resistance	VGS=0V, VDS=0V, f=1MHz	0.4	1.4	3.5	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	VGS=10V, VDS=20V, ID=12A		11.3		nC
Q_{gs}	Gate Source Charge			3		nC
Q_{gd}	Gate Drain Charge			1.7		nC
$t_{D(on)}$	Turn-On Delay Time	VGS=10V, VDS=20V, RL=1.6Ω, RGEN=3Ω		4.4		ns
t_r	Turn-On Rise Time			35		ns
$t_{D(off)}$	Turn-Off Delay Time			9.6		ns
t_f	Turn-Off Fall Time			23.6		ns
t_{rr}	Body Diode Reverse Recovery Time	IF=12A, dI/dt=100A/μs		6		ns
Q_{rr}	Body Diode Reverse Recovery Charge	IF=12A, dI/dt=100A/μs		2		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 1oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta Jc}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted on 1in^2 FR-4 board with 1oz. Copper, in a still air environment with TA=25℃

G. The maximum current rating is package limited

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P-MOS Thermal Characteristics

Characteristic		Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient A	t ≤ 10s	$R_{\theta JA}$	16.8	25	°C/W
Maximum Junction-to-Ambient A D	Steady-State		43	53	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	3.3	5	°C/W

P-MOS Electrical Characteristics (@T_A = +25°C unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	-40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=−40V, V_{GS}=0V			-1	μA
		TJ=55℃			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250μA	-1	-1.5	-2.1	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=−10V, I_D=-12A		34	43	mΩ
		TJ=125℃		51	64	
		V_{GS}=−4.5V, I_D=-8A		42	57	mΩ
g_{FS}	Forward Trans conductance	V_{DS}=-5V, I_D=-12A		23		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.76	-1	V
I_S	Maximum Body-Diode Continuous Current				-12	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-20V, f=1MHz		1048		pF
C_{oss}	Output Capacitance			93		pF
C_{rss}	Reverse Transfer Capacitance			85		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V,	3.5	10	16.5	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-20V, I_D=-12A		24		nC
Q_{gs}	Gate Source Charge			5.4		nC
Q_{gd}	Gate Drain Charge			4.1		nC
$t_{D(on)}$	Turn-On Delay Time	V_{GS}=-10V, V_{DS}=-20V, RL=1.4Ω, R_{GEN}=3Ω		8.7		ns
t_r	Turn-On Rise Time			62		ns
$t_{D(off)}$	Turn-Off Delay Time			60		ns
t_f	Turn-Off Fall Time			78		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-12A, dI/dt=100A/μs		27		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-12A, dI/dt=100A/μs		6.5		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 1oz Copper, in a still air environment with T_A =25°C. The value in any given in any application depends on the user's specific board design

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta Jc}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted on 1in² FR-4 board with 1oz. Copper, in a still air environment with TA=25℃

G. The maximum current rating is package limited

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N-MOS TYPICAL ELECTRICAL AND THERMAL CHARACTERIS

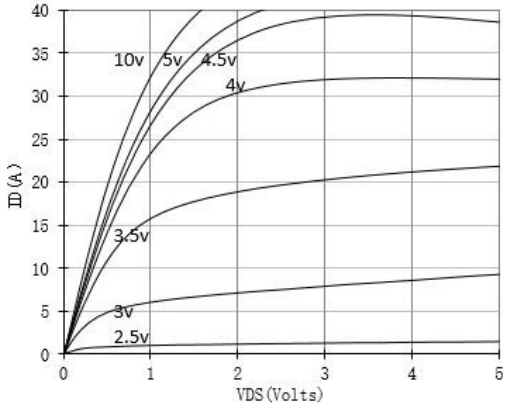

Figure 1：On-Region Characteristics (Note E)

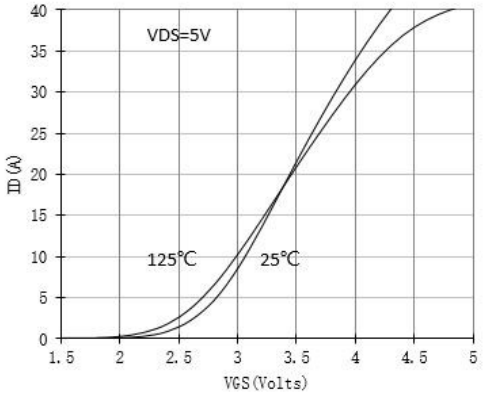

Figure 2 Transfer Characteristics (Note E)

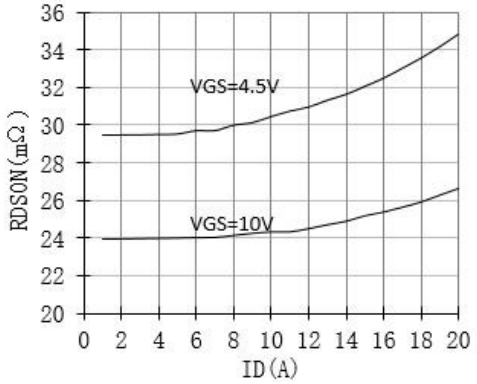

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

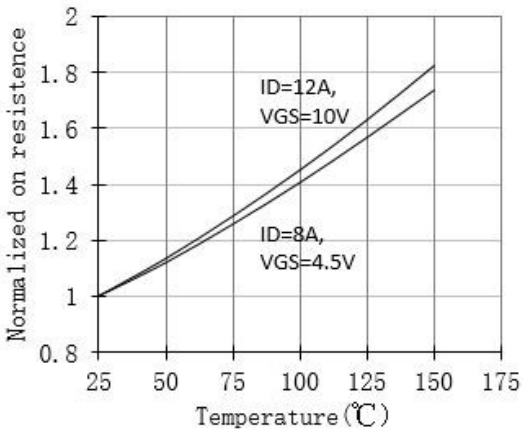

Figure 4: On-Resistance vs. Junction Temperature (Note E)

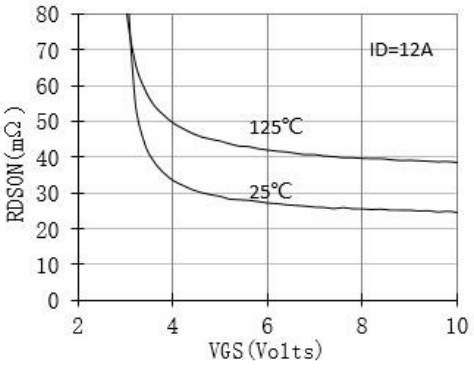

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

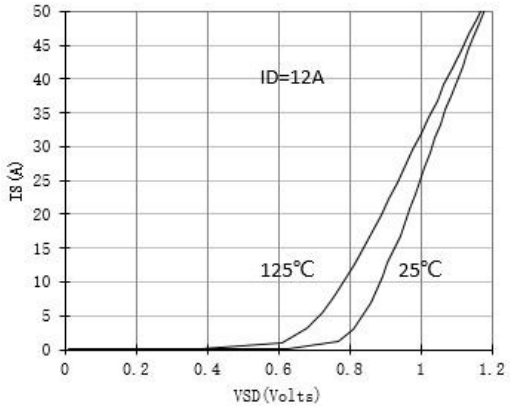

Figure 6: Body-Diode Characteristics (Note E)

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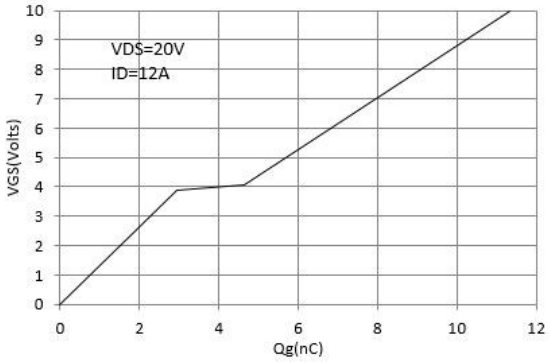

Figure 7: Gate-Charge Characteristics

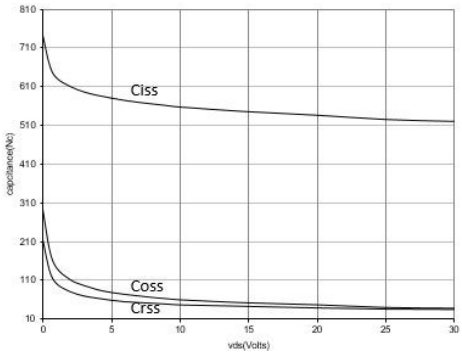

Figure 8: Capacitance Characteristics

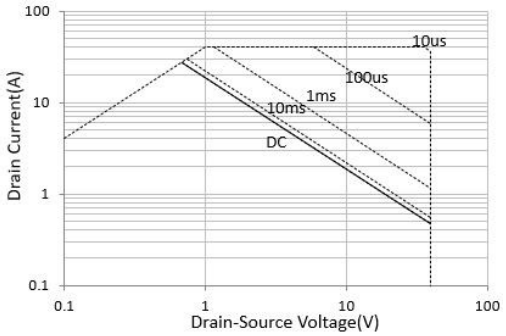

Figure 9: Maximum Forward Biased Safe Operating Area

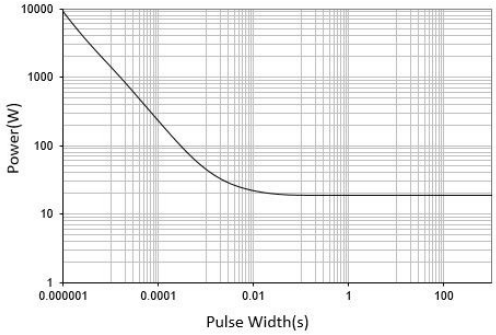

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

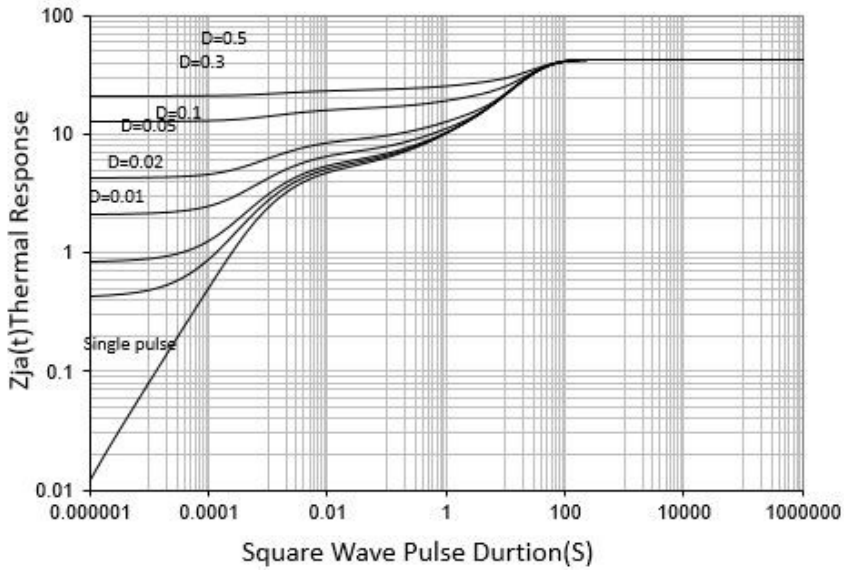

Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

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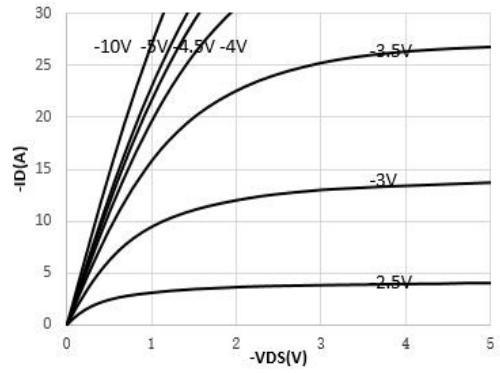
P-MOS TYPICAL ELECTRICAL AND THERMAL CHARACTERIS



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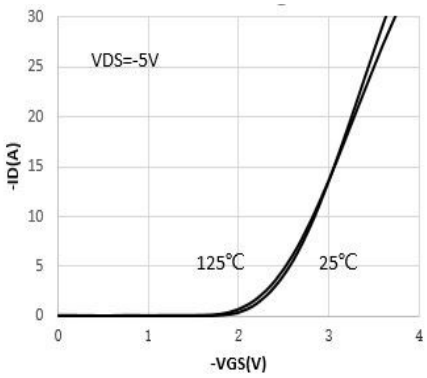


Figure 2 Transfer Characteristics (Note E)

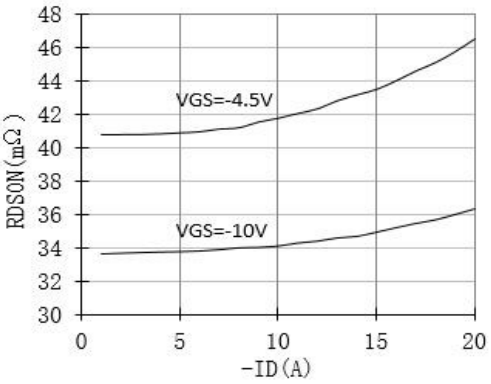
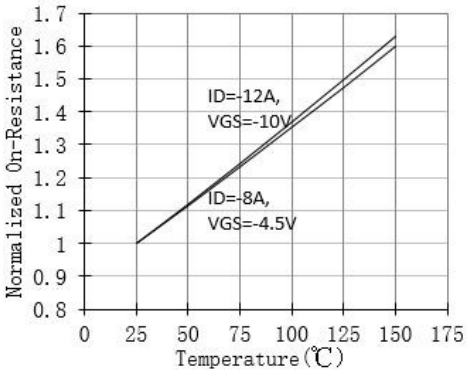


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)



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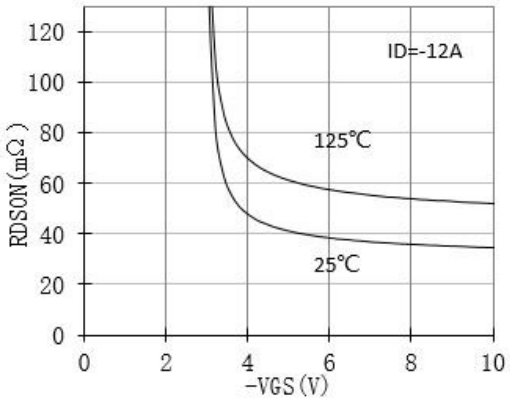

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

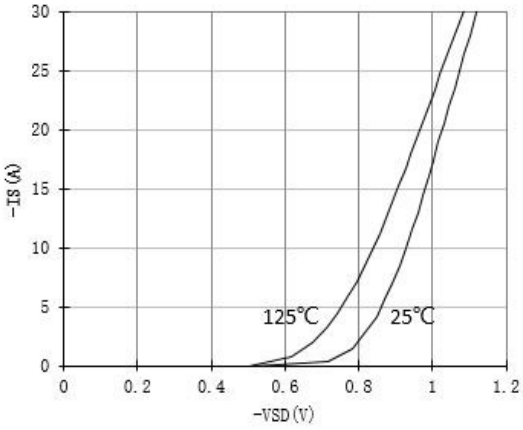

Figure 6: Body-Diode Characteristics (Note E)

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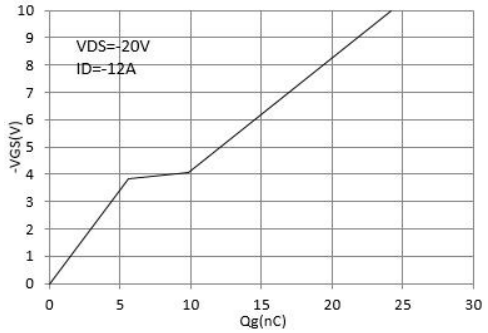

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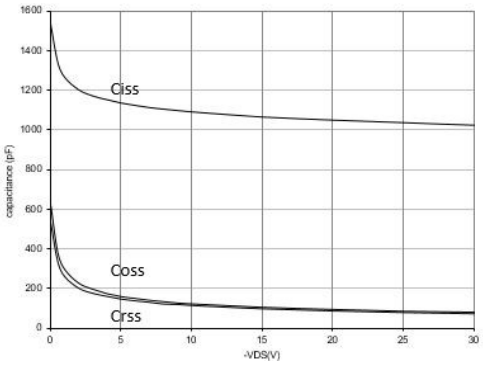

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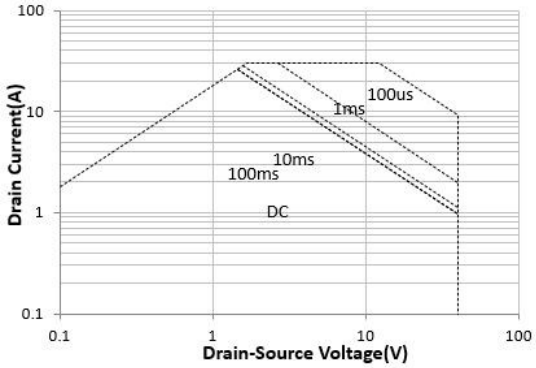

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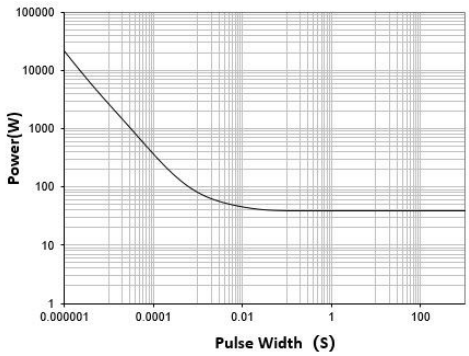

Figure 10: Single Pulse Power Rating Junction-to-Case

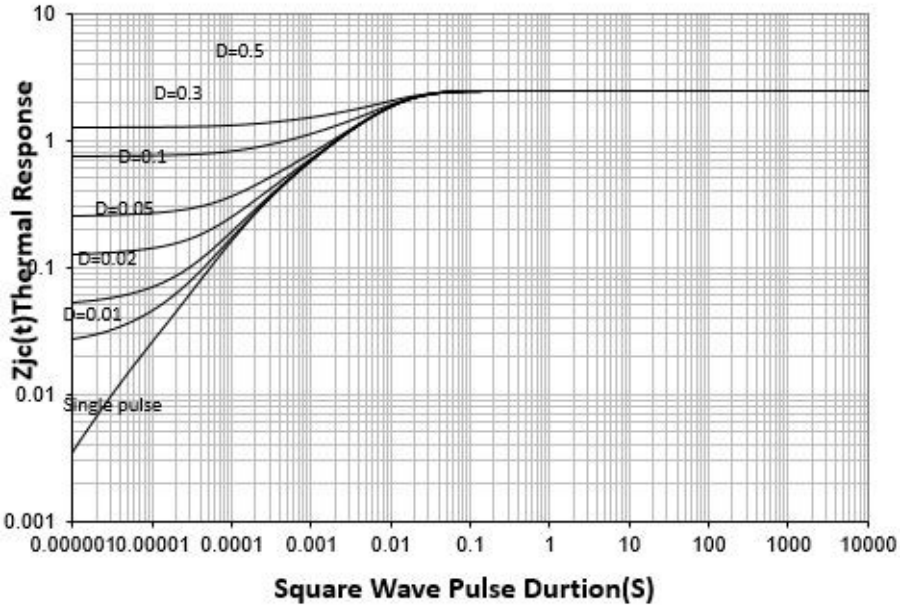

Figure 11: Normalized Maximum Transient Thermal Impedance

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