CQD03N3R5

30V N-CHANNEL MOSFET

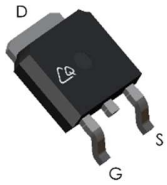
Product Summary

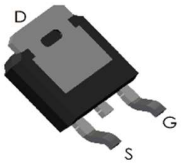
V(BR)DSS	RDS(ON) max	ID max
30V	<5.3mΩ @ VGS = 10V	54A
	<6.4mΩ @ VGS = 4.5V	

Description and Applications

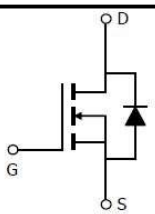
- Trench Power MOSFET technology
- Low RDSON and Low Gate Charge
- RoHS and Halogen-Free Complaint
- Low Side Switch in CPU Core Power Conversion
- 100% UIS Tested
- 100% Rg Tested

View and Internal Schematic Diagram





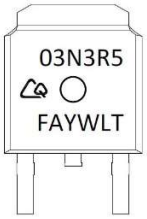
TO252 DPAK



Internal Schematic

Marking Information

TO252 DPAK



NOTE:
LOGO - CQAOS
03N3R5 - Part number coder
F - Fab location code
A - Assembly location code
Y - Year code
W - Week code
L&T - Assembly lot code

Ordering Information

Part Number	Case	Packaging
CQD03N3R5	DPAK	2,500/Tape & Reel

Maximum Ratings (@TA = +25°C unless otherwise specified.)

Parameters		Symbol	Max	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	20	V
Continuous Drain Current [G]	T_C = +25°C T_C= +100°C	I_D	54 54	A
Pulsed Drain Current [C]		I_{DM}	200	A
Avalanche Current [C]		I_{AS}	36	A
Avalanche Energy [C]	L=0.1mH	E_{AS}	65	mJ
Power Dissipation [B]	T_C = +25°C T_C = +100°C	P_D	60 30	W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to+175	°C

Thermal Characteristics

Characteristic		Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	14.2	20	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		40	50	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	2.1	2.5	°C/W

Electrical Characteristics (@TA = +25°C unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	1.1	1.5	1.9	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		4.3	5.3	mΩ
		T_J=125°C		6.2		
		V_{GS}=4.5V, I_D=20A		5.2	6.4	mΩ
g_{FS}	Forward Trans conductance	V_{DS}=5V, I_D=20A		80		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.73	1	V
I_S	Maximum Body-Diode Continuous Current				54	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		2382		pF
C_{oss}	Output Capacitance			275		pF
C_{rss}	Reverse Transfer Capacitance			185		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.5	1.85	3.5	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=15V, I_D=20A		22.5		nC
Q_{gs}	Gate Source Charge			8		nC
Q_{gd}	Gate Drain Charge			8.6		nC
$t_{D(on)}$	Turn-On Delay Time	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		7.6		ns
t_r	Turn-On Rise Time			62		ns
$t_{D(off)}$	Turn-Off Delay Time			40		ns
t_f	Turn-Off Fall Time			65.7		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=100A/μs		9.3		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=100A/μs		2		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 1oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using ≤ 10s junction-to-case thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted on 1in^2 FR-4 board with 1oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating

G. The maximum current rating is limited by the package.

TYPICAL ELECTRICAL AND THERMAL CHARACTERIS

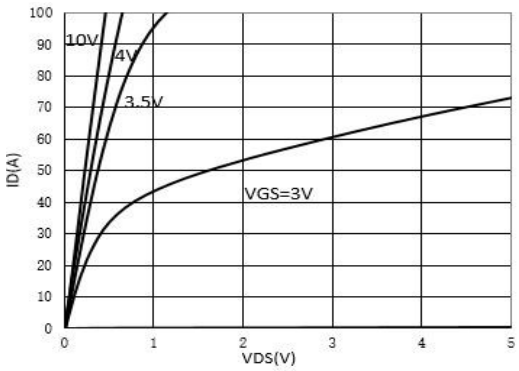


Figure1: On-Region Characteristics (Note E)

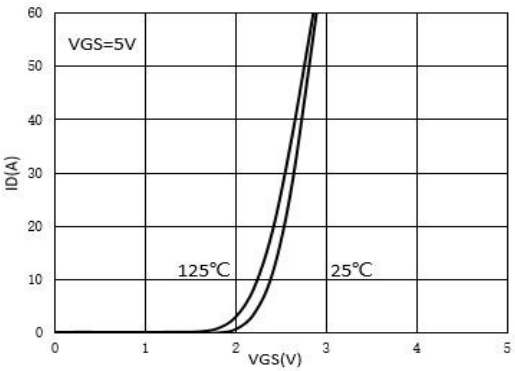


Figure 2: Transfer Characteristics(Note E)

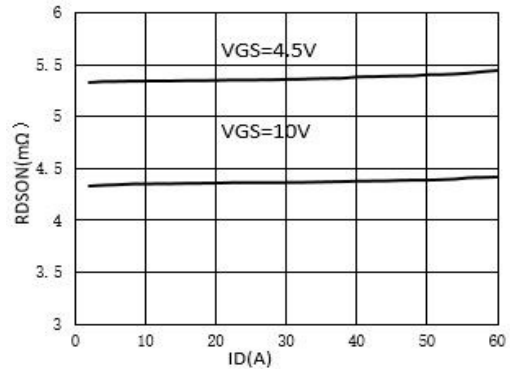


Figure3: On-Resistance vs. Drain Current and Gate Voltage(Note E)

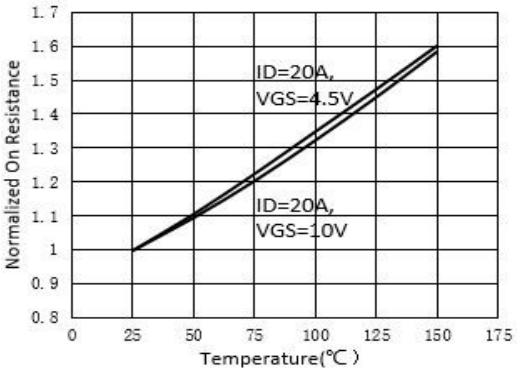


Figure 4: On-Resistance vs. Junction Temperature (Note E)

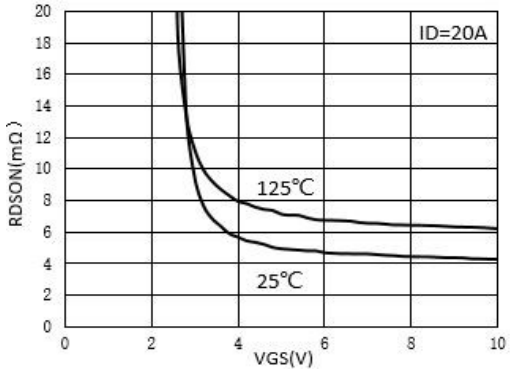


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

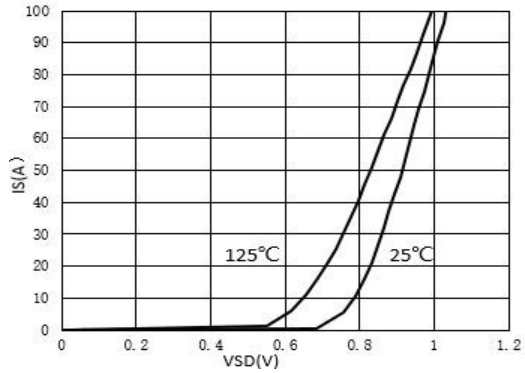


Figure 6:Body-Diode Characteristics(Note E)

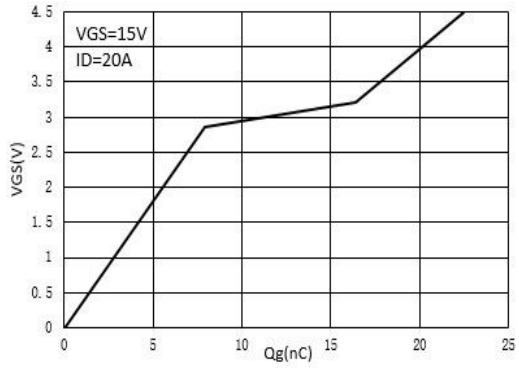


Figure 7:Gate-Charge Characteristics

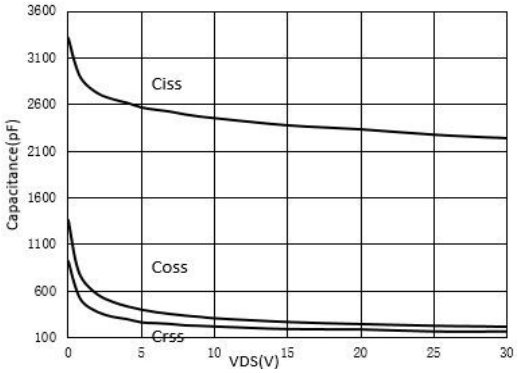


Figure 8:Capacitance Characteristics

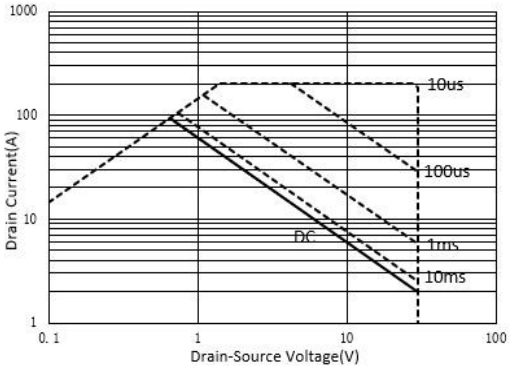


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

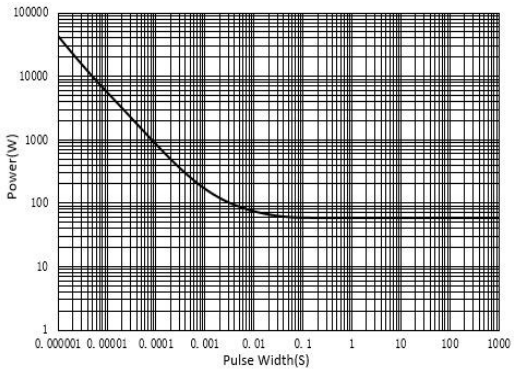


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

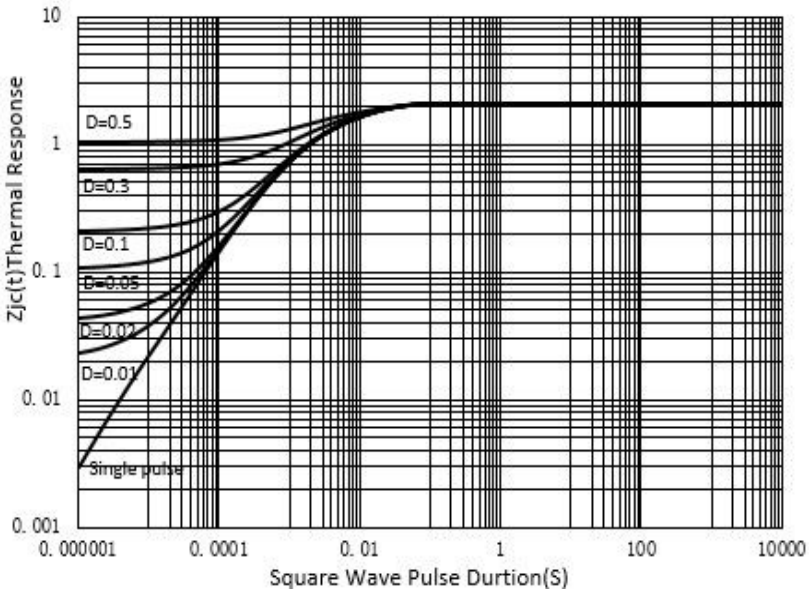
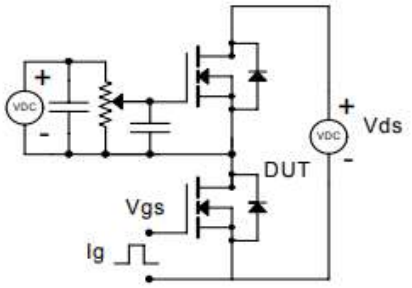
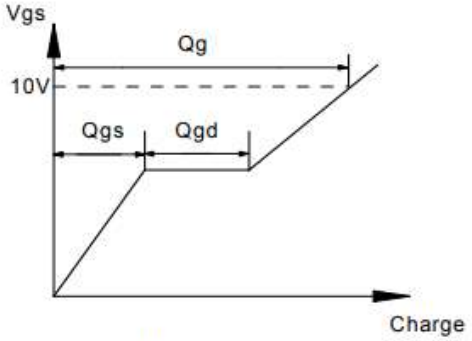


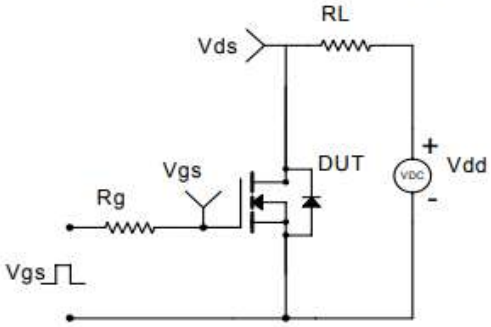
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

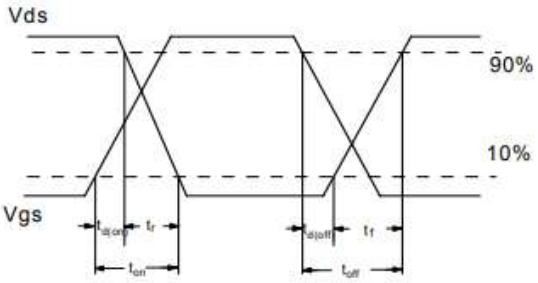
Gate Charge Test Circuit & Waveform



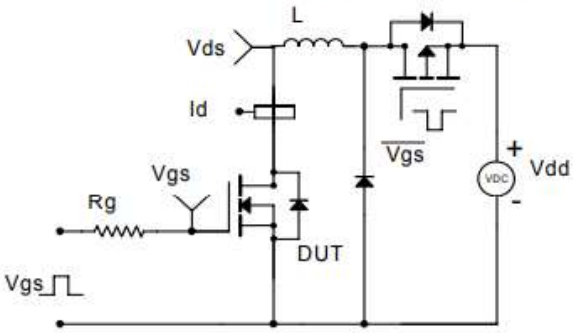


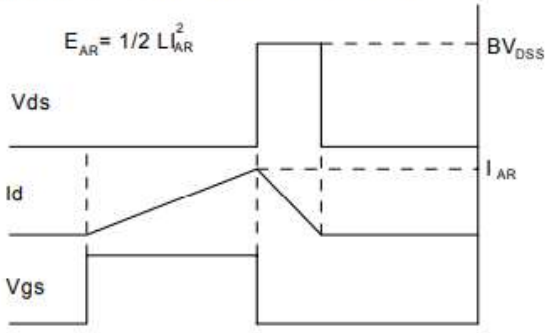
Resistive Switching Test Circuit & Waveforms



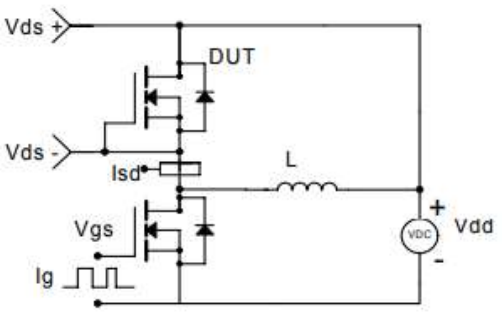


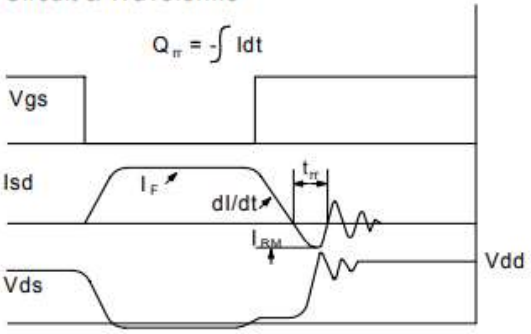
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms





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