

# 400G MACsec Gearbox + Retimer



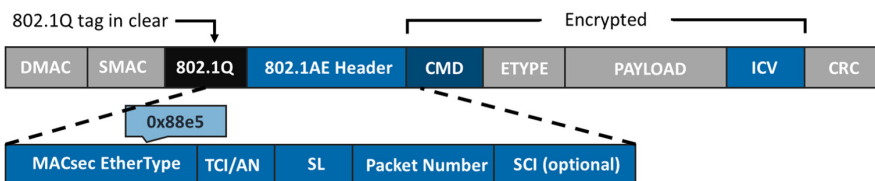
56G SerDes

## B52 MACsec Supports Gearbox and Retimer

CreDO is a leading provider of high performance/low power semiconductor solutions for the data center, enterprise networking and high performance computing markets. Our innovative Serializer-Deserializer (SerDes) technology delivers the bandwidth, scalability and end-to-end signal integrity needed to meet the demands of advanced networks up to 800G with single-lane 28G, 56G, or 112G connectivity.

CreDO's purpose-built approach to SerDes design enables our products to be built on mature process technology, providing our customers with a competitive edge.

The **CMS42550** MACsec is pin compatible with the **CMX42550** Sparrow 400G Gearbox. It is suitable for both backplane and front panel applications including cloud- scale switches, high density routing platforms and advanced server NIC cards.



### Product Family

#### CMS42550

400G Bi-directional LR Gearbox with MACsec  
 8x56G PAM4  $\Rightarrow$  16x28G NRZ Gearbox  
 8x56G PAM4  $\Rightarrow$  8x56G PAM4 Retimer  
 23nm x 23nm with 0.8mm ball pitch

Pin compatible to **CMX42550** Sparrow 400G Gearbox

### Key Parameters

<b>Channels</b> (bidirectional)	8 / 16
<b>MAC Rates</b> (bidirectional)	25-28 : 50-58 Gbps
<b>Insertion Loss</b>	30dB
<b>Output Voltage</b> (programmable)	100-1,000 mVp-p
<b>Power Supplies</b>	1.8V +/- 5% 0.9V +/- 5%
<b>Operating Temp</b>	-10 to 85 °C
<b>Registration Interface</b>	MDIO / I <sup>2</sup> C
<b>Process Node</b>	TSMC 28nm

## Key Features

### Gearbox with MACsec Mode

- ☑ SERDES ☑ FEC ☑ PCS ☑ MAC ☑ MACsec
- 1x400G (8x56G to 8x56G)
- 2x200G (4x56G to 4x56G)
- 4x100G (2x56G to 4x28G)
- 3x100G (4x28G to 4x28G)
- 8x50G (1x56G to 1x56G)
- 12x25G (1x28G to 1x26G)
- 12x10G (1x10G to 1x10G)

### Bit-MUX with MACsec Mode

- ☒ SERDES ☒ FEC ☑ PCS ☑ MAC ☑ MACsec
- Any one lane to 2 lanes bit mux mode
- Specifically 3x40G (2x20G to 4x10G)

### Gearbox Only Mode

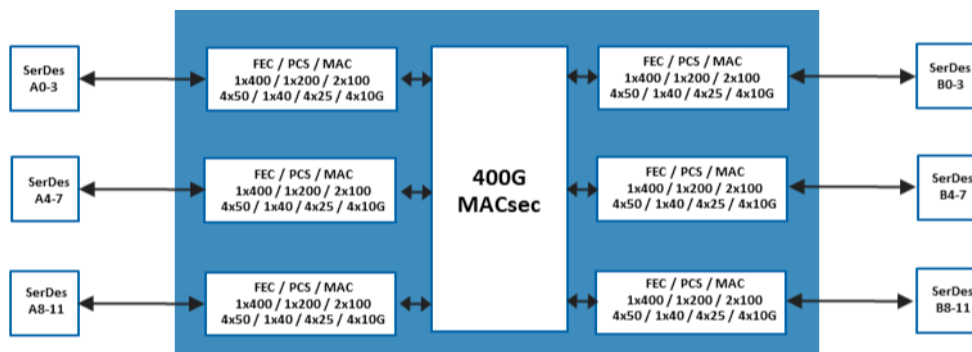
- ☒ SERDES ☑ FEC ☑ PCS ☑ MAC ☒ MACsec
- 4x100G (2x56G to 4x28G)
- 8x50G (1x56G to 2x28G)
- FEC trans-coding

- Any PAM4 (up to 56G) and NRZ (up to 28G) retimer modes (no FEC+PCS+MAC+MACsec)
- Auto-negotiation support for all IEEE defined modes and 50G/25G consortium modes
- Link training support for various lane modulation and speed (10G, 28G NRZ, 56G PAM4)
- All FEC types (KP FEC, KR FEC, BaseR FEC or no FEC)
- Proven and certified MACsec engine
- Standard MDC/MDIO supports all IEEE defined registers
- IEEE 802.1AE MACsec with GCM-AES-256b encryption
- Advanced low-power equalization architecture
- Robust programmable TX equalization
- Fully adaptive and programmable RX equalization with CTLE, FFE and DFE
- IEEE KP4 RS-FEC (Clause 91) and BaseR FEC (Clause 74)
- Supports FEC bypass mode for low latency / low power applications

## Supported Standards and Interfaces

- 400G / 200G / 100G / 50G / 40G / 25G / 10G Ethernet
- 400GBASE-SR16/FR8/LR8
- 200GBASE-KR4/CR4/SR4/DR4/FR4/LR4
- 100GBASE-KR2/CR2/SR2
- 100GBASE-CR4/KR4/SR4/LR4/ER4/KP4
- 100GBASE-CR10/SR10
- 50GBASE-CR/KR/SR/FR/LR
- 40GBASE-CR4/KR4/SR4/LR4/ER4
- 25GBASE-CR/CR-S/KR/KR-S/SR
- 10GBASE-KR/CR/SR/LR/ER
- XLAUI
- 25GAUI
- 50GAUI-2/50GAUI-1/LAUI-2
- CAUI-4/CAUI-10/100GAUI-4/100GAUI-2
- 200GAUI-4/200GAUI-8
- 400GAUI-8/400GAUI-16
- CEI-56G-VSR/MR/L R-PAM4
- CEI-28G-VSR/SR/MR
- CEI-25G-LR
- CEI-11G-SR/MR/LR
- KR4 FEC RS(528, 514) for 50G and 100G Ethernet
- KP4 FEC RS(544,514) for 50G and 100G Ethernet

## Functional Block Diagram



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