



Silicon N-Channel Power MOSFET



HPD800R750PD-G

General Description:

HPD800R750PD-G, the silicon N-channel Enhanced MOSFETs, is obtained by the super junction technology which reduces the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package type is TO-252, which accords with the RoHS standard.

Features:

- | Fast Switching
- | Low Gate Charge
- | Low Reverse transfer capacitances
- | 100% Single Pulse avalanche energy Test
- | Halogen Free
- | Zener-Protected

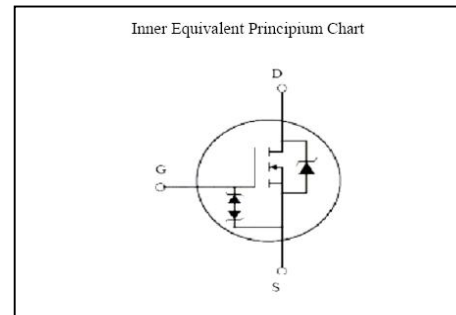
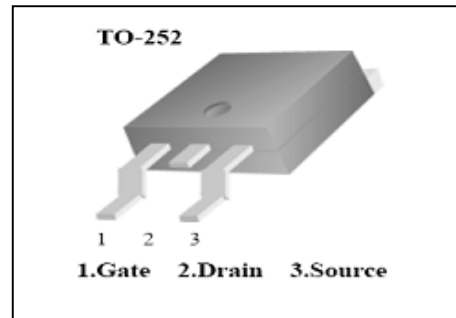
Applications:

Power switch circuit of adaptor and charger.

Absolute (T_j= 25°C unless otherwise specified):

Symbol	Parameter	Rating	Units
V _{DSS}	Drain-to-Source Voltage(V _{GS} =0V)	800	V
I _D ^{a1}	Continuous Drain Current T _C = 25 °C	7	A
I _{DM} ^{a2}	Pulsed Drain Current T _C = 25 °C	21	A
V _{GSS}	Gate-to-Source Voltage	±30	V
E _{AS} ^{a3}	Single Pulse Avalanche Energy	125	mJ
dv/dt ^{a4}	Peak Diode Recovery dv/dt	15	V/ns
dv/dt	MOSFET dv/dt ruggedness	50	V/ns
di _f /dt	Maximum diode communication speed	500	A/us
P _D	Power Dissipation(T _C =25°C)	116	W
V _{ESD(G-S)}	Gate source ESD (HBM-C= 100pF, R=1.5kΩ)	3000	V
T _J , T _{stg}	Operating and Storage Temperature Range	-55...+150	°C

V _{DSS(Tjmax)}	850	V
I _D	7	A
P _{D(Tc=25°C)}	116	W
R _{DS(ON)Typ}	0.65	Ω
E _{oss@400V}	1.3	uJ



Electrical Characteristics (T_j= 25°C unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V _{DSS}	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	800	--	--	V
ΔBV _{DSS} /ΔT _J	Bvdss Temperature Coefficient	ID=250uA	--	0.88	--	V/°C
I _{DSS}	Drain to Source Leakage Current	V _{DS} = 800V, V _{GS} = 0V, T _j = 25°C	--	--	10	μA
		V _{DS} =640V, V _{GS} = 0V, T _j = 125°C	--	--	100	
I _{GSS(F)}	Gate to Source Forward Leakage	V _{GS} =+30V V _{DS} = 0V,	--	--	10	uA
I _{GSS(R)}	Gate to Source Reverse Leakage	V _{GS} =-30V V _{DS} = 0V,	--	--	-10	uA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R _{DS(ON)}	Drain-to-Source On-Resistance	V _{GS} =10V,I _D =2.7A	--	0.65	0.75	Ω
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2.0	--	4.0	V
Pulse width tp ≤ 300μs, δ ≤ 2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R _g	Gate resistance	f = 1.0MHz	--	21	--	Ω
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = 100V f = 1.0MHz	--	682	--	pF
C _{oss}	Output Capacitance		--	18.8	--	
C _{rss}	Reverse Transfer Capacitance		--	0.15	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
t _{d(ON)}	Turn-on Delay Time	I _D =2.7A V _{DD} = 400V V _{GS} = 13V R _G =12Ω	--	16	--	ns
t _r	Rise Time		--	7.8	--	
t _{d(OFF)}	Turn-Off Delay Time		--	81	--	
t _f	Fall Time		--	37	--	
Q _g	Total Gate Charge	ID =2.7A VDD =640V VGS = 10V	--	22	--	nC
Q _{gs}	Gate to Source Charge		--	2.9	--	
Q _{gd}	Gate to Drain (“Miller”)Charge		--	11.6	--	
V _{plateau}	Gate Plateau Voltage		--	4.5	--	



Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)	$T_c=25^\circ\text{C}$	--	--	7	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	21	A
V_{SD}	Diode Forward Voltage	$I_S=3.5\text{A}, V_{GS}=0\text{V}$	--	--	1.2	V
T_{rr}	Reverse Recovery Time	$I_S=1.4\text{A}, T_j = 25^\circ\text{C}$ $dI_F/dt=100\text{A}/\mu\text{s},$ $V_{GS}=0\text{V}$	--	151	--	ns
Q_{rr}	Reverse Recovery Charge		--	904	--	nC
I_{rrm}	Reverse Recovery Current		--	12	--	A

Thermal Restistance

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	1.08	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient	100	$^\circ\text{C}/\text{W}$

Gate-source Zener diode						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{GSO}	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{mA}(\text{Open Drain})$	30			V
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.						

- ^{a1}: Limited by T_{jmax} Maximum duty cycle $D=0.75$
- ^{a2}: Repetitive rating; pulse width limited by maximum junction temperature
- ^{a3}: $L=20.0\text{mH}, R_g=25\ \Omega, V_{dd}=50\text{V}, \text{Start } T_j=25^\circ\text{C}$
- ^{a4}: Identical low side and high side switch with identical R_g
- ^{a5}: Recommend soldering temperature defined by IPC/JEDEC J-STD 020

Characteristics Curve:

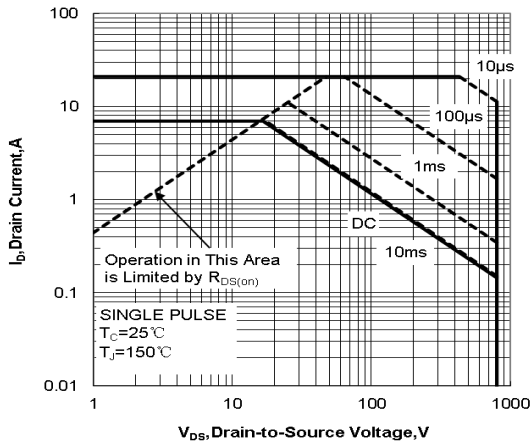


Figure.1 Maximum Forward Bias Safe Operating Area

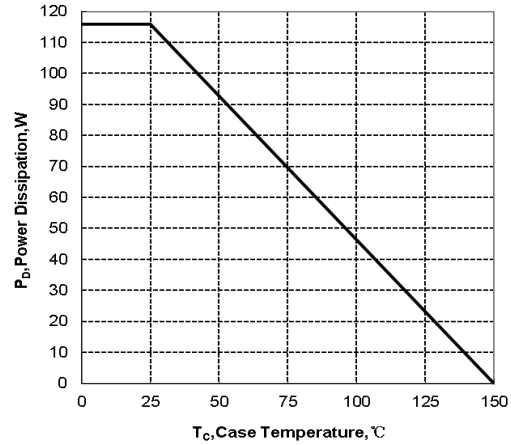


Figure.2 Maximum Power Dissipation vs Case Temperature

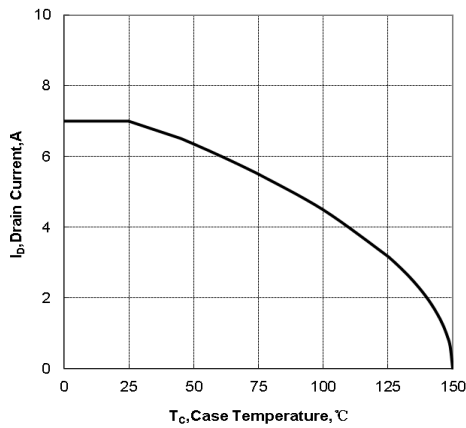


Figure.3 Maximum Continuous Drain Current vs Case Temperature

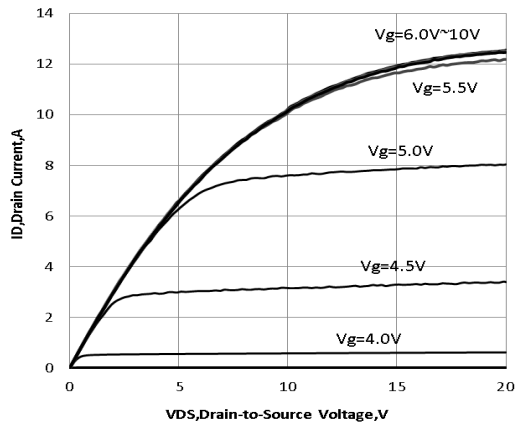


Figure.4 Typical Output Characteristics

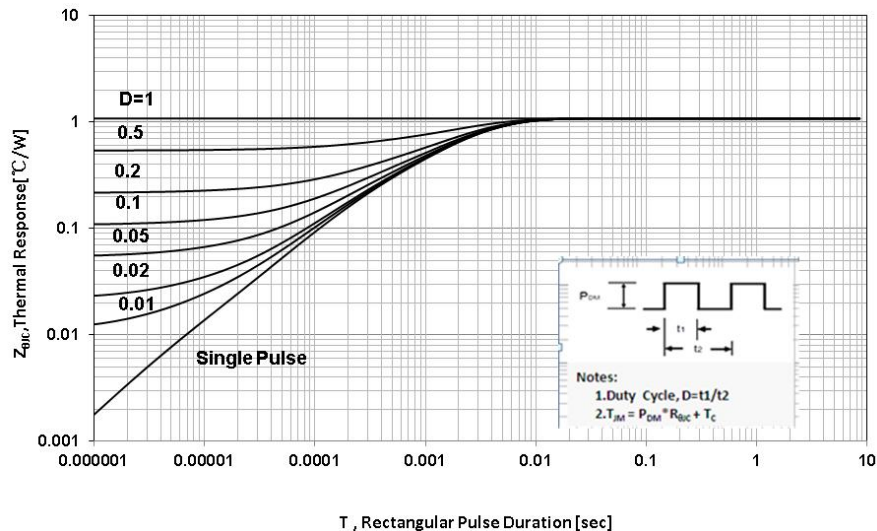


Figure.5 Maximum Effective Thermal Impedance, Junction to Case

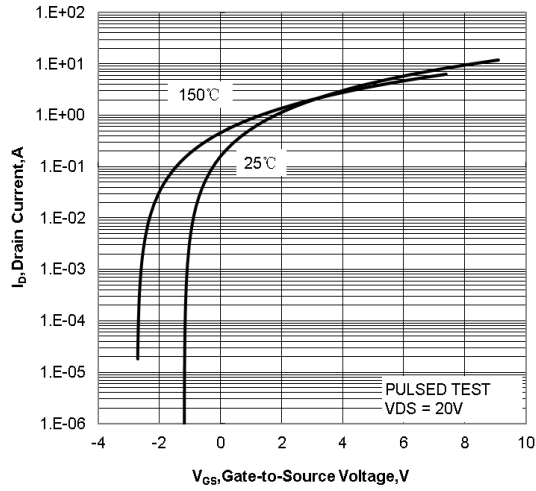


Figure.6 Typical Transfer Characteristics

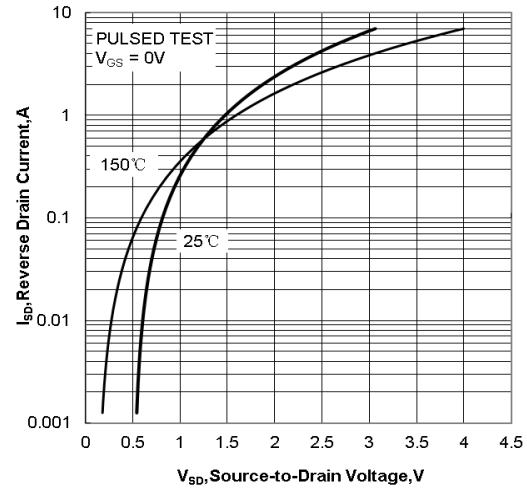


Figure.7 Typical Body Diode Transfer Characteristics

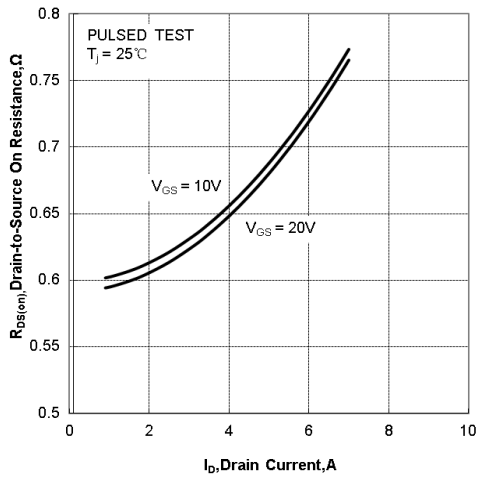


Figure.8 Typical Drain to Source ON Resistance vs Drain Current

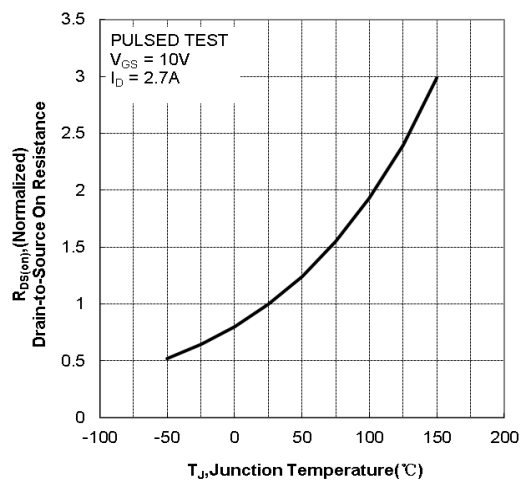


Figure.9 Typical Drain to Source on Resistance vs Junction Temperature

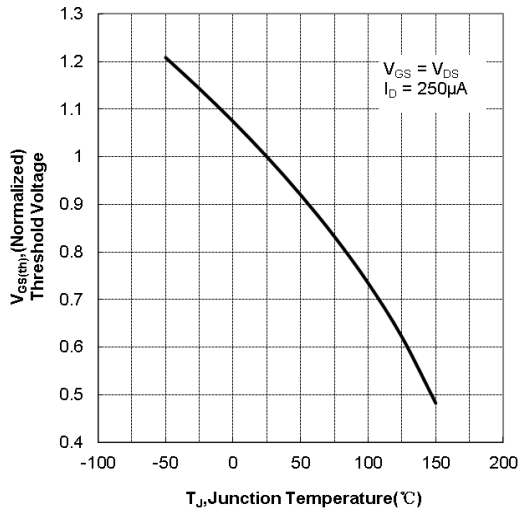


Figure.10 Typical Theshold Voltage vs Junction Temperatu

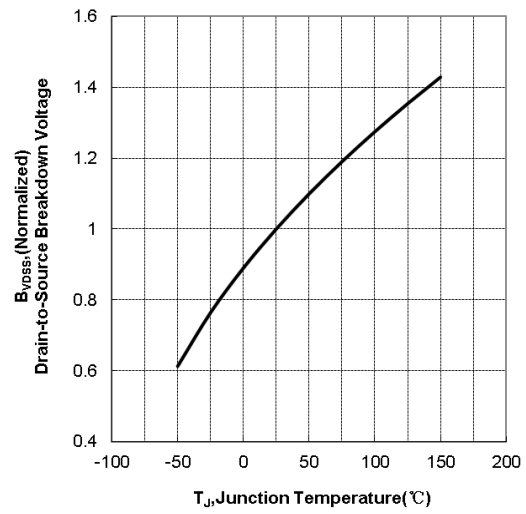


Figure 11 Typical Breakdown Voltage vs Junction Temperature

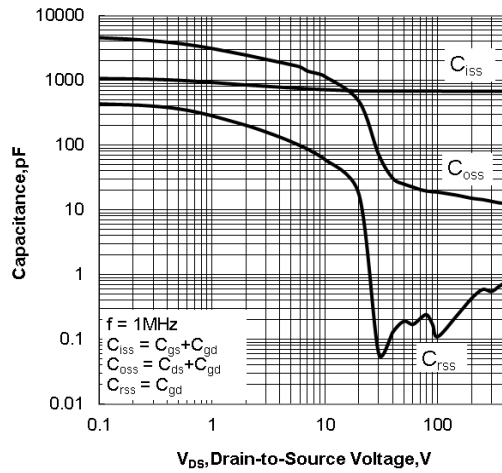


Figure.12 Typical Capacitance vs Drain to Source Voltage

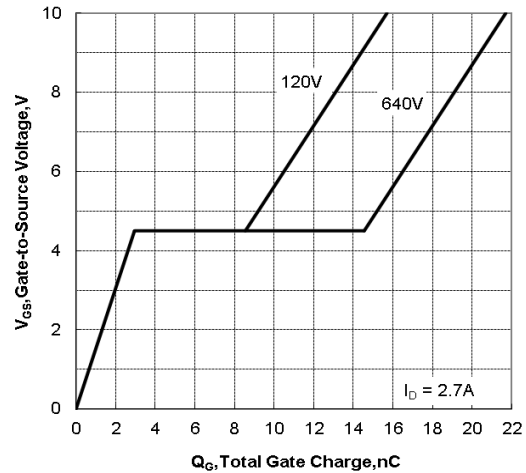


Figure.13 Typical Gate Charge vs Gate to Source Voltage

Test Circuit and Waveform



Figure 14. Gate Charge Test Circuit

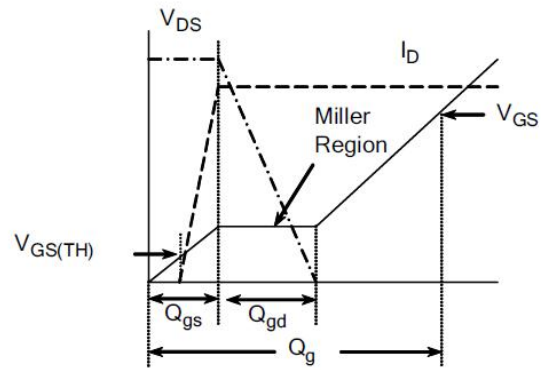


Figure 15. Gate Charge Waveforms



Figure 16. Resistive Switching Test Circuit



Figure 17. Resistive Switching Waveforms

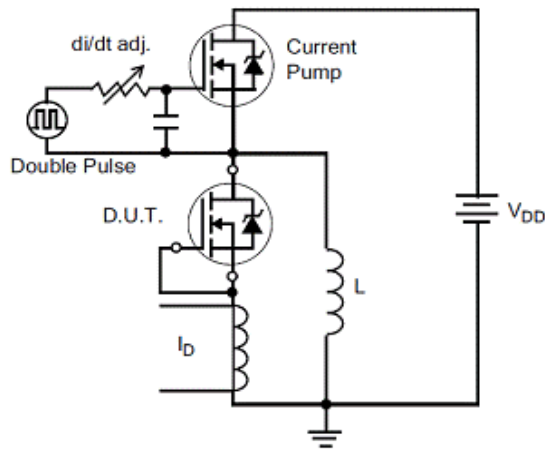


Figure 18. Diode Reverse Recovery Test Circuit

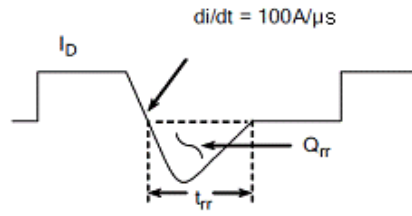


Figure 19. Diode Reverse Recovery Waveform

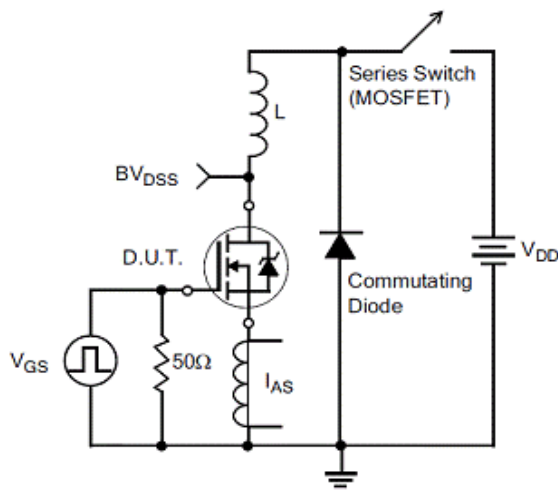


Figure 20. Unclamped Inductive Switching Test Circuit

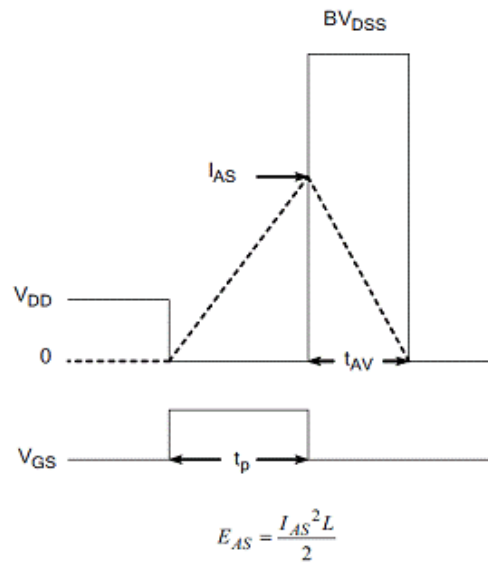
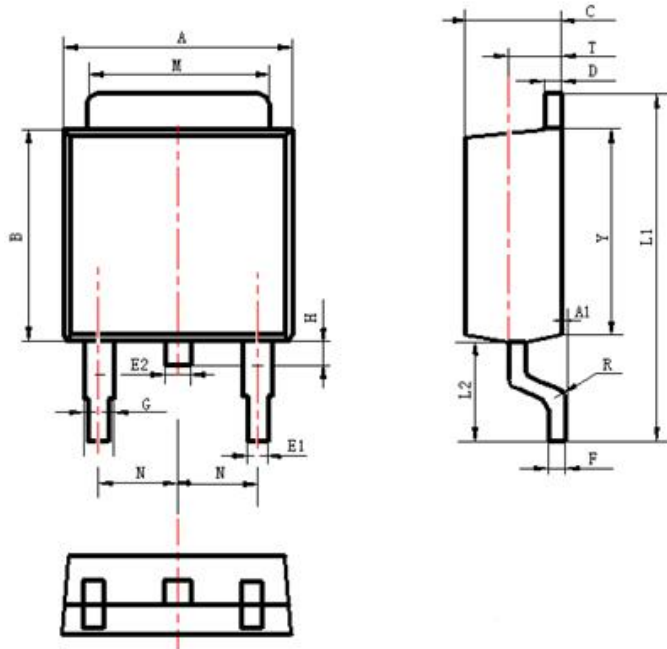


Figure 21. Unclamped Inductive Switching Waveform

Package Information



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
A1	0	0.16
B	5.70	6.30
C	2.10	2.50
D	0.30	0.70
E1	0.60	0.90
E2	0.70	1.00
F	0.30	0.60
G	0.70	1.20
L1	9.60	10.50
L2	2.70	3.10
H	0.40	1.00
M	5.10	5.50
N	2.09	2.49
R	0.3	
T	1.40	1.60
Y	5.10	6.30

TO-252 Package

The name and content of poisonous and harmful material in products

	Hazardous Substance									
	Pb	Hg	Cd	Cr(VI)	PBB	PBDE	DBP	DEHP	DBP	BBP
Limit	≤0.1%	≤0.1%	≤ 0.01%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%
Lead Frame	○	○	○	○	○	○	○	○	○	○
Molding	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
Wire Bonding	○	○	○	○	○	○	○	○	○	○
Solder	×	○	○	○	○	○	○	○	○	○
Note	○: Means the hazardous material is under the criterion of 2011/65/EU. ×: Means the hazardous material exceeds the criterion of 2011/65/EU. The plumbum element of solder exist in products presently, but within the allowed range of Eurogroup's RoHS.									

Warnings

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. It is suggested to be used under 80 percent of the maximum ratings of the device.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heatsink.
3. VDMOSFET is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. This publication is made by HuaJing Microelectronics and subject to regular change without notice.

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