uPOL Module

5A, High Efficiency uPOL Module

MUN12AD05-SMF SERIES

FEATURES:

- High Density uPOL Module
- 5A Output Current
- Input Voltage Range from 4.5 to 20V
- Output Voltage Range
  1.9V to 5V for MUN12AD05-SMFH
  0.6V to 1.8V for MUN12AD05-SMFL
- 92% Peak Efficiency(@Vin=12V)
- Enable / PGOOD Function
- Force PWM Mode
- Protections (Non-latching: OCP, OTP, SCP, OVP)
- Internal Soft Start
- Compact Size: 6mm*6mm*3.5mm(Max)
- Pb-free for RoHS compliant
- MSL 2, 250℃ Reflow

APPLICATIONS:

- Distributed Power Supply
- Server, Workstation, and Storage
- Networking and Datacom

GENERAL DESCRIPTION:

The uPOL module is non-isolated dc-dc converters that can deliver up to 5A of output current. The PWM switching regulator, high frequency power inductor are integrated in one hybrid package.

Instant PWM architecture to achieve fast transient responses. Other features include remote enable function, internal soft-start, non-latching over current protection and power good.

The low profile and compact size package (6.0mm × 6.0mm x 3.5mm) is suitable for automated assembly by standard surface mount equipment. The uPOL module is Pb-free and RoHS compliance.

TYPICAL APPLICATION CIRCUIT:

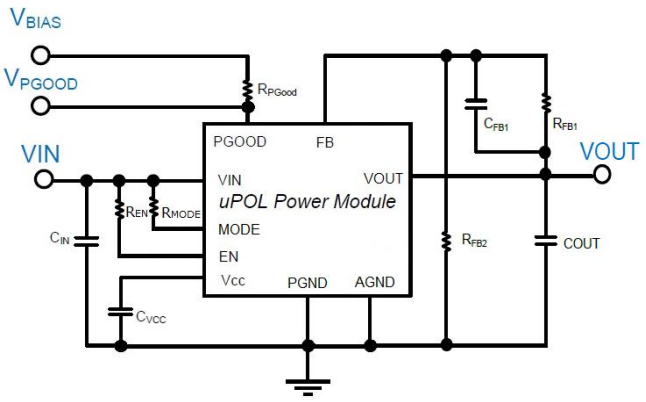


FIG. 1 TYPICAL APPLICATION CIRCUIT

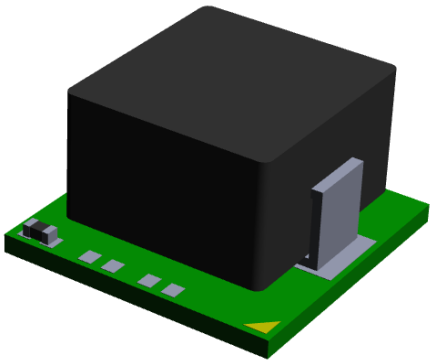


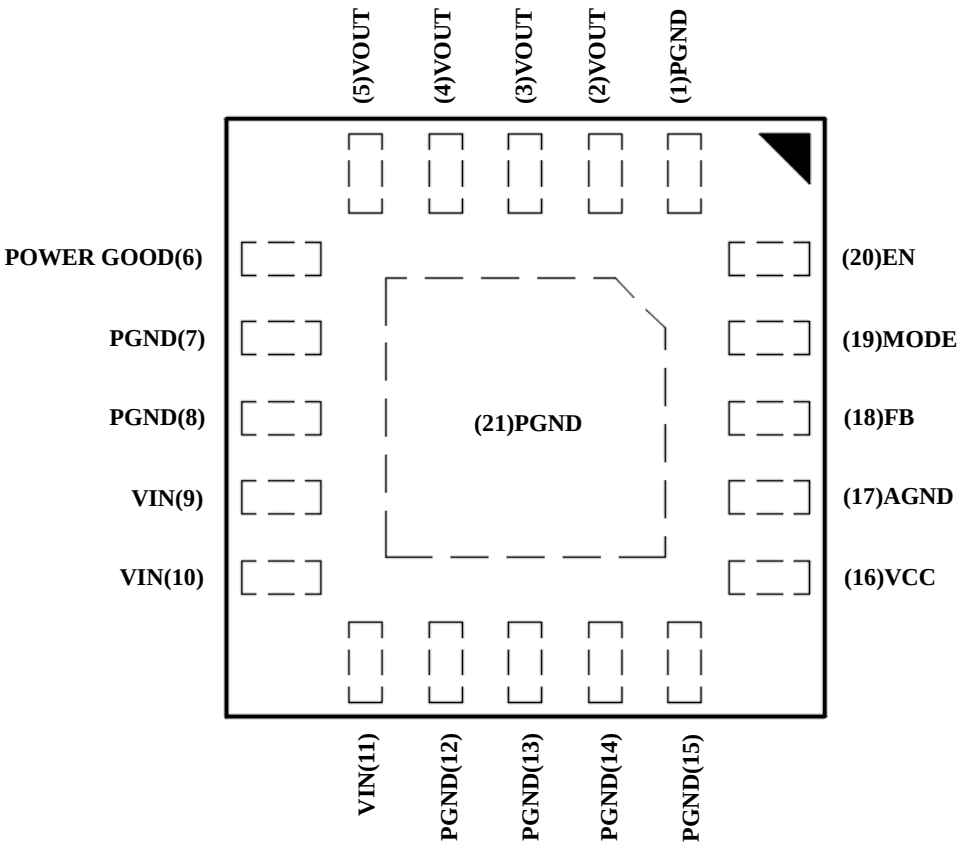
FIG. 2 HIGH DENSITY uPOL MODULE

ORDER INFORMATION:

Part Number	Ambient Temp. Range (°C)	Package (Pb-Free)	MSL	Note
MUN12AD05-SMFH	-40 ~ +85	QFN	Level 2	-
MUN12AD05-SMFL	-40 ~ +85	QFN	Level 2	-

Order Code	Packing	Quantity
MUN12AD05-SMFH	Tape and reel	1000
MUN12AD05-SMFL	Tape and reel	1000

PIN CONFIGURATION:



TOP VIEW

PIN DESCRIPTION:

Symbol	Pin No.	Description
PGND	1,7,8,12,13, 14, 15,21	Power ground pin, input, and output return path. This pin needs to connect one or more ground plane directly. Connect to thermal exposed pad of PGND_TPD(21) for heat transferring.
VOUT	2,3, 4, 5	Power output pin. These pins should be connected by a copper island under for thermal relief. Place the output capacitors as closely as possible to this pin.
PGOOD	6	Power good Indicator. Open drain output when the output voltage is within 90% to 120% of regulation point.
VIN	9, 10, 11	Power input pin. It needs to connect input rail and for heat transferring. Place the input ceramic type capacitor as closely as possible to this pin. One capacitor of 10uF at least for input capacitance.
VCC	16	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Connect a 2.2uF for Bypass capacitor.
AGND	17	Signal ground of the IC.
FB	18	Feedback input. Connect an external resistor divider to set the output voltage.
MODE	19	Pull this pin high for PWM operation. Do not leave this pin floating.
EN	20	On/Off control pin for module. Do not leave this pin floating.

ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN to GND		-0.3	-	+25	V
VOUT to GND		-0.3	-	+6	V
PHASE to GND		-0.3	-	+25	V
PGOOD to GND		-0.3	-	+25	V
VCC to GND		-0.3	-	+4.0	V
FB to GND		-0.3	-	+4.0	V
EN to GND		-0.3	-	+25	V
Tc	Case Temperature of Inductor	-	-	+110	℃
Tstg	Storage Temperature	-40	-	+125	℃
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+4.5		+20	V
VOUT	Adjusted Output Voltage (Note 1)	+1.9	-	+5	V
	Adjusted Output Voltage (Note 2)	+0.6	-	+1.8	V
Ta	Ambient Temperature	-40	-	+85	℃
■ Thermal Information					
Rth(j_{choke}-a)	Thermal resistance from junction to ambient (Note 3)	-	26	-	°C/W

NOTES:
1. Input Supply Voltage and Output voltage range for MUN12AD05-SMFH application
2. Input Supply Voltage and Output voltage range for MUN12AD05-SMFL application
3. Rth(j_{choke}-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 30mm×30mm×1.6mm with 4 layers. The test condition is complied with JEDEC EIJ/JESD 51 Standards.

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Vin=12V Vout=2.5V
Cin = 4.7uF/25V/1206x2, Cout = 47uF/6.3V/1206x3、100nF/16V/0603x1

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
$I_{SD(IN)}$	Input shutdown current	Vin =12V, EN = GND	-	10	-	uA
$I_{(IN)}$	Input supply current	Vin = 12V, Iout = 0A Vout = 2.5V, EN = VIN	-	145	-	uA
$I_{S(IN)}$	Input supply current	Vin = 12V, EN = VIN				
		Iout = 5mA,Vout =2.5V	-	14	-	mA
		Iout = 5A,Vout =2.5V	-	1.19	-	A
■ Output Characteristics						
$I_{OUT(DC)}$	Output continuous current range		0	-	5	A
$V_{O(SET)}$	Output Voltage Set Point	With 0.1% tolerance for external resistor used to set output voltage(Iout=5A)	-2	-	+2	% $V_{O(SET)}$
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	Vin = 7.0V to 15V Vout = 2.5V, Iout = 0A Vout = 2.5V, Iout = 5A	-	0.5	-	% $V_{O(SET)}$
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	Iout = 0A to 5A Vin = 12V, Vout = 2.5V PWM Mode	-	1	-	% $V_{O(SET)}$
$V_{OUT(AC)}$	Output ripple voltage	Vin = 12V, Vout = 2.5V EN = VIN,20MHz Bandwidth	-	-	-	-
		Iout = 5mA	-	10	-	mVp-p
		Iout = 5A	-	10	-	mVp-p
■ Control Characteristics						
F_{OSC}	Oscillator frequency		-	0.6	-	MHz
V_{REF}	Referance voltage		0.594	0.600	0.606	V
V_{PG_TH}	PGOOD high	Respect the V_{REF}	88	90	92	% V_{out}
V_{PG_LV}	PGOOD logic low voltage	I_{PGOOD}=4mA	0.04	0.15	0.3	V
I_{ILIM}	Over current limit		6.7		12	A
V_{ENL}	EN Low threshold		0	-	0.4	V
V_{ENH}	EN High Threshold		1.2	-	VIN	V
OVP	Output Over Voltage protection	V_{out} Rising	-	120	-	%V_{out}
D_{MAX}	Maximum Duty Cycle		80	85	-	%

TYPICAL PERFORMANCE CHARACTERISTICS: (1.0 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin = 4.7uF/25V/1206x2, Cout = 47uF/6.3V/1206x3、100nF/16V/0603x1
The following figures provide the typical characteristic curves at 1.0Vout.

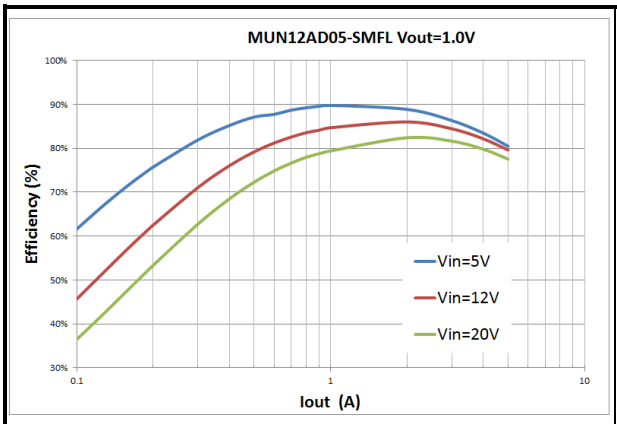


FIG.3 EFFICIENCY V.S. LOAD CURRENT

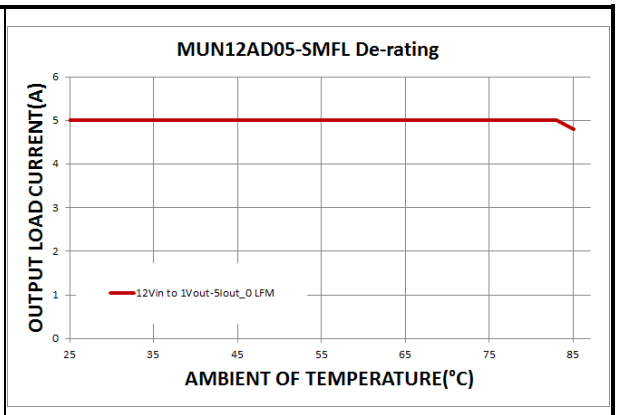


FIG.4 12VIN DE-RATING CURVE

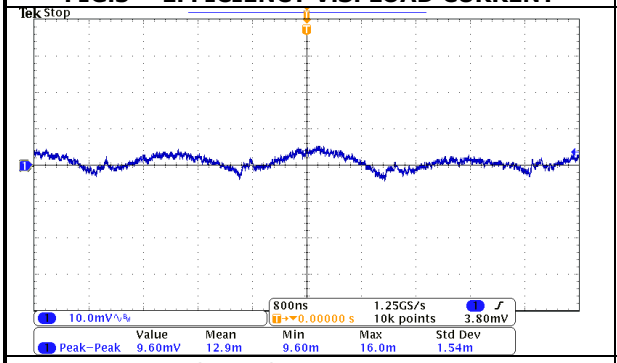


FIG.5 OUTPUT RIPPLE
(12VIN, 1.0VOUT, IOUT=0A)

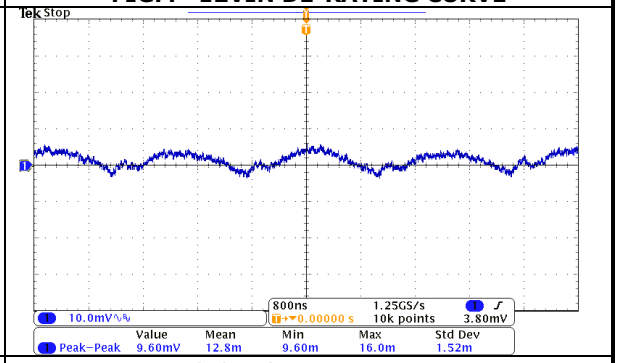


FIG.6 OUTPUT RIPPLE
(12VIN, 1.0VOUT, IOUT=5A)

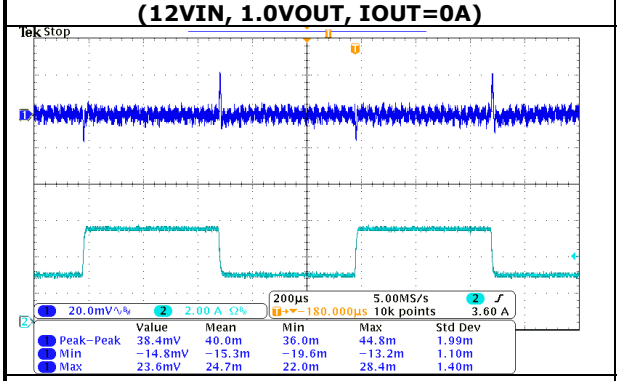


FIG.7 TRANSIENT RESPONSE
(12VIN, 1.0VOUT, 50% to 100% LOAD STEP)

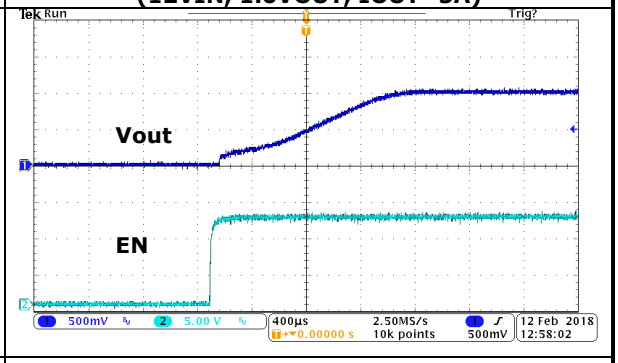


FIG.8 TURN-ON
(12VIN, 1.0VOUT, IOUT=5A)

TYPICAL PERFORMANCE CHARACTERISTICS: (1.2 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin = 4.7uF/25V/1206x2, Cout = 47uF/6.3V/1206x3、100nF/16V/0603x1
The following figures provide the typical characteristic curves at 1.2Vout.

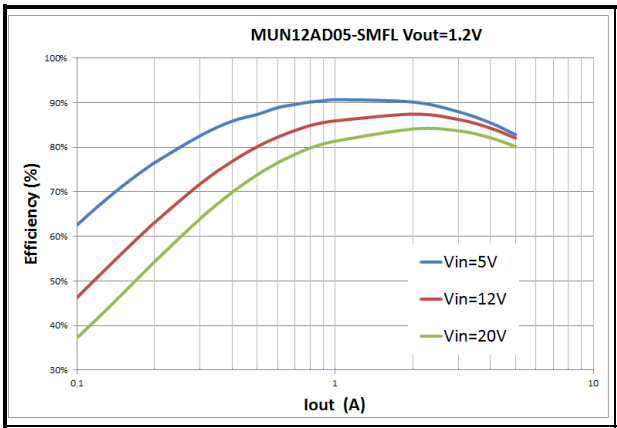


FIG.9 EFFICIENCY V.S. LOAD CURRENT

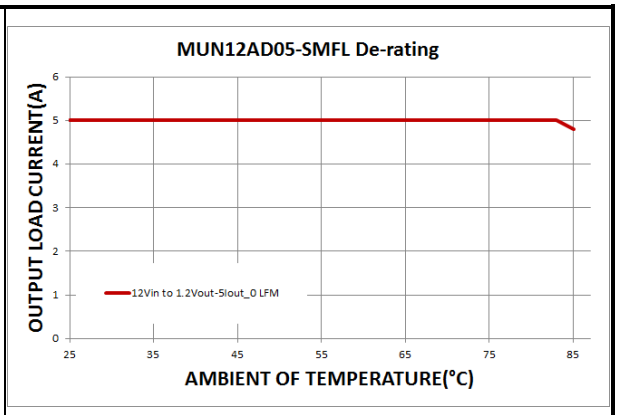


FIG.10 12VIN DE-RATING CURVE

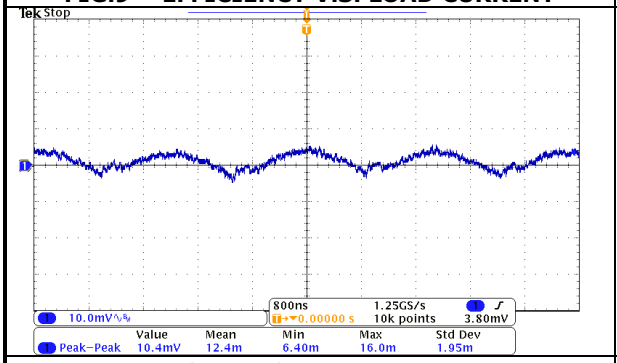


FIG.11 OUTPUT RIPPLE
(12VIN, 1.2VOUT, IOUT=0A)

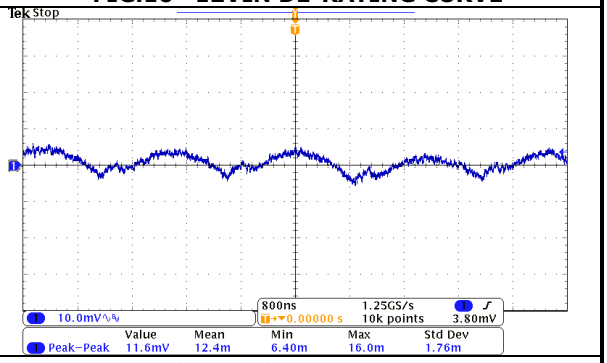


FIG.12 OUTPUT RIPPLE
(12VIN, 1.2VOUT, IOUT=5A)

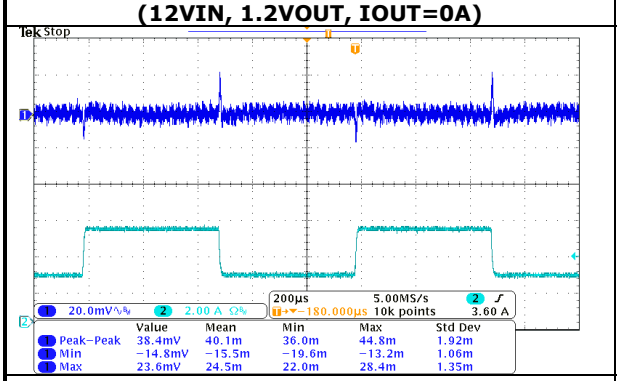


FIG.13 TRANSIENT RESPONSE
(12VIN, 1.2VOUT, 50% to 100% LOAD STEP)

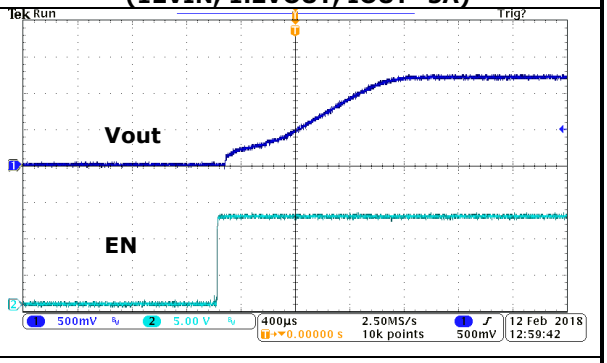


FIG.14 TURN-ON
(12VIN, 1.2VOUT, IOUT=5A)

TYPICAL PERFORMANCE CHARACTERISTICS: (1.8 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin = 4.7uF/25V/1206x2, Cout = 47uF/6.3V/1206x3、100nF/16V/0603x1
The following figures provide the typical characteristic curves at 1.8Vout.

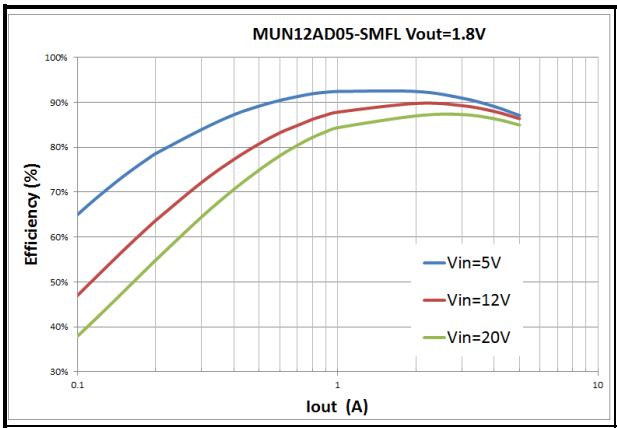


FIG.15 EFFICIENCY V.S. LOAD CURRENT

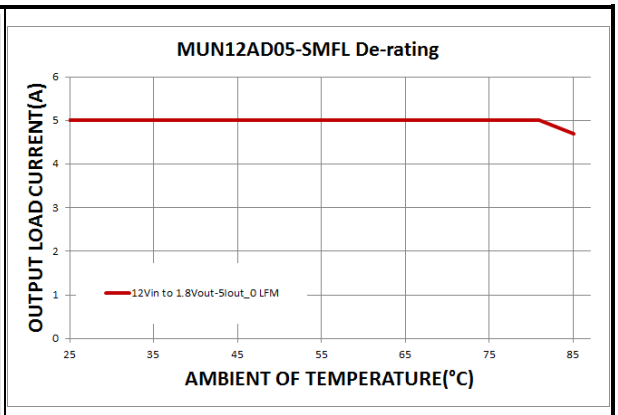


FIG.16 12VIN DE-RATING CURVE

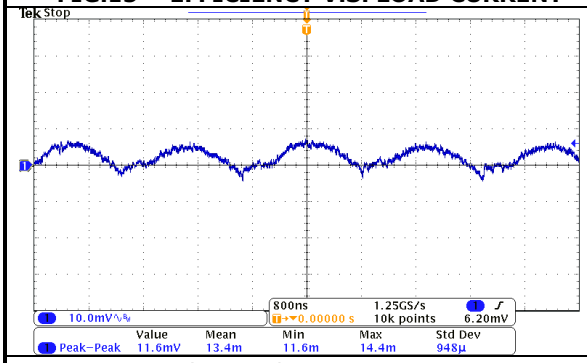


FIG.17 OUTPUT RIPPLE
(12VIN, 1.8VOUT, IOUT=0A)

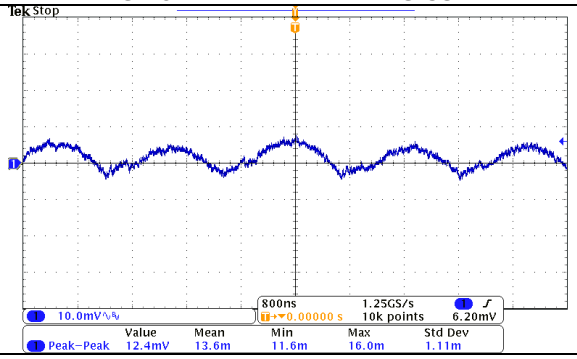


FIG.18 OUTPUT RIPPLE
(12VIN, 1.8VOUT, IOUT=5A)

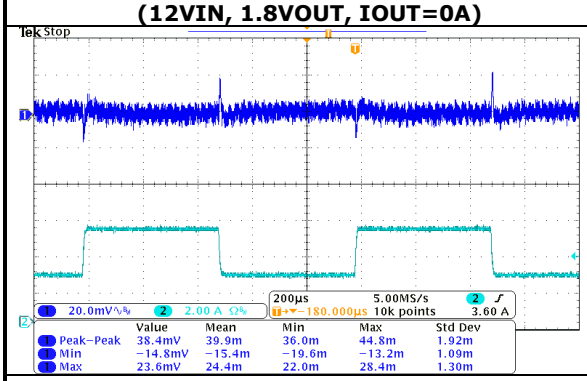


FIG.19 TRANSIENT RESPONSE
(12VIN, 1.8VOUT, 50% to 100% LOAD STEP)

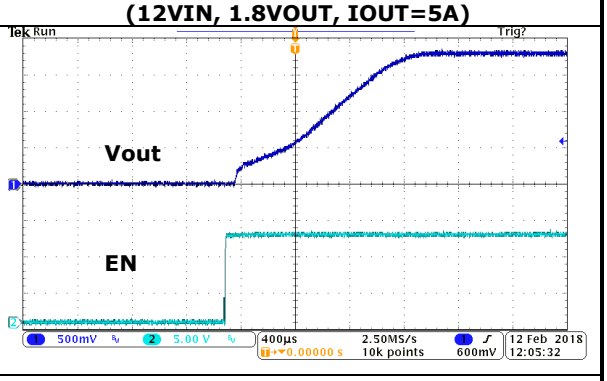


FIG.20 TURN-ON
(12VIN, 1.8VOUT, IOUT=5A)

TYPICAL PERFORMANCE CHARACTERISTICS: (2.5 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin = 4.7uF/25V/1206x2, Cout = 47uF/6.3V/1206x3、100nF/16V/0603x1
The following figures provide the typical characteristic curves at 2.5Vout.

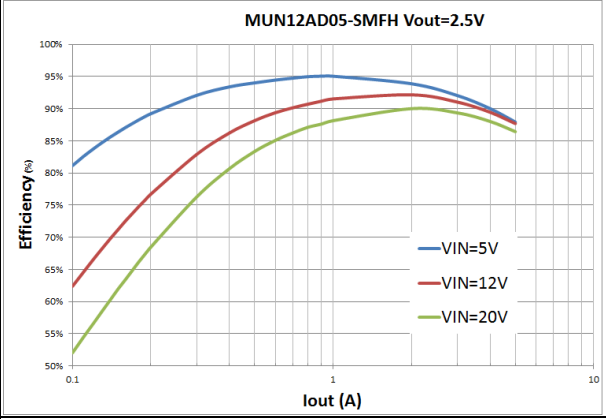


FIG.21 EFFICIENCY V.S. LOAD CURRENT

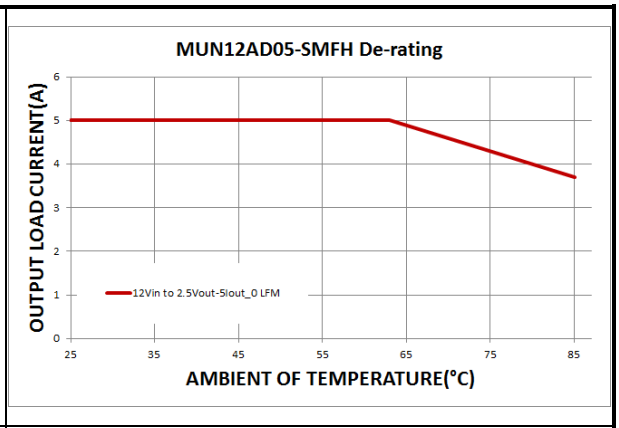


FIG.22 12VIN DE-RATING CURVE

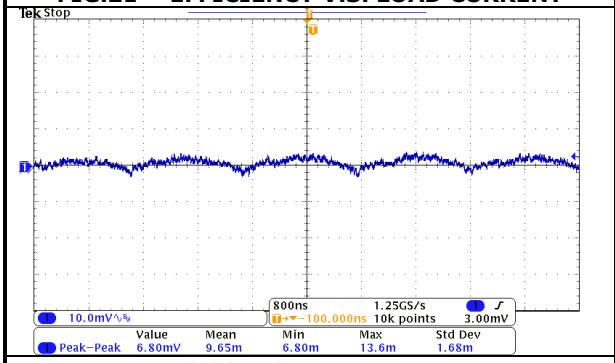


FIG.23 OUTPUT RIPPLE
(12VIN, 2.5VOUT, IOUT=0A)

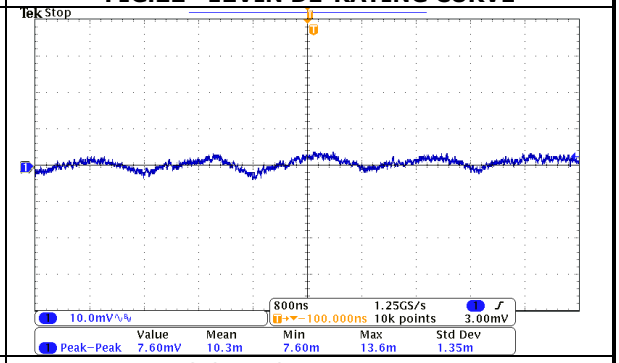


FIG.24 OUTPUT RIPPLE
(12VIN, 2.5VOUT, IOUT=5A)

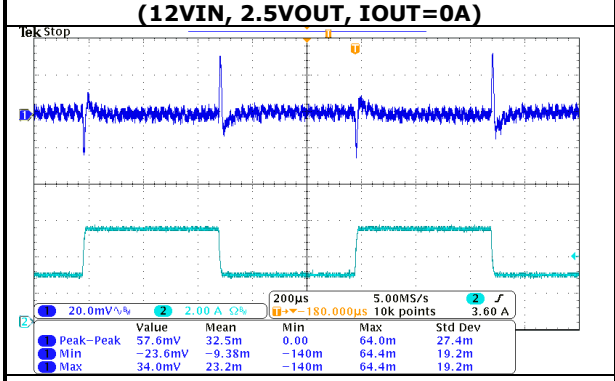


FIG.25 TRANSIENT RESPONSE
(12VIN, 2.5VOUT, 50% to 100% LOAD STEP)

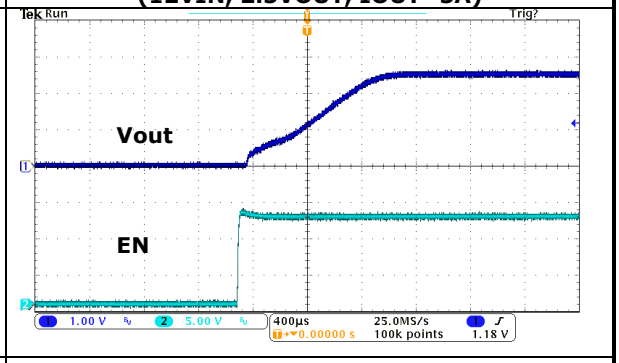


FIG.26 TURN-ON
(12VIN, 2.5VOUT, IOUT=5A)

TYPICAL PERFORMANCE CHARACTERISTICS: (3.3 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin = 4.7uF/25V/1206x2, Cout = 47uF/6.3V/1206x3、100nF/16V/0603x1
The following figures provide the typical characteristic curves at 3.3Vout.

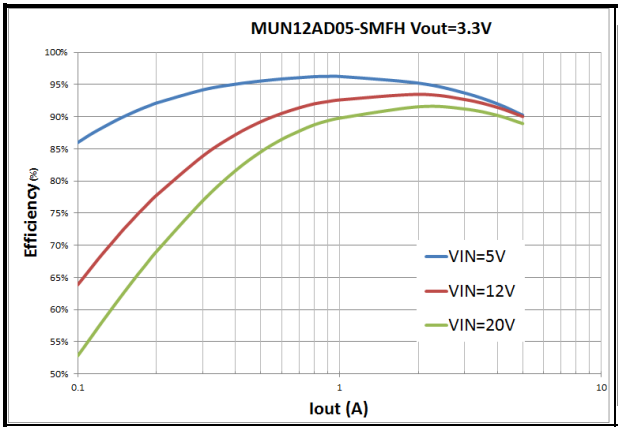


FIG.27 EFFICIENCY V.S. LOAD CURRENT

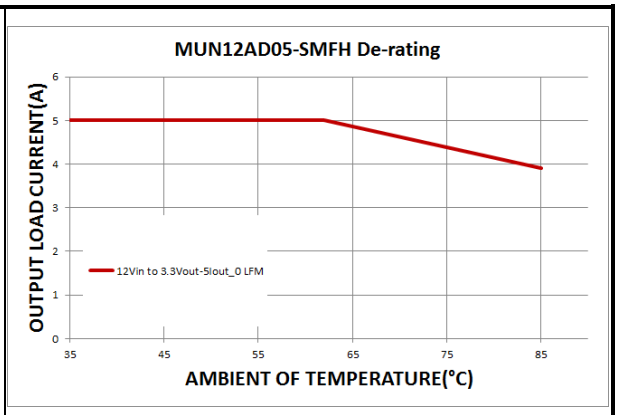


FIG.28 12VIN DE-RATING CURVE

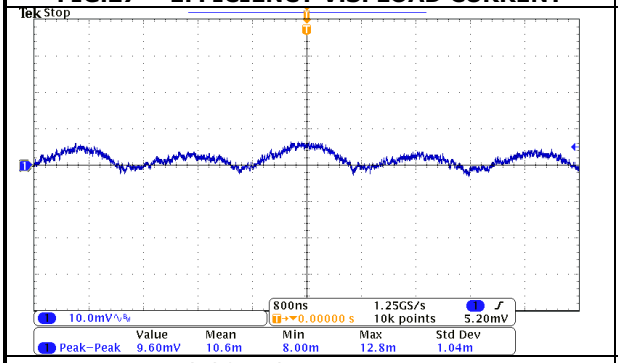


FIG.29 OUTPUT RIPPLE
(12VIN, 3.3VOUT, IOUT=0A)

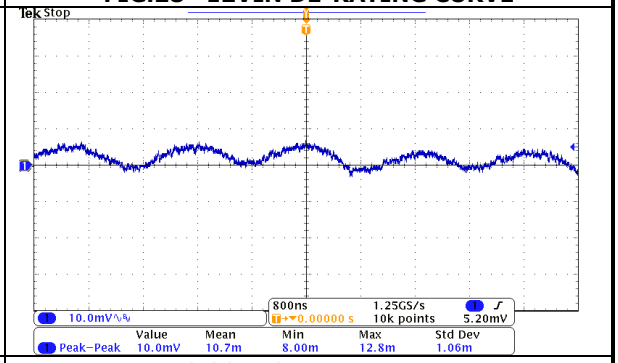


FIG.30 OUTPUT RIPPLE
(12VIN, 3.3VOUT, IOUT=5A)

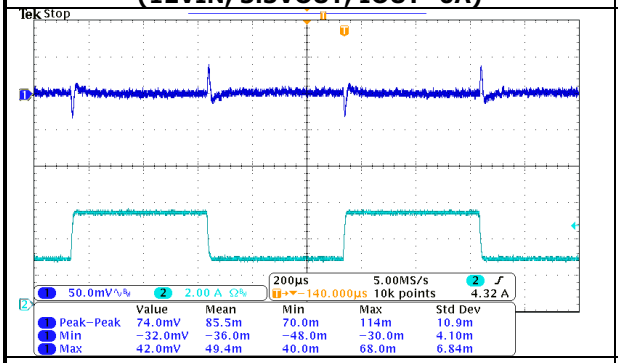


FIG.31 TRANSIENT RESPONSE
(12VIN, 3.3VOUT, 50% to 100% LOAD STEP)

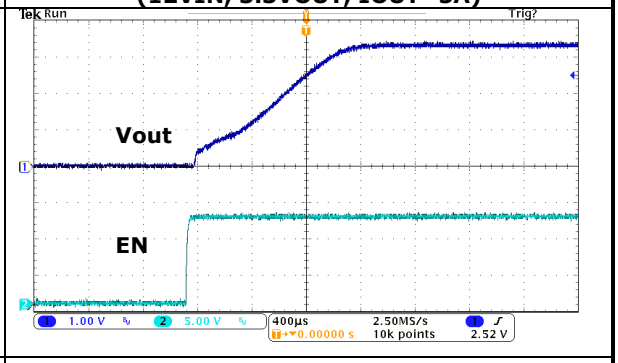


FIG.32 TURN-ON
(12VIN, 3.3VOUT, IOUT=5A)

TYPICAL PERFORMANCE CHARACTERISTICS: (5 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2Oz . The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Cin = 4.7uF/25V/1206x2, Cout = 47uF/6.3V/1206x3、100nF/16V/0603x1

The following figures provide the typical characteristic curves at 5Vout.

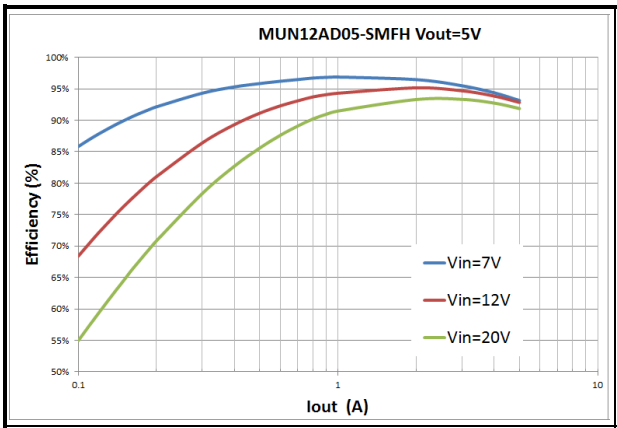


FIG.33 EFFICIENCY V.S. LOAD CURRENT

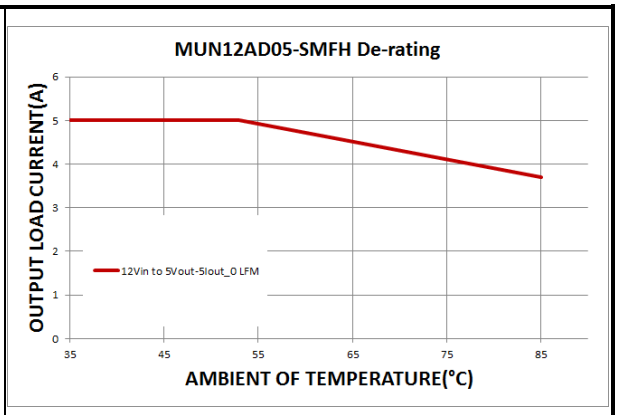


FIG.34 12VIN DE-RATING CURVE

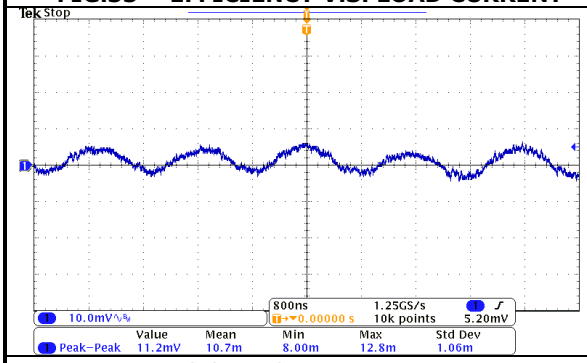


FIG.35 OUTPUT RIPPLE
(12VIN, 5VOUT, IOUT=0A)

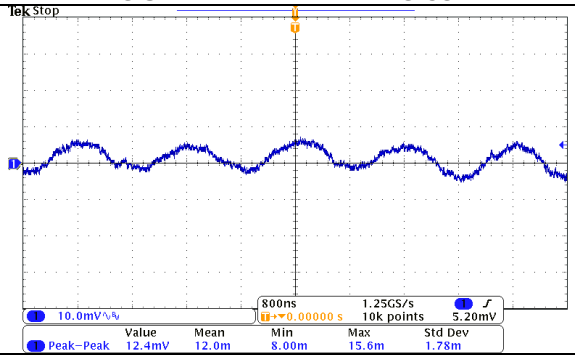


FIG.36 OUTPUT RIPPLE
(12VIN, 5VOUT, IOUT=5A)

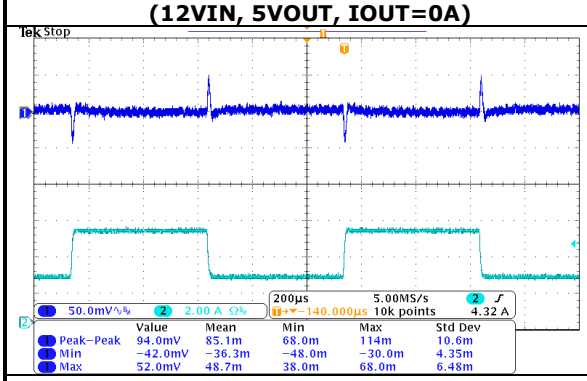


FIG.37 TRANSIENT RESPONSE
(12VIN, 5VOUT, 50% to 100% LOAD STEP)

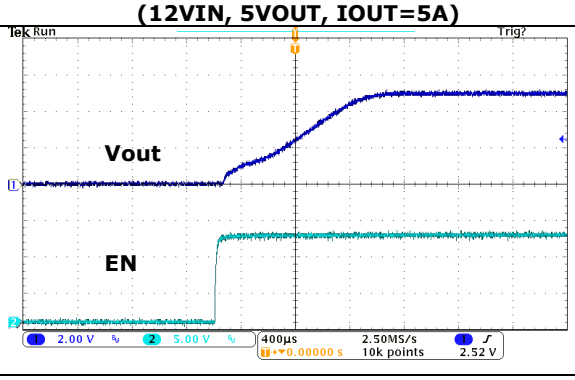


FIG.38 TURN-ON
(12VIN, 5VOUT, IOUT=5A)

APPLICATIONS INFORMATION: (Cont.)

INPUT FILTERING:

The module should be connected to a source supply of low AC impedance and high inductance in which line inductance can affect the module stability. An input capacitor must be placed as near as possible to the input pin of the module so to minimize input ripple voltage and ensure module stability.

OUTPUT FILTERING:

To reduce output ripple and improve the dynamic response as the step load changes, an additional capacitor at the output must be connected. Low ESR polymer and ceramic capacitors are recommended to improve the output ripple and dynamic response of the module.

LOAD TRANSIENT CONSIDERATIONS:

The MUN12AD05-SMF module adopts the instant PWM architecture to achieve good stability and fast transient responses. In applications with high step load current, adding 47pF Capacitor (C_{FB}) in parallel with R_{FB1} may further speed up the load transient responses.

PROGRAMMING OUTPUT VOLTAGE:

The module has an internal 0.6V reference voltage. The output voltage can be programmed by the dividing resistor (R_{FB1} and R_{FB2}). The output voltage can be calculated by Equation 1, resistor choice may be referred TABLE 1.

$$VOUT\ (V) = 0.6 \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \qquad \text{(EQ.1)}$$

Vout	RFB1(Ohm)	RFB2 (Ohm)
1.0V	100k	150k
1.2V	100k	100k
1.8V	100k	50k
2.5V	100k	31.6k
3.3V	100k	22.1k
5.0V	100k	13.7k

TABLE 1 Resistor values for common output voltages

APPLICATIONS INFORMATION: (Cont.)

REFERENCE CIRCUIT FOR GENERAL APPLICATION:

Figure 39 show the module application schematics for input voltage +12V.

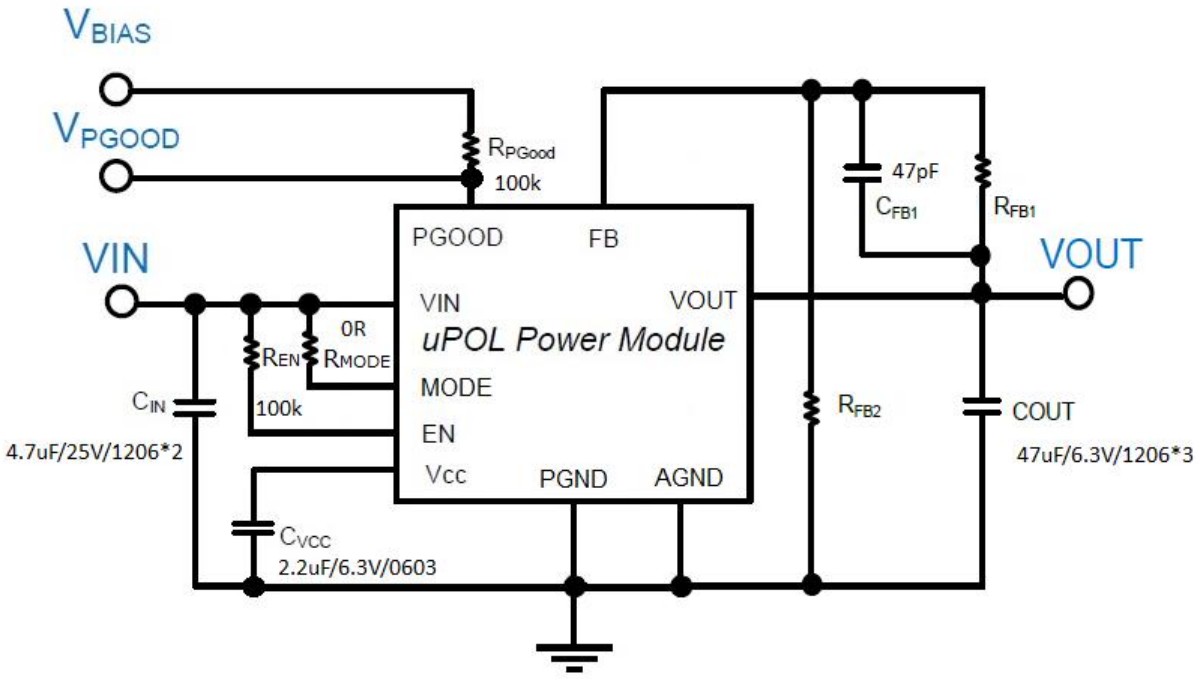


FIG.39 Reference Circuit for General Application

APPLICATIONS INFORMATION: (Cont.)

RECOMMENDATION LAYOUT GUIDE:

In order to achieve stable, low losses, less noise or spike, and good thermal performance some layout considerations are necessary. The recommendation layout is shown as Figure 40.

1. The ground connection between pin 1, 7, 8, 21 and PIN12 to15 should be a solid ground plane under the module. It can be connected one or more ground plane by using several Vias.
2. Place high frequency ceramic capacitors between pin 9 to 11 (VIN), and pin 7 to 8, pin 21 (PGND) for input side; and pin 2 to 5 (VOUT), and pin 7 to 8, pin21 (PGND) for output side, as close to module as possible to minimize high frequency noise.
3. Keep the R_{FB1} and R_{FB2} connection trace to the module pin 18 (FB) short.
4. Use large copper area for power path (VIN, VOUT, and GND) to minimize the conduction loss and enhance heat transferring. Also, use multiple Vias to connect power planes in different layer.
5. If the system chip interfacing with the pin 20 (EN) has a high impedance state at shutdown mode and the VIN pin is connected directly to a power source such as a Li-Ion battery. A 1MΩ pull down resistor should be placed between the enable pin and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

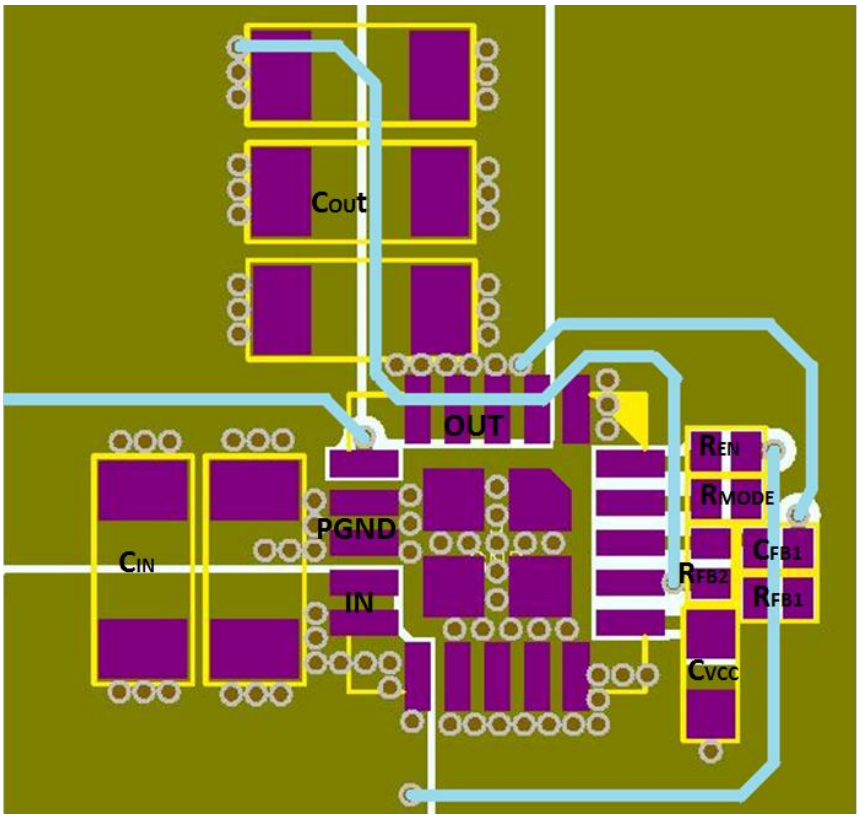


FIG.40 Recommendation Layout

REFLOW PARAMETERS:

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Figure 56 shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60 seconds limit to melt the solder and make the peak temperature at the range from 240°C to 250°C. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

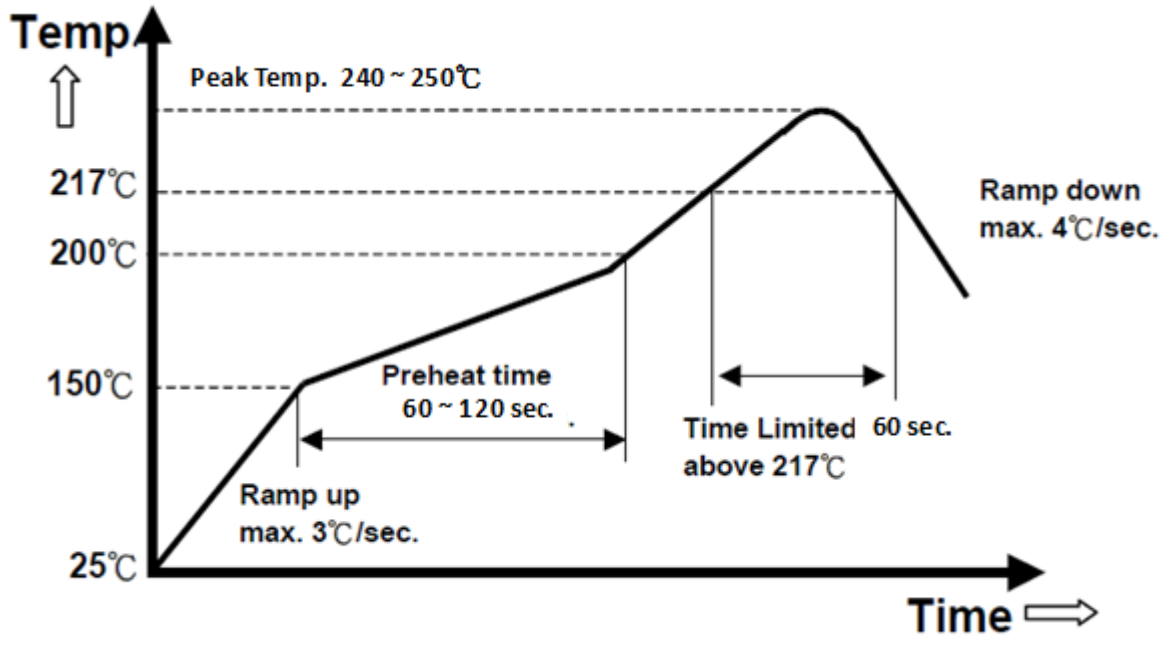
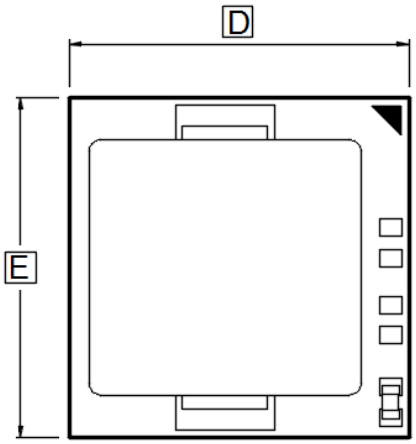


FIG.41 Recommendation Reflow Profile

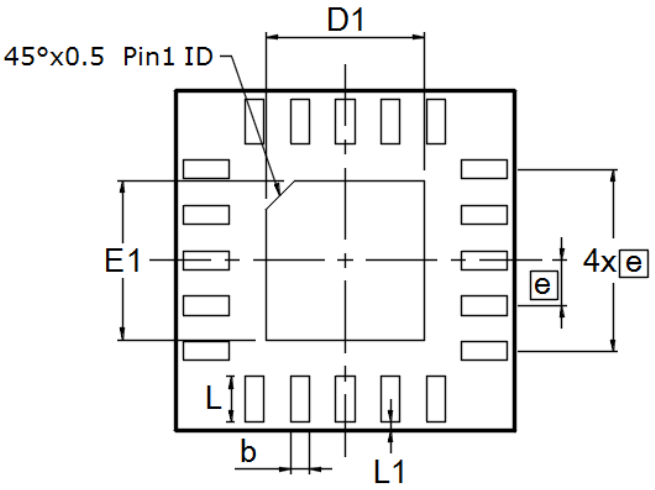
PACKAGE OUTLINE DRAWING:

Unit: mm

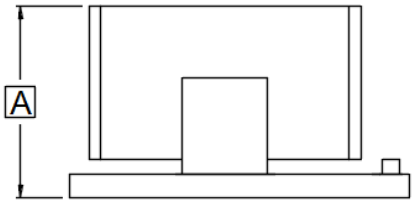
General Tolerance: +/- 0.1mm



TOP VIEW



BOTTOM VIEW

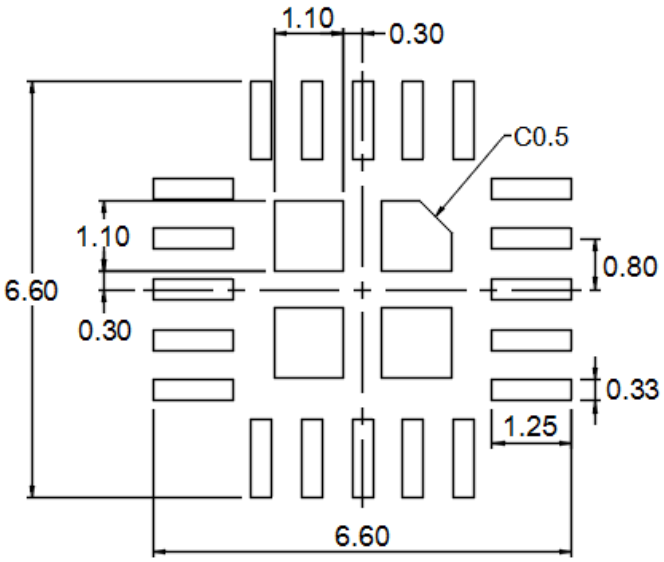


END VIEW

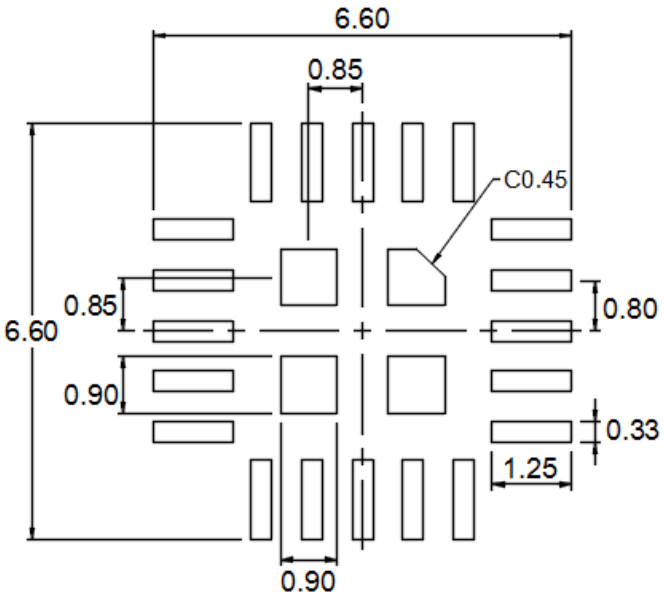
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	-	-	3.50
D	5.90	6.00	6.10
D1	2.70	2.80	2.90
E	5.90	6.00	6.10
E1	2.70	2.80	2.90
e	0.70	0.80	0.90
b	0.23	0.33	0.43
L	0.70	0.80	0.90
L1	0.05	0.15	0.25

LAND PATTERN REFERENCE:

Unit: mm



RECOMMENDED LAND PATTERN

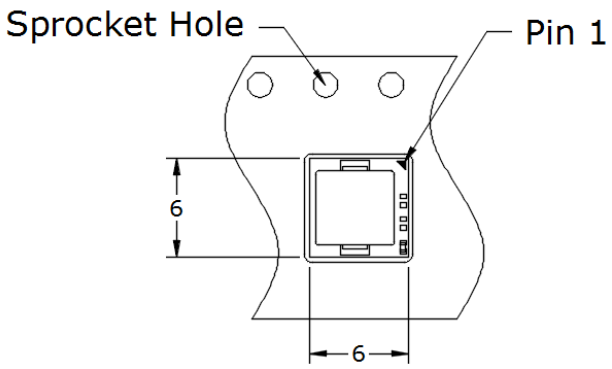


RECOMMENDED STENCIL PATTERN
BASED ON 0.1mm THICKNESS STENCIL

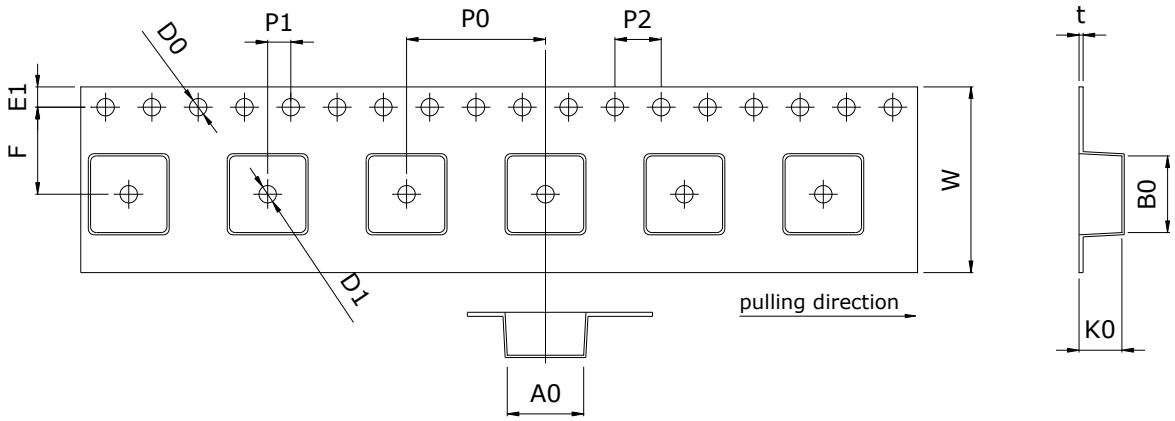
PACKING REFERENCE:

Unit: mm

Package In Tape Loading Orientation



Tape Dimension

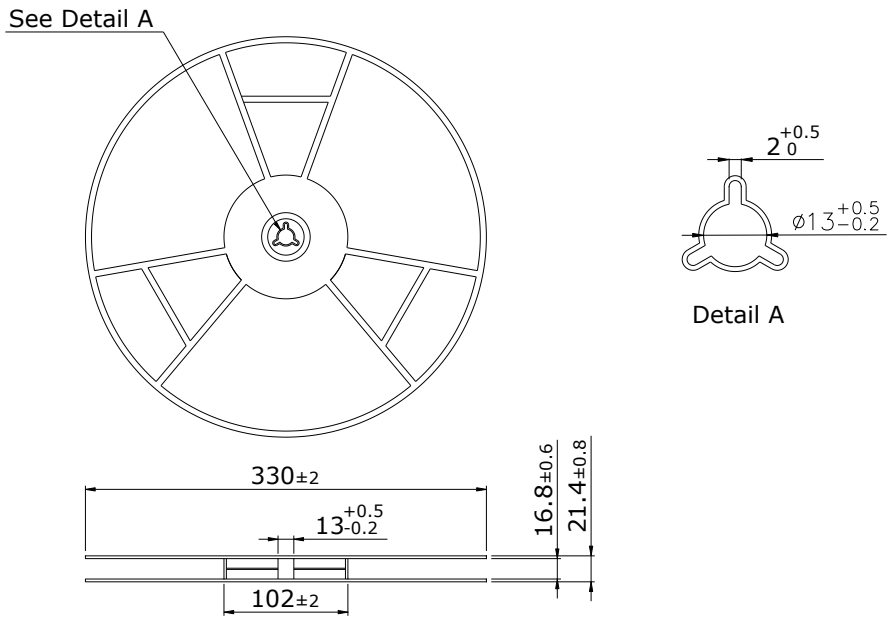


A0	6.60 ± 0.10	E1	1.75 ± 0.10
B0	6.60 ± 0.10	K0	3.70 ± 0.10
F	7.50 ± 0.10	P0	12.00 ± 0.10
W	16.00 ± 0.30	P1	2.00 ± 0.10
D0	φ1.5 +0.1/-0.0	P2	4.00 ± 0.10
D1	φ1.5 Min.	t	0.35 ± 0.05

PACKING REFERENCE: (Cont.)

Unit: mm

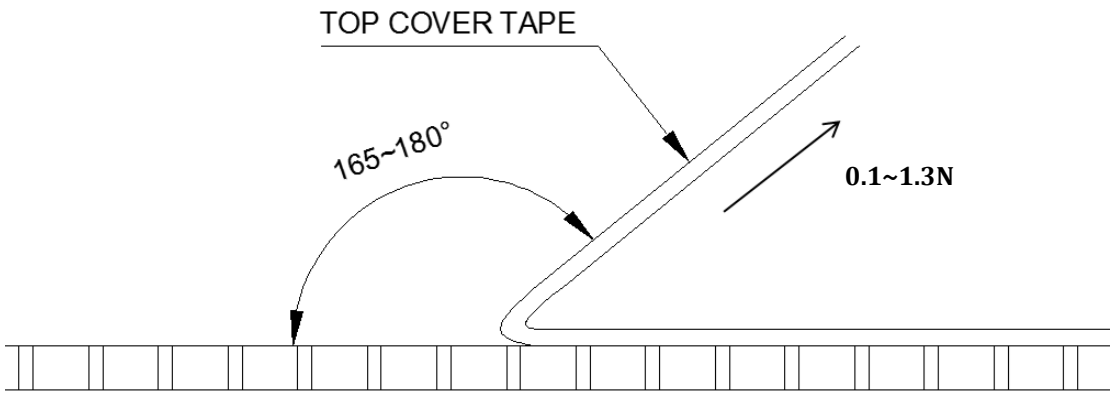
Reel Dimension



Peel Strength of Top Cover Tape

The peel speed shall be about 300mm/min.

The peel force of top cover tape shall between 0.1N to 1.3N



REVISION HISTORY:

Date	Revision	Changes
2018.03.29	P0	Release the preliminary specification
2018.04.18	P1	Modify Input Range ,Add Max Duty Cycle SPEC.
2018.10.01	P2	Error updated
2019.3.20	P3	Modify FB PIN Description & Page 16、Page19
2021.03.11	P4	Modify EN PIN Description & Absolute Maximum Ratings & Recommendation Layout Guide

单击下面可查看定价，库存，交付和生命周期等信息

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