

### FEATURES:

- High Power Density Power Module
- Typical Load: 20A for 0.6V ~ 2.5V
- Typical Load: 15A above 2.5V ~ 5.5V
- Input Voltage Range from 4.5V to 15V
- Output Voltage Range from 0.6V to 5.5V
- 96% Peak Efficiency at 12Vin to 5Vout
- Protections (Non-Latch OCP, UVP, UVLO, OTP and Latch-Off for OVP)
- Differential Output Voltage Remote Sense
- Programmable Soft-Start
- Pre-Biased Output
- Forced CCM Operation
- Power Good Indication
- Output Voltage Tracking
- Size 10.0mm x 9.0mm x 6.5mm
- Pb-free (RoHS compliant)
- MSL 3, 245°C Reflow

### APPLICATIONS:

- General Buck DC/DC Conversion
- DC Distributed Power System
- Telecom and Networking Equipments
- Servers System

### GENERAL DESCRIPTION:

The MSN12AD20-MQ is a high frequency, high power density and complete DC/DC power module. The PWM controller, power MOSFETs and most of support components are integrated in one hybrid package.

The features of MSN12AD20-MQ include constant-on-time (COT) control mode that provides fast transient response and eases loop stabilization. Besides, MSN12AD20-MQ is an easy to use DC/DC power module, it only needs input/output capacitors, one voltage dividing resistor, one over current protection resistor and one resistor of MODE pin to perform properly.

The low profile and compact size enables utilization of space on the bottom or top of PC boards either for highly density point of load regulation to save the space and area. It is suitable for automated assembly by standard surface mount equipment and complies with Pb-free and RoHS compliance.

### TYPICAL APPLICATION CIRCUIT & PACKAGE SIZE:

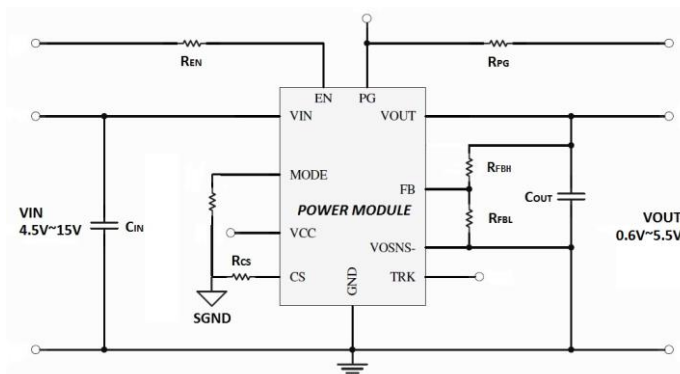


FIG.1 TYPICAL APPLICATION CIRCUIT

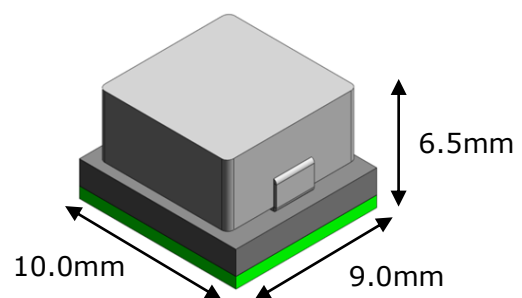


FIG.2 HIGH DENSITY POWER MODULE

## ORDER INFORMATION:

| Part Number  | Ambient Temp. Range (°C) | Package (Pb-Free) | MSL     | Note     |
|--------------|--------------------------|-------------------|---------|----------|
| MSN12AD20-MQ | -40 ~ +105               | LGA               | Level 3 | -        |
| Order Code   |                          | Packing           |         | Quantity |
| MSN12AD20-MQ |                          | Tray              |         | 800      |

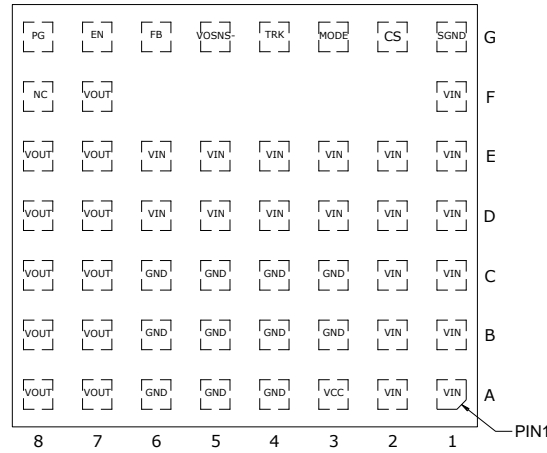
## ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures outside of warranty.

| Parameter                          | Description  | Min.       | Typ. | Max.    | Unit  |
|------------------------------------|--|------------|------|---------|-------|
| ■ Absolute Maximum Ratings         |  |            |      |         |       |
| VIN to GND                         | Continuous   | -          | -    | +18     | V     |
| SW to GND                          | Continuous   | -0.3       | -    | VIN+0.3 | V     |
| VCC to GND                         |  | -          | -    | +4.5    | V     |
| EN to GND                          | Continuous   | -          | -    | +4.5    | V     |
|                                    | Continuous, I <sub>EN</sub> <30uA                    | -          | -    | +16     | V     |
| All other pins to GND              |  | -0.3       | -    | +4.3    | V     |
| OCP Setting point                  | 0.6Vo~2.5Vo  | -          | -    | 23      | A     |
|                                    | Over 2.5Vo~5.5Vo                                     | -          | -    | 20      |       |
| Tc                                 | Operating case temperature                           | -          | -    | +120    | °C    |
| Tj                                 | Operating junction temperature                       | -40        | -    | +150    | °C    |
| Tstg                               | Storage temperature                                  | -40        | -    | +150    | °C    |
| ■ Thermal Information              |  |            |      |         |       |
| Rth(ja)                            | Thermal resistance from junction to ambient (note 1) | -          | 15   | -       | °C/W  |
| ■ Recommendation Operating Ratings |  |            |      |         |       |
| VIN                                | Input Supply Voltage                                 | +4.5       | -    | +15.0   | V     |
| VOUT                               | Adjusted Output Voltage                              | +0.6       | -    | +5.5    | V     |
| Ta                                 | Ambient Temperature                                  | -40        | -    | +105    | °C    |
| ■ Mean Time Between Failure        |  |            |      |         |       |
| MTBF                               | 12V to 5V@15A, Ta=40°C                               | 22,997,956 |      |         | Hours |

### NOTES:

- The test board size is 80mm×80mm×1.6mm with 4 layers, 2oz per layer, on 0 LFM condition.  
The test condition is complied with JEDEC EIJ/JESD 51 Standards.

**PIN CONFIGURATION:**

**TOP VIEW**
**PIN DESCRIPTION:**

| Symbol | Pin No.                         | Description   |
|--------|---------------------------------|---|
| VIN    | A1,2;B1,2;C1,2;<br>D1~6;E1~6;F1 | Power input pin. It needs to be connected to input rail. It also needs to be connected to thermal dissipation layer by vias connection.   |
| VCC    | A3                              | Internal 3V LDO output. The driver and control circuits are powered from the VCC voltage.   |
| GND    | A4~6;B3~6;<br>C3~6              | System ground. All voltage levels are referenced to the pins. All pins should be connected together with a ground plane   |
| VOUT   | A7,8;B7,8;C7,8;<br>D7,8;E7,8;F7 | Power output pin. It needs to be connected to output rail. It also needs to be connected to thermal dissipation layer by vias connection.   |
| NC     | F8                              | No connect.   |
| SGND   | G1                              | Analog ground. Select SGND as the control circuit reference point.  |
| CS     | G2                              | Current limit. Connect a resistor to ground to set the current limit trip point.  |
| MODE   | G3                              | Connect MODE pin to SGND by 60.4kΩ Resistance   |
| TRK    | G4                              | External tracking voltage input. The input signal of this pin is the tracking reference for the module output voltage.<br>Soft-start purpose: place a decoupling ceramic capacitor between TRK and VOSNS- as close to the module as possible. The capacitance of this capacitor determines the soft start time. |
| VOSNS- | G5                              | Remote sense negative input. Connect VOSNS- to the negative side of the voltage sense point directly. Short VOSNS- to GND if the remote sense is not used.  |
| FB     | G6                              | Feedback. Connect a resistor between this pin and VOSNS- for adjusting output voltage. Place this resistor as closely as possible to this pin and VOSNS-.   |
| EN     | G7                              | Enable – to pull the pin higher than 1.22V<br>Disable – to pull the pin lower than 0.8V   |
| PG     | G8                              | Power good output. PG is an open-drain signal. A pull-up resistor connected to VCC to indicate a logic high signal if the output voltage is within regulation.  |

**ELECTRICAL SPECIFICATIONS:**

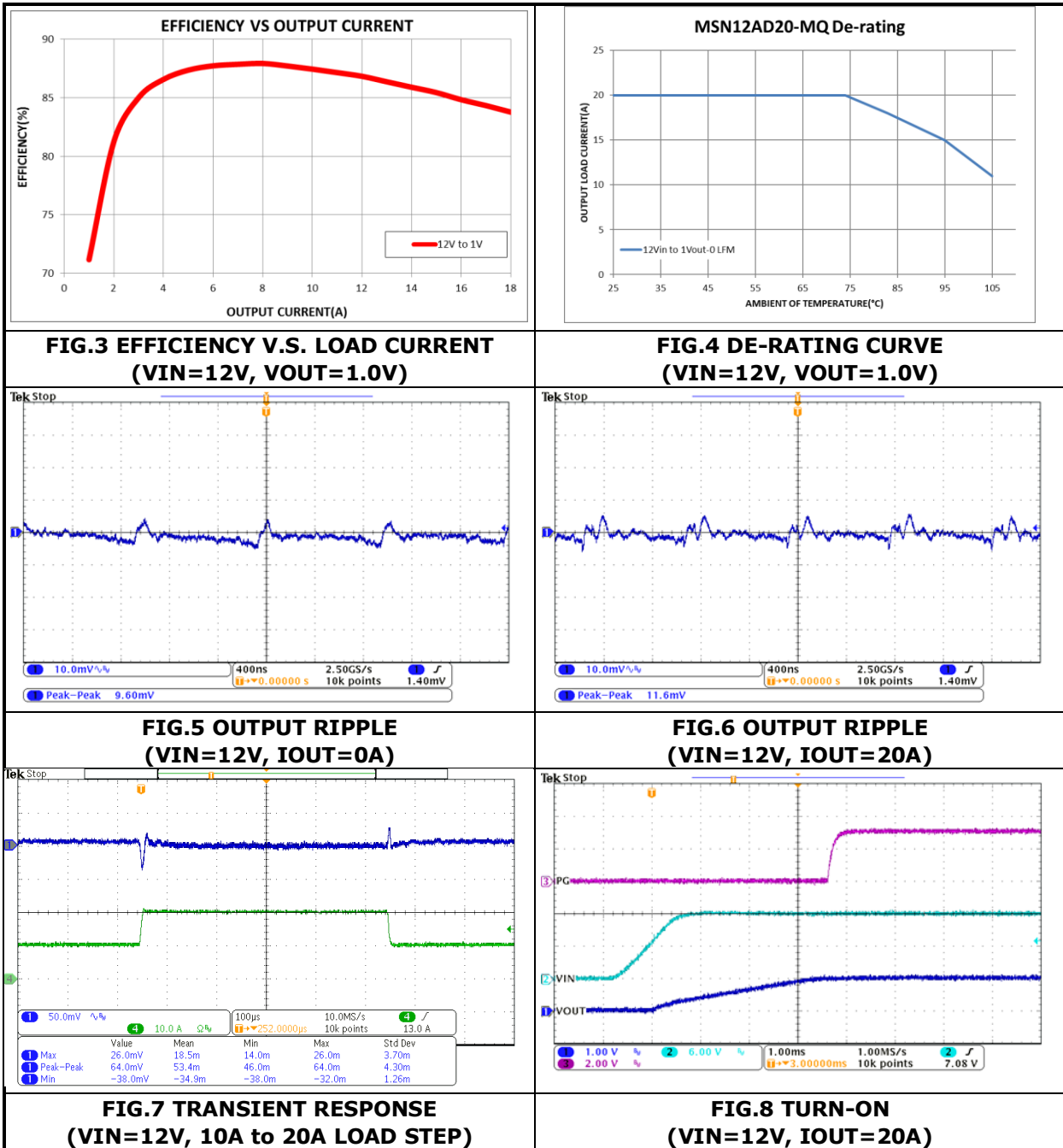
Conditions:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified. Test Board Information: 80mm×80mm×1.6mm, 4 layers 2 oz. The output ripple and transient response measurement is short loop probing and 20MHz bandwidth limited.  $C_{in} = 22\mu\text{F}/25\text{V}/1210/\text{X7R}$  MLCC \* 3 pcs,  $C_{out} = 47\mu\text{F}/6.3\text{V}/1210/\text{X7R}$  MLCC \* 3 pcs + Low ESR POScap 330uF (6TPE330MIL).

| Symbol                              | Parameter                          | Conditions   | Min.          | Typ. | Max.  | Unit             |
|-------------------------------------|------------------------------------|--|---------------|------|-------|------------------|
| <b>■ Input Characteristics</b>      |                                    |  |               |      |       |                  |
| $I_{in(VIN)}$                       | Input supply bias current          | $V_{in}=12\text{V}$ , $V_{out}=1.8\text{V}$ , $I_{out}=0\text{A}$ , 1MHz                               | -             | 35   | -     | mA               |
| $I_{S(VIN)}$                        | Input supply current               | $V_{in}=12\text{V}$ , $V_{out}=1.8\text{V}$ , $I_{out}=18\text{A}$ , 1MHz                              | -             | 3    | -     | A                |
| <b>■ Output Characteristics</b>     |                                    |  |               |      |       |                  |
| $I_{OUT(DC)}$                       | Output continuous current range    | $V_{in}=12\text{V}$ , $V_{out}=0.6\sim 2.5\text{V}$  | 0             | -    | 20    | A                |
|                                     |                                    | $V_{in}=12\text{V}$ , $V_{out}=\text{Over } 2.5\text{V}\sim 5.5\text{V}$                               | 0             | -    | 15    |                  |
| $\Delta V_{OUT}/\Delta V_{IN}$      | Line regulation                    | $V_{in}=4.5\text{V}$ to 15V, $V_{out}=1.8\text{V}$ , $I_{out}=20\text{A}$                              | -             | 0.5  | -     | %                |
| $\Delta V_{OUT}/\Delta I_O$         | Load regulation                    | $V_{in}=12\text{V}$ , $V_{out}=1.8\text{V}$ , $I_{out}=0\sim 20\text{A}$                               | -             | 0.5  | -     | %                |
| $V_{O, set}$                        | Output voltage set point           | $V_{in}=12\text{V}$ , $V_{out}=1.8\text{V}$ with 0.1% resistor   | -1.0          | -    | +1.0  | % $V_{O, set}$   |
| $F_{SW}$                            | Switching Frequency                | MODE connect a 60.4K $\Omega$ to SGND  | 850           | 1050 | 1250  | KHz              |
| $V_{CC}$                            | VCC regulator                      |  | -             | 3.0  | -     | V                |
| <b>■ Enable Signal</b>              |                                    |  |               |      |       |                  |
| $V_{ENABLE}$                        | Logic high Voltage                 | Module On  | 1.17          | 1.22 | 1.27  | V                |
|                                     | Logic low Voltage                  | Module Off   | -             | -    | 0.8   | V                |
| $V_{EN-HYS}$                        | Enable hysteresis                  |  | -             | 0.2  | -     | V                |
| <b>■ Power Good</b>                 |                                    |  |               |      |       |                  |
| $V_{PGH}$                           | Power good high threshold          | FB Voltage   | >96%          | -    | <110% | $V_{REF}$        |
| $V_{PGL}$                           | Power good low threshold           | FB Voltage   | <88%          | -    | >120% |                  |
| $V_{PG}$                            | Power good sink current capability | $I_{PG} = 1\text{mA}$  | -             | -    | 0.8   | V                |
| $PG_{TD}$                           | Power good low to high delay       | After $V_{REF}$ rise > 95%   | -             | 0.9  | -     | mS               |
| <b>■ Protection Characteristics</b> |                                    |  |               |      |       |                  |
| OVP                                 | Output over voltage protection     |  | -             | 116% | -     | $V_{REF}$        |
| UVP                                 | Output under voltage protection    |  | -             | 80%  | -     |                  |
| $T_{SD}$                            | Thermal shutdown temperature       |  | -             | 160  | -     | $^\circ\text{C}$ |
| $T_{SD-HY}$                         | Thermal shutdown hysteresis        |  | -             | 30   | -     | $^\circ\text{C}$ |
| OCP                                 | Recommend over current protection  | $V_{in}=12\text{V}$ , $V_{out}=0.6\text{V}\sim 2.5\text{V}$ , $R_{cs}=5.23\text{K}\Omega//47\text{pF}$ | 21.5          | -    | 24.5  | A                |
|                                     |                                    | $V_{in}=12\text{V}$ , $V_{out}=3.3\text{V}\sim 5.5\text{V}$ , $R_{cs}=6.8\text{K}\Omega//47\text{pF}$  | 18            | -    | 21    | A                |
| SCP                                 | Short current protection           |  | Auto-recovery |      |       |                  |

## TYPICAL PERFORMANCE CHARACTERISTICS: (VOUT=1.0V)

Conditions:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified. Test Board Information: 80mm×80mm×1.6mm, 4 layers 2 oz. The output ripple and transient response measurement is short loop probing and 20MHz bandwidth limited.  $C_{in} = 22\mu\text{F}/25\text{V}/1210/\text{X7R}$  MLCC \* 3 pcs,  $C_{out} = 47\mu\text{F}/6.3\text{V}/1210/\text{X7R}$  MLCC \* 3 pcs + Low ESR POScap 330uF (6TPE330MIL).

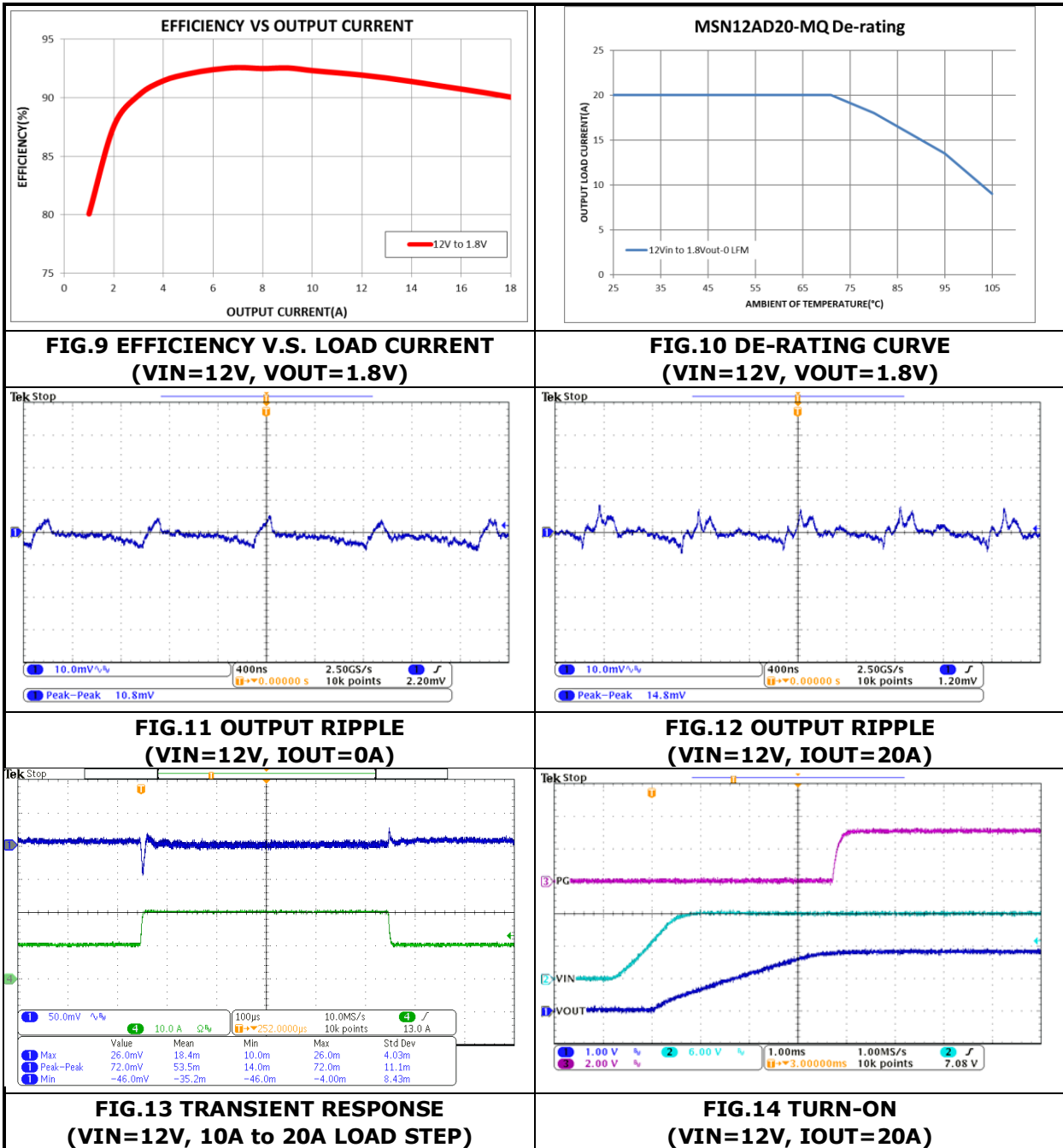
The following figures provide the typical characteristic curves at 1.0Vout.



## TYPICAL PERFORMANCE CHARACTERISTICS: (VOUT=1.8V)

Conditions:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified. Test Board Information: 80mm×80mm×1.6mm, 4 layers 2 oz. The output ripple and transient response measurement is short loop probing and 20MHz bandwidth limited.  $C_{in} = 22\mu\text{F}/25\text{V}/1210/\text{X7R}$  MLCC \* 3 pcs,  $C_{out} = 47\mu\text{F}/6.3\text{V}/1210/\text{X7R}$  MLCC \* 3 pcs + Low ESR POScap 330uF (6TPE330MIL).

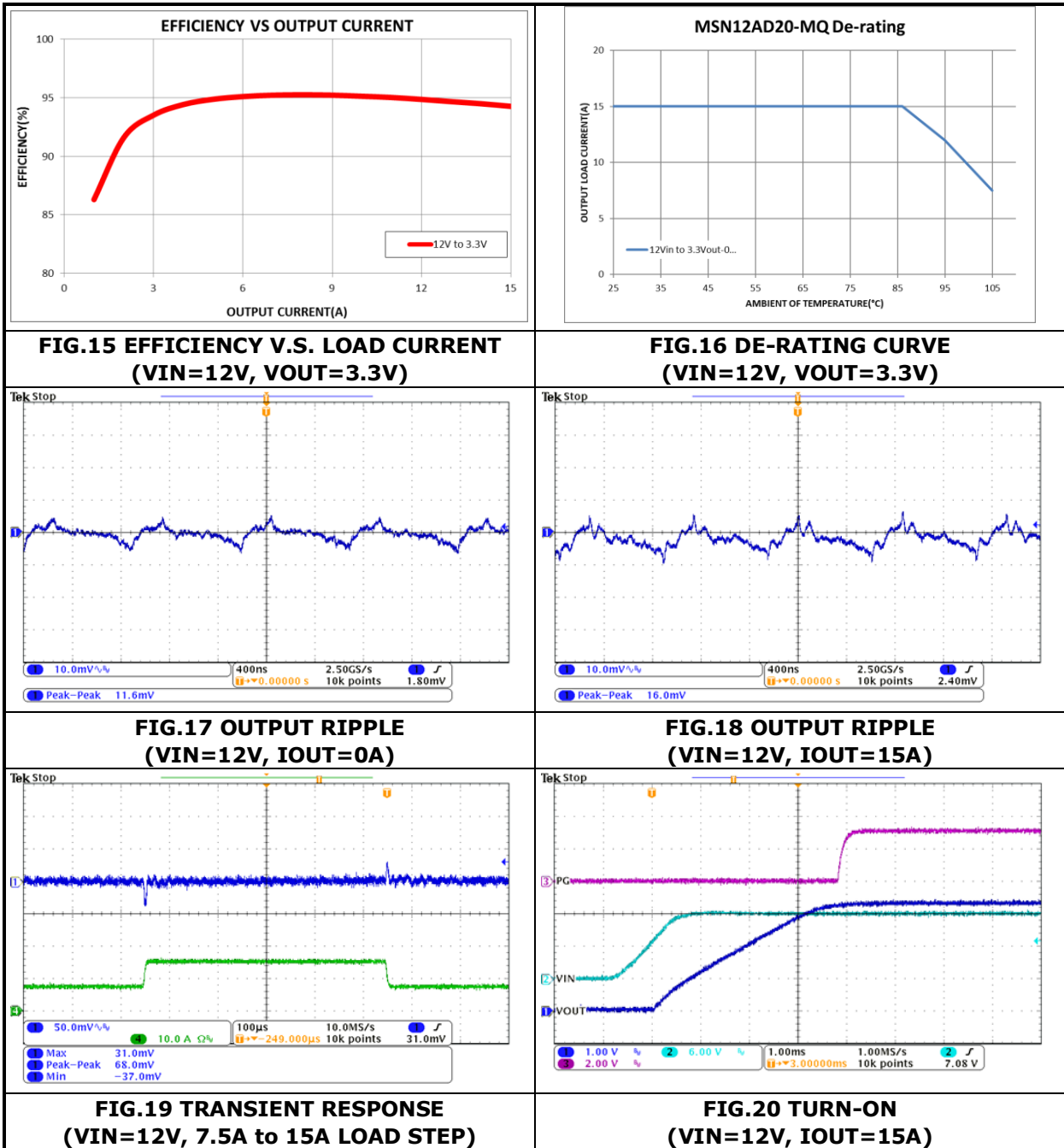
The following figures provide the typical characteristic curves at 1.8Vout.



## TYPICAL PERFORMANCE CHARACTERISTICS: (VOUT=3.3V)

Conditions:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified. Test Board Information: 80mm×80mm×1.6mm, 4 layers 2 oz. The output ripple and transient response measurement is short loop probing and 20MHz bandwidth limited.  $C_{in} = 22\mu\text{F}/25\text{V}/1210/\text{X7R}$  MLCC \* 3 pcs,  $C_{out} = 47\mu\text{F}/6.3\text{V}/1210/\text{X7R}$  MLCC \* 3 pcs + Low ESR POScap 330uF (6TPE330MIL).

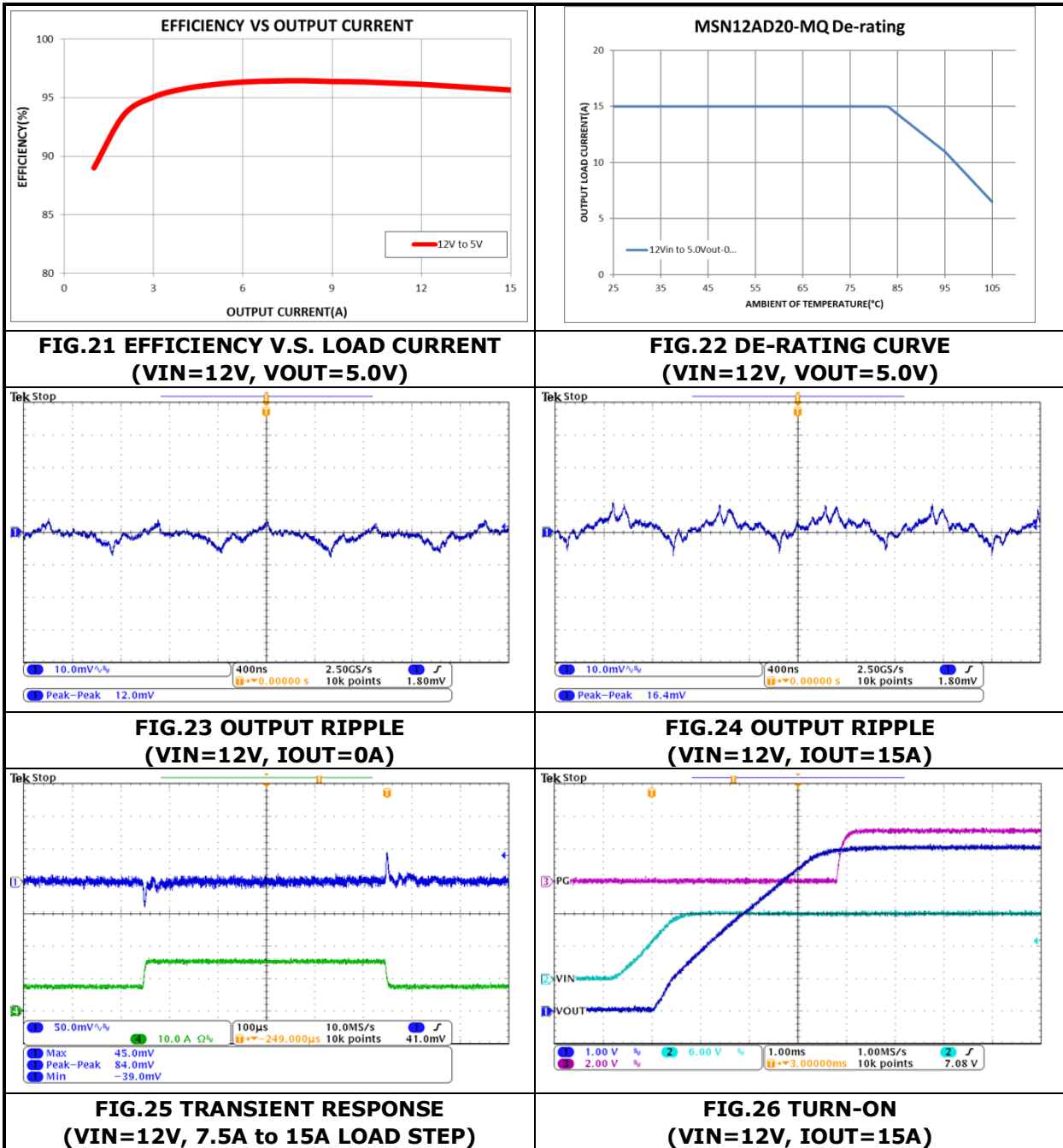
The following figures provide the typical characteristic curves at 3.3Vout.



## TYPICAL PERFORMANCE CHARACTERISTICS: (VOUT=5.0V)

Conditions:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified. Test Board Information: 80mm×80mm×1.6mm, 4 layers 2 oz. The output ripple and transient response measurement is short loop probing and 20MHz bandwidth limited.  $C_{in} = 22\mu\text{F}/25\text{V}/1210/\text{X7R}$  MLCC \* 3 pcs,  $C_{out} = 47\mu\text{F}/6.3\text{V}/1210/\text{X7R}$  MLCC \* 3 pcs + Low ESR POScap 330uF (6TPE330MIL).

The following figures provide the typical characteristic curves at 5Vout.





**APPLICATIONS INFORMATION:**
**SAFETY CONSIDERATION:**

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Fuses should also be used when there is the possibility of sustained input voltage reversal which is not current limited. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line. The installer must observe all relevant safety standards and regulations. For safety agency approvals, install the converter in compliance with the end-user safety standard.

**INPUT FILTERING:**

The module should be connected to as low AC impedance source supply and a highly inductive source or line inductance can affect the stability of the module. An input capacitor must be placed directly to the input pin of the module, to minimize input ripple voltage and ensure module stability.

**OUTPUT FILTERING:**

To reduce output ripple and improve the dynamic response to as step load change, the additional capacitor at the output must be used. Low ESR polymer and ceramic capacitors are recommended to improve the output ripple and dynamic response of the module.

**OUTPUT VOLTAGE PROGRAMMING:**

The Module has an internal 0.6V reference voltage, The output voltage can be programmed by the dividing resistor  $R_{FBH}$  and  $R_{FBL}$ , and division resistor needs to be closed as possible to the VOUT pin, FB pin and VOSNS- pin. A value of between 100Ω and 3.4kΩ is highly recommended for both resistors. Assume  $R_{FBH}$  set 976 ohm, The output voltage can be calculated as shown in Equation 1 and the resistance according to typical output voltage is shown in TABLE 1.

$$V_{OUT} = 0.6 \times \left( 1 + \frac{R_{RBH}}{R_{FBL}} \right) \quad (EQ.1)$$

| VOUT       | 1.0V | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | 5V  |
|------------|------|------|------|------|------|------|-----|
| Rtrim(ohm) | 1470 | 976  | 649  | 487  | 309  | 215  | 133 |

**TABLE 1**
**SOFT START TIME PROGRAMMING:**

The minimum soft-start time is limited at 3ms. It can be increased by adding a SS capacitor between TRK pin and VOSNS- pin. The total SS capacitor value can be determined with Equation 2:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times 36(\mu A)}{0.6(V)} - 220nF \quad (EQ.2)$$

**OUTPUT VOLTAGE TRACKING AND REFERENCE:**

The Module provides an analog input pin (TRK) to track another power supply or accept an external reference. When an external voltage signal is connected to TRK, it acts as a reference for the Module output voltage. The FB voltage follows this external voltage signal exactly, and the soft-start settings are ignored. The TRK input signal can be in the range of 0.3V to 1.4V. During the initial start-up, the TRK must reach at least 600mV first to ensure proper operation. After that, it can be set to any value between 0.3V and 1.4V.

**APPLICATIONS INFORMATION : (Cont.)**
**POWER GOOD (PG):**

The Module has a power good (PG) output. PG is the open-drain of a MOSFET. Connect PG to VCC or another external voltage source less than 3.6V through a pull-up resistor (typically 10kΩ). After applying the input voltage, the MOSFET turns on, so PG is pulled to GND before soft-start is ready. After the FB voltage reaches 96% of the REF voltage, PG is pulled high after a 0.8ms delay.

When the FB voltage drops to 80% of the REF voltage, or exceeds 116% of the nominal REF voltage, PG is latched low. PG can only be pulled high again after a new soft start.

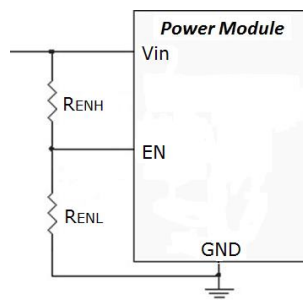
If the input supply fails to power the Module, PG is clamped low, even though PG is tied to an external DC source through a pull-up resistor.

**UVLO (ENABLE) PROGRAMMING:**

The Module turns on when EN goes high; the Module turns off when EN goes low. EN cannot be left floating for proper operation.

As FIG.27, EN can be connected a resistor divider from VIN to AGND used to program the input voltage (UVLO thresholds). RENH and RENL should be chosen that VEN doesn't exceed 3.6V when VIN reaches the maximum value. The resistor divider values can be determined with Equation 3:

$$V_{UVLO} = 1.22V \times \frac{R_{ENH} + R_{ENL}}{R_{ENL}} \quad (\text{EQ.3})$$



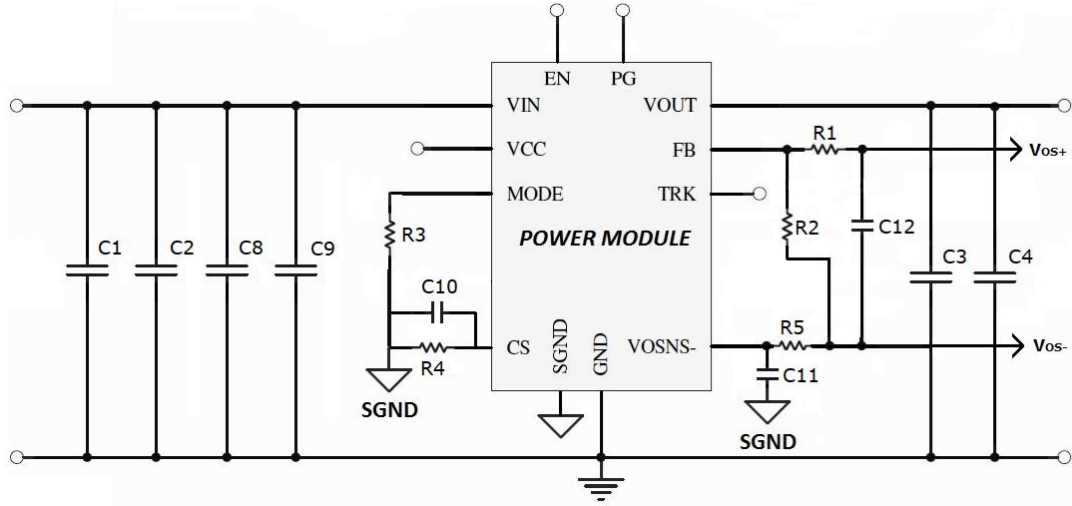
**FIG.27 PROGRAM EN CIRCUIT(UVLO SETTING)**

When only RENH is connected to Vin without RENL, then RENH should be chosen so that the maximum current going to EN is 30μA, RENH can be calculated with Equation 4:

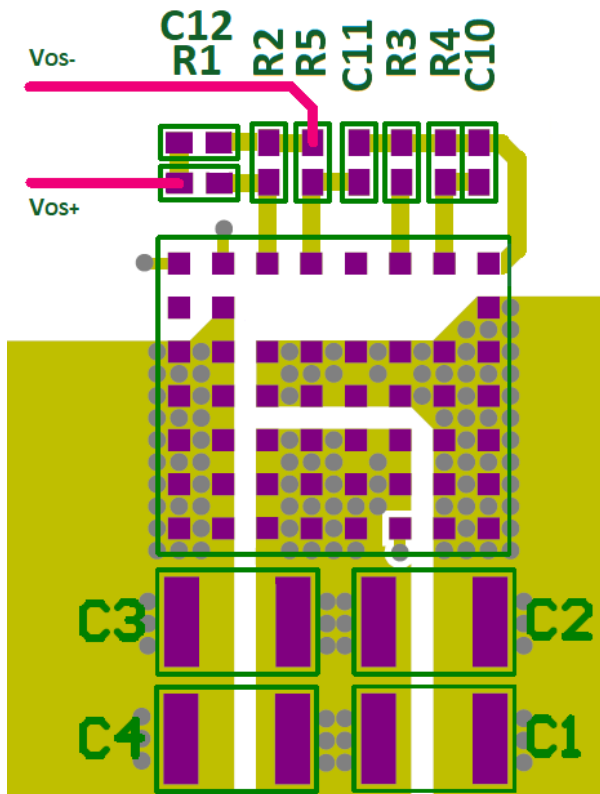
$$R_{ENH} (K\Omega) = \frac{V_{IN-MAX} (V)}{0.03(mA)} \quad (\text{EQ.4})$$

## APPLICATIONS INFORMATION : (Cont.)

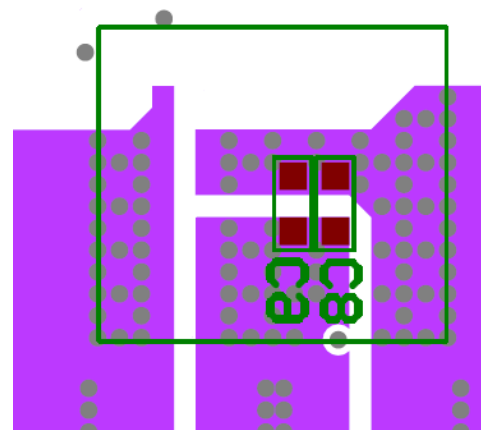
### RECOMMENDATION LAYOUT GUIDE:



**FIG.28 LAYOUT GUIDE SCHEMATIC**



**FIG.29 TOP LAYER**



**FIG.30 BOTTOM LAYER**

**APPLICATIONS INFORMATION : (Cont.)****RECOMMENDATION ON LAYOUT: (Cont.)**

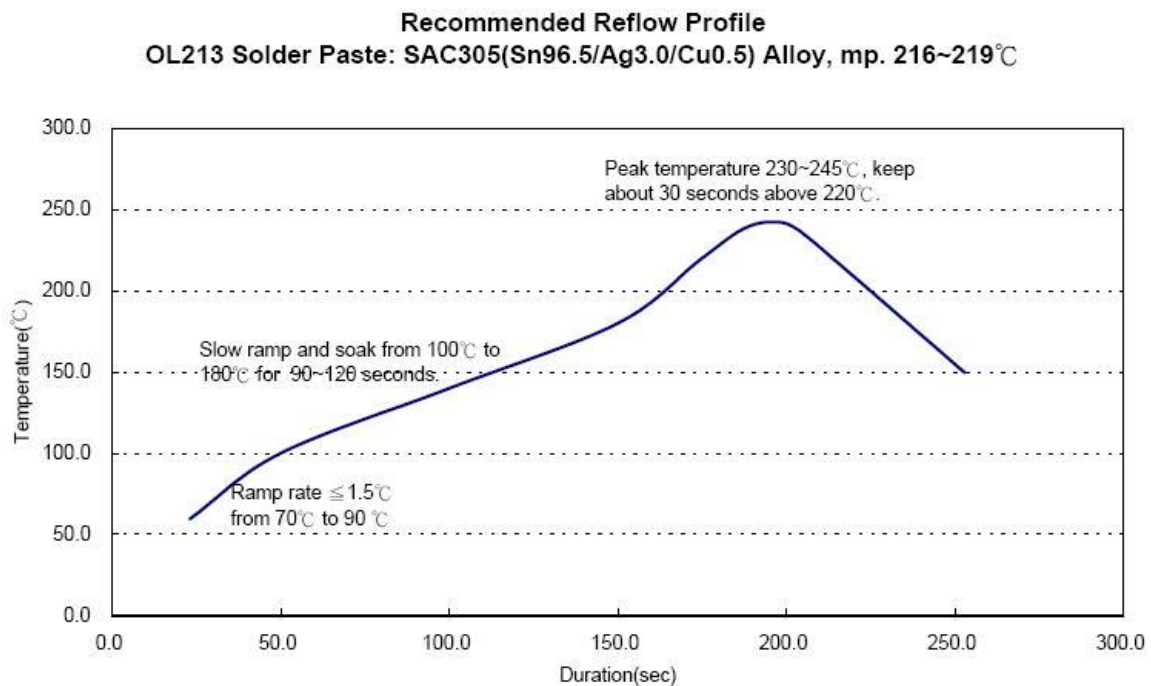
- 1、 Place the FB components R1(RFBH) · R2(RFBL) close to the module, so that the FB trace can be minimized to offer less noise coupling.
- 2、 For lower noise coupling of the differential output voltage remote sense function, an C filter (C12-100pF) must be in place between Vos+ and Vos-, an R-C filter (R5-2ohm, C11-100pF) must be in place within the path of Vos-, VOSNS- and SGND. Refer to Fig.28 for the exact circuitry
- 3、 SGND and PGND don't need connected together, because already connect at inside of power module.
- 4、 OCP point setting resistor R4 must be connected with a MLCC C10 (47pF) in parallel.
- 5、 MLCC input decoupling capacitors C8 and C9 (1uF and 100pF) are required to be placed on the bottom side of the PCB connecting pin VIN and pin PGND (refer to Fig. 30)

**THERMAL CONSIDERATIONS:**

All of thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 80mm×80mm×1.6mm with 4 layers on 0 LFM condition. The Module is designed for using when the case temperature is below 120°C regardless the change of output current, input/output voltage or ambient temperature.

**APPLICATIONS INFORMATION : (Cont.)**
**REFLOW PARAMETERS:**

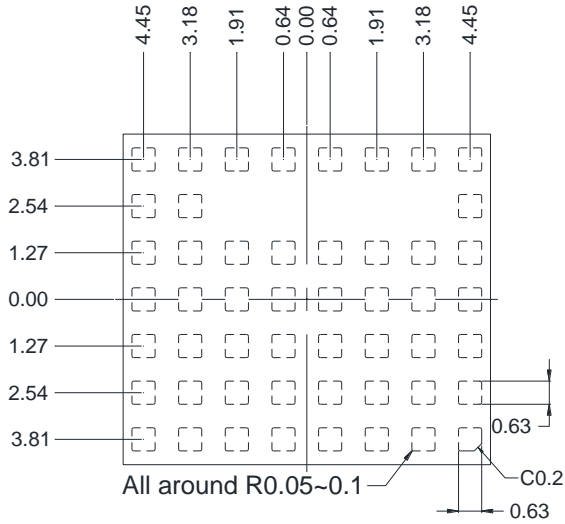
Lead-free soldering process is a standard of making electronic products. Many solder alloys like Sn/Ag, Sn/Ag/Cu, Sn/Ag/Bi and so on are used extensively to replace traditional Sn/Pb alloy. Here the Sn/Ag/Cu alloy (SAC) are recommended for process. In the SAC alloy series, SAC305 is a very popular solder alloy which contains 3% Ag and 0.5% Cu. It is easy to get it. FIG.31 shows an example of reflow profile diagram. Typically, the profile has three stages. During the initial stage from 70°C to 90°C, the ramp rate of temperature should be not more than 1.5°C/sec. The soak zone then occurs from 100°C to 180°C and should last for 90 to 120 seconds. Finally the temperature rises to 230°C to 245°C and cover 220°C in 30 seconds to melt the solder. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and user could switch to optimize the profile according to various solder type and various manufactures' formula.


**FIG.31 RECOMMENDATION REFLOW PROFILE**

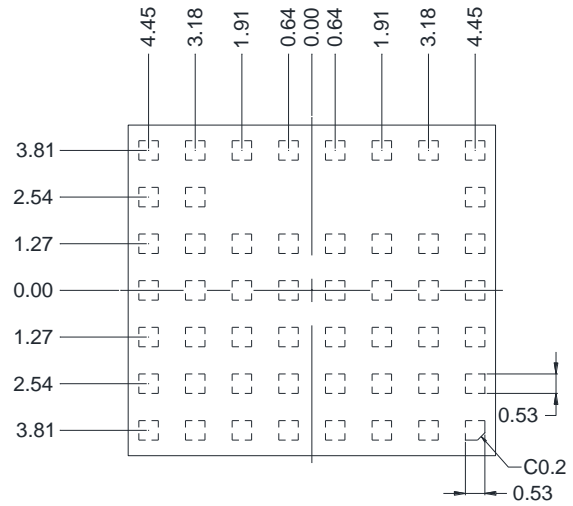
## LAND PATTERN REFERENCE:

Unit: mm

General Tolerances:  $\pm 0.2$ mm



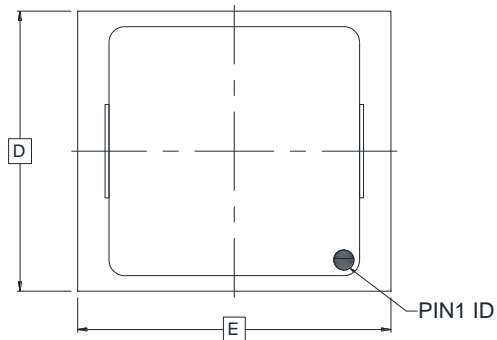
**TOP VIEW**  
**TYPICAL RECOMMENDED**  
**LAND PATTERN**



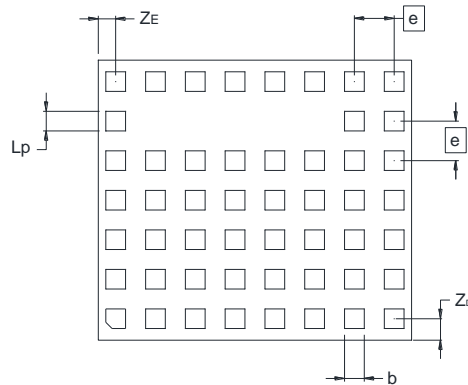
**TOP VIEW**  
**STENCIL PATTERN**  
**WITH PADS (STENCIL  $t=120 \mu\text{m}$ )**

**PACKAGE OUTLINE DRAWING:**

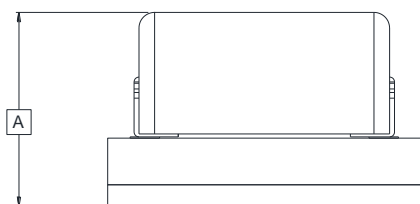
Unit: mm  
 General Tolerances: ±0.2mm



Top View



Bottom View

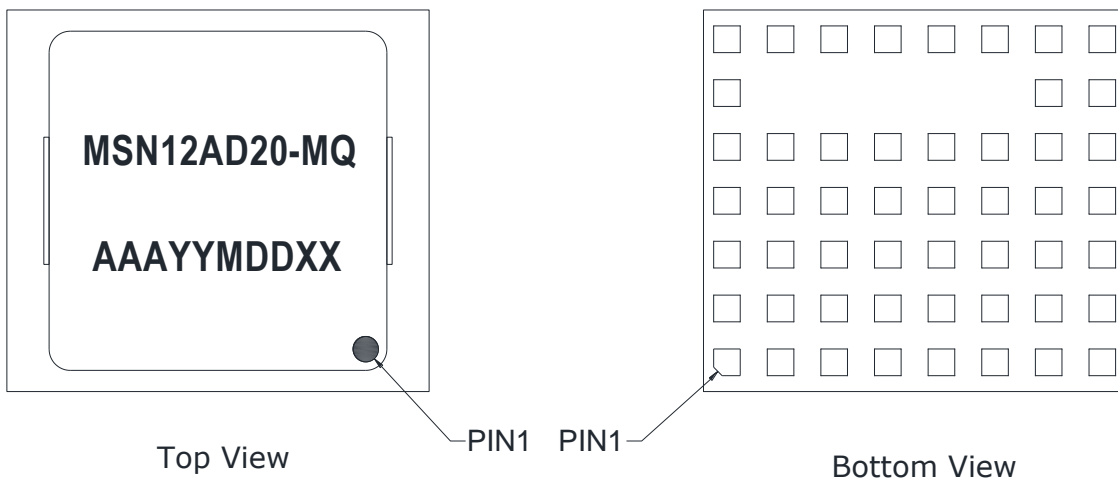


Side View

| DIM | MILLIMETERS |       |       |
|-----|-------------|-------|-------|
|     | MIN         | NOM   | MAX   |
| A   | -           | -     | 6.5   |
| D   | 8.8         | 9.0   | 9.2   |
| E   | 9.80        | 10    | 10.2  |
| e   | 1.22        | 1.27  | 1.32  |
| Zb  | 0.59        | 0.69  | 0.79  |
| ZE  | 0.455       | 0.555 | 0.655 |
| Lp  | 0.58        | 0.63  | 0.68  |
| b   | 0.58        | 0.63  | 0.68  |

## MARKING REFERENCE:

Unit: mm  
General Tolerances:  $\pm 0.2\text{mm}$



### Marking note:

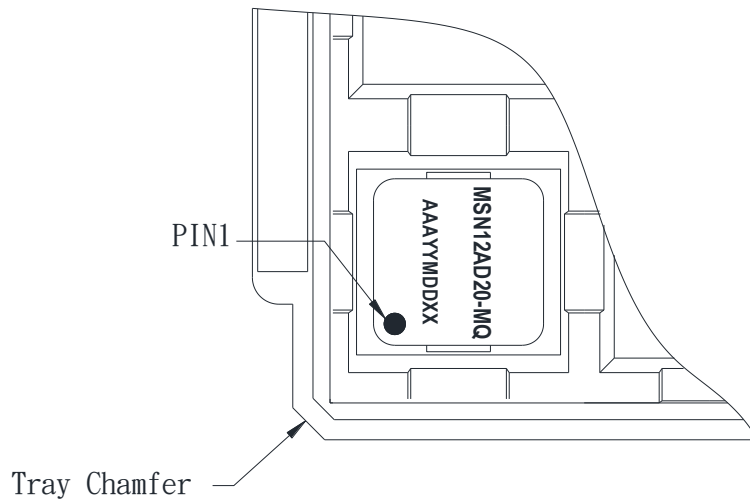
1. Circle represents the fiducial point of SMT
2. MSN12AD20-MQ represents the Product Name
3. AAAYYMDDXX represents the Lot Number



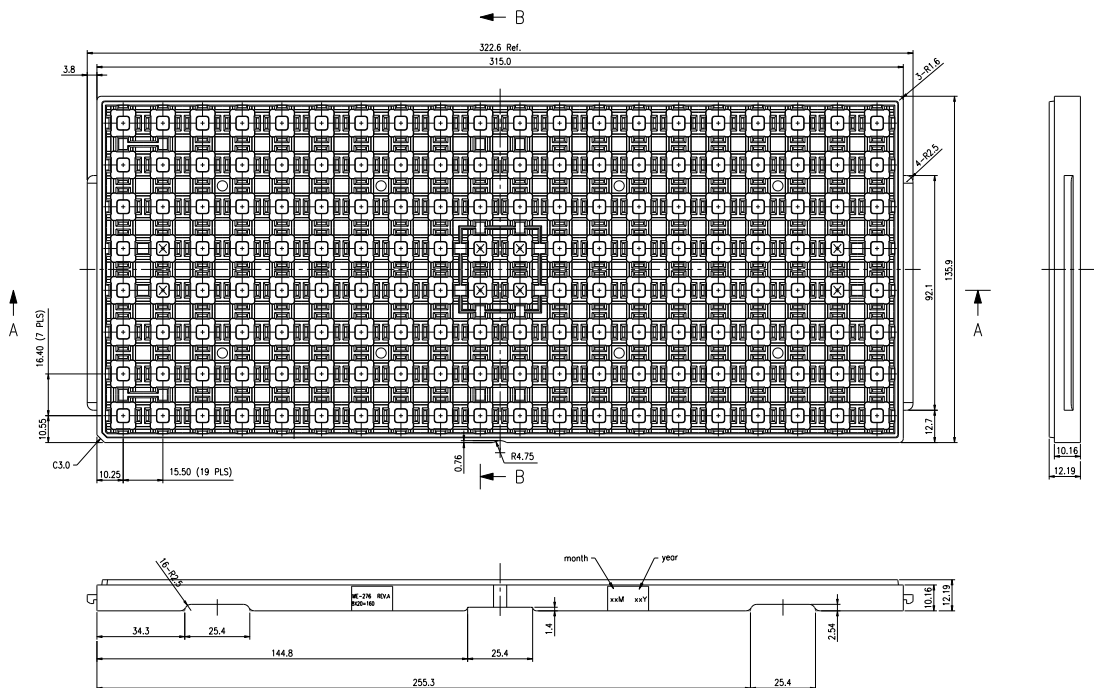
## PACKING INFORMATION:

Unit: mm

### Tray Packing



### PACKAGE IN TRAY LOADING ORIENTATION



### TRAY DIMENSION

**REVISION HISTORY:**

| <b>Date</b> | <b>Revision</b> | <b>Changes</b>  |
|-------------|-----------------|---|
| 2017.07.10  | 00              | Release the preliminary datasheet.  |
| 2017.10.13  | 01              | <ul style="list-style-type: none"> <li>1 · Change module no. from MMN12AD20-MQ to MSN12AD20-MQ</li> <li>2 · Change page 1 height of module outline from typical 6.4mm to maximum 6.5mm</li> <li>3 · Add page 2 thermal information</li> <li>4 · Add page 5 Functional block diagram</li> <li>5 · Update Page 6~9 performance characteristic</li> </ul>  |
| 2018.03.05  | 02              | <ul style="list-style-type: none"> <li>1 · Update Page 1 typical application circuit and forced CCM 600KHz fixed operation</li> <li>2 · Remove page 5 Functional block diagram</li> <li>2 · Update Page 5~9 electrical Specifications</li> <li>3 · Add Page 10~14 applications information</li> </ul>   |
| 2018.05.14  | 03              | <ul style="list-style-type: none"> <li>1 · Update switching frequency from 600kHz to 1MHz</li> <li>2 · Update Vin and Vout range</li> <li>3 · Remote VOSNS+ pin</li> <li>4 · Update page 5~10 electrical Specification</li> <li>5 · Update page 6~13 application information</li> </ul>   |
| 2018.08.13  | 04              | <ul style="list-style-type: none"> <li>1 · Update maximum output current from 20A to 15A or 18A</li> <li>2 · Update operation temperature from -40°C to -5°C</li> <li>3 · Add layout guide</li> <li>4 · Add package outline drawing</li> <li>5 · Add land pattern reference</li> <li>6 · Add marking Drawing</li> <li>7 · Add package information</li> </ul>  |
| 2018.11.14  | 05              | <ul style="list-style-type: none"> <li>1 · Update page 13 · 14 pin 1 of bottom view</li> </ul>  |
| 2018.12.28  | 06              | <ul style="list-style-type: none"> <li>1 · Update page 2 Ambient Temp. Range from -5 to -40 °C</li> <li>2 · Update page 15 marking reference information</li> </ul>   |
| 2019.03.29  | 07              | <ul style="list-style-type: none"> <li>1 · Update page 14 pad information of bottom view</li> </ul>   |
| 2019.04.09  | 08              | <ul style="list-style-type: none"> <li>1 · Update page 2 OCP setting point</li> <li>2 · Update page 3 pin description of SGND</li> <li>3 · Add page 11 layout guide schematic</li> <li>4 · Update page 11 layout guide of top and bottom layer</li> <li>5 · Update page 12 recommendation information of layout</li> </ul>  |
| 2019.07.01  | 09              | <ul style="list-style-type: none"> <li>1 · Update page 1 0.6V~2.5V load current from 18A to 20A</li> <li>2 · Update page 2 Ambient Temp. Range from 85 to 105 °C</li> <li>3 · Page 2 packing transfer to tray from tape &amp; reel and quantity update to 800 pcs from 1000 pcs</li> <li>4 · Update page 2 Tj and Tstg maximum from 125°C to 150°C</li> <li>5 · Add page 2 MTBF information</li> <li>6 · Update page 11 and 12 information about layout guide</li> <li>7 · Add page 17 packing information</li> <li>8 · Updated page 2 Rth(jchoke-a) to Rth(jc)</li> <li>9 · Update page 14 stencil pattern with square pads to stencil pattern with pads.</li> </ul> |
| 2020.07.13  | 10              | <ul style="list-style-type: none"> <li>1 · Update page 2 Rth(ja)</li> </ul>   |

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[>>CYNTEC\(乾坤科技\)](#)