

COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(on)}$	I_D $T_A = +25^\circ C$
Q1	30V	60mΩ @ $V_{GS} = 10V$	3.4A
		100mΩ @ $V_{GS} = 4.5V$	2.7A
Q2	-30V	95mΩ @ $V_{GS} = -10V$	-2.8A
		140mΩ @ $V_{GS} = -4.5V$	-2.3A

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

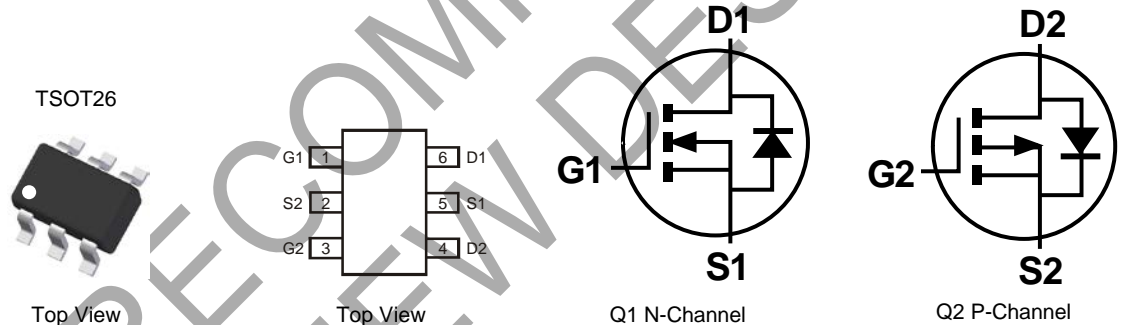
Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(on)}$) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

- Backlighting
- DC-DC Converters
- Power Management Functions

Mechanical Data

- Case: TSOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish—Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.013 grams (Approximate)

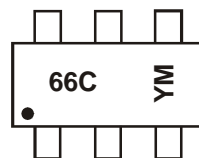


Ordering Information (Note 3)

Part Number	Case	Packaging
DMG6602SVT-7	TSOT26	3000 / Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



66C = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: X = 2010)
 M = Month (ex: 9 = September)

Date Code Key

Year	2010	2011	2012	2013	2014	2015	2016	2017
Code	X	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings – Q1 (@TA = +25°C unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	30	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current (Note 6) V _{GS} = 10V	Steady State	T _A = +25°C	I _D	3.4	A
		T _A = +70°C		2.7	
Continuous Drain Current (Note 6) V _{GS} = 4.5V	Steady State	T _A = +25°C	I _D	2.7	A
		T _A = +70°C		2.2	
Maximum Continuous Body Diode Forward Current (Note 6)			I _S	1.5	A
Pulsed Drain Current (Note 6)			I _{DM}	25	A

Maximum Ratings – Q2 (@TA = +25°C unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	-30	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current (Note 6) V _{GS} = -10V	Steady State	T _A = +25°C	I _D	-2.8	A
		T _A = +70°C		-2.4	
Continuous Drain Current (Note 6) V _{GS} = -4.5V	Steady State	T _A = +25°C	I _D	-2.3	A
		T _A = +70°C		-2.1	
Maximum Continuous Body Diode Forward Current (Note 6)			I _S	-1.5	A
Pulsed Drain Current (Note 6)			I _D	-20	A

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	T _A = +25°C	P _D	0.84	W
	T _A = +70°C		0.52	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	R _{θJA}	155	°C/W
	t < 10s		109	
Total Power Dissipation (Note 6)	T _A = +25°C	P _D	1.27	W
	T _A = +70°C		0.8	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	R _{θJA}	102	°C/W
	t < 10s		71	
Thermal Resistance, Junction to Case (Note 6)		R _{θJC}	34	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 substrate PCB, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PCB, 2oz copper, with 1inch square copper plate.

Electrical Characteristics – Q1 NMOS (@TA = +25°C unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	2.3	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	38	60	m Ω	$V_{GS} = 10V, I_D = 3.1A$
			55	100		$V_{GS} = 4.5V, I_D = 2A$
Forward Transfer Admittance	$ Y_{fs} $	—	4	—	S	$V_{DS} = 5V, I_D = 3.1A$
Diode Forward Voltage	V_{SD}	—	0.8	1	V	$V_{GS} = 0V, I_S = 1A$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	290	400	pF	$V_{DS} = 15V, V_{GS} = 0V, f = 1.2MHz$
Output Capacitance	C_{oss}	—	40	80		
Reverse Transfer Capacitance	C_{rss}	—	40	80		
Gate Resistance	R_g	—	1.4	—	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1MHz$
Total Gate Charge ($V_{GS} = 4.5V$)	Q_g	—	4	6	nC	$V_{DS} = 15V, V_{GS} = 4.5V, I_D = 3.1A$
Total Gate Charge ($V_{GS} = 10V$)	Q_g	—	9	13		
Gate-Source Charge	Q_{gs}	—	1.2	—		
Gate-Drain Charge	Q_{gd}	—	1.5	—		
Turn-On Delay Time	$t_{D(on)}$	—	3	—	ns	$V_{GS} = 10V, V_{DS} = 15V, R_G = 3\Omega, R_L = 4.7\Omega$
Turn-On Rise Time	t_r	—	5	—		
Turn-Off Delay Time	$t_{D(off)}$	—	13	—		
Turn-Off Fall Time	t_f	—	3	—		

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

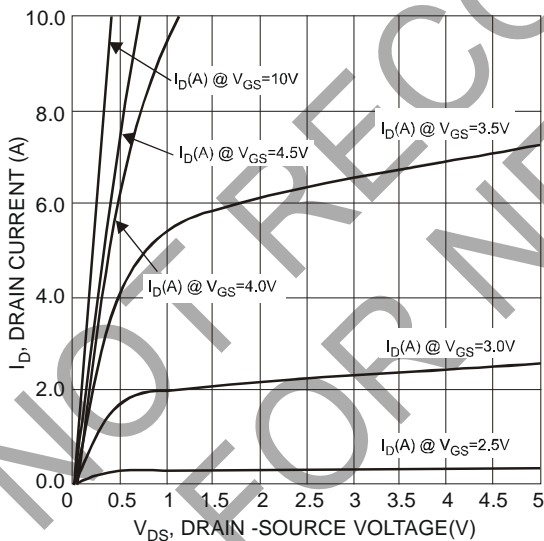


Fig. 1 Typical Output Characteristics

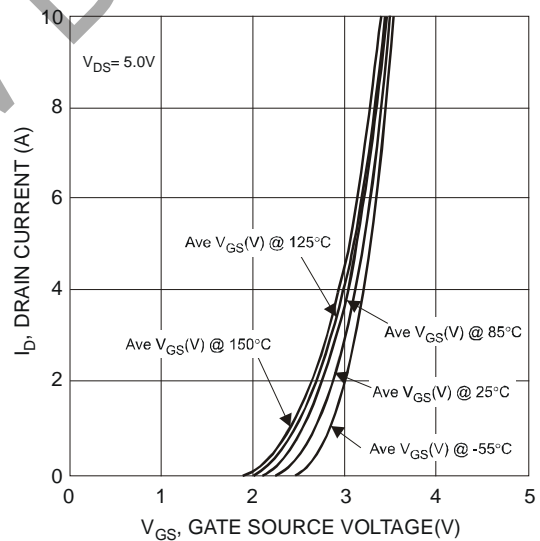


Fig. 2 Typical Transfer Characteristics

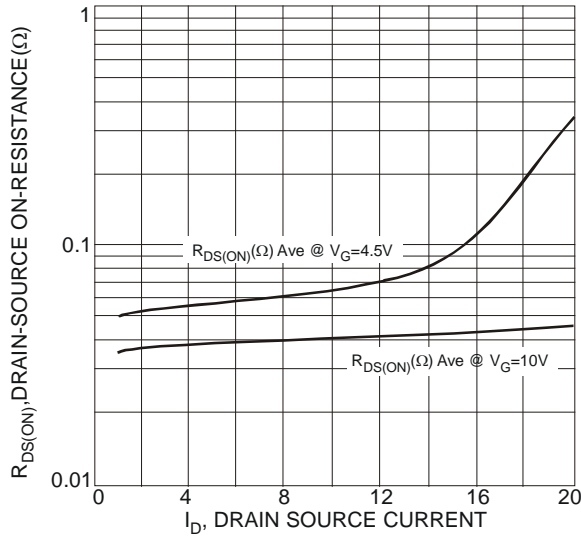


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

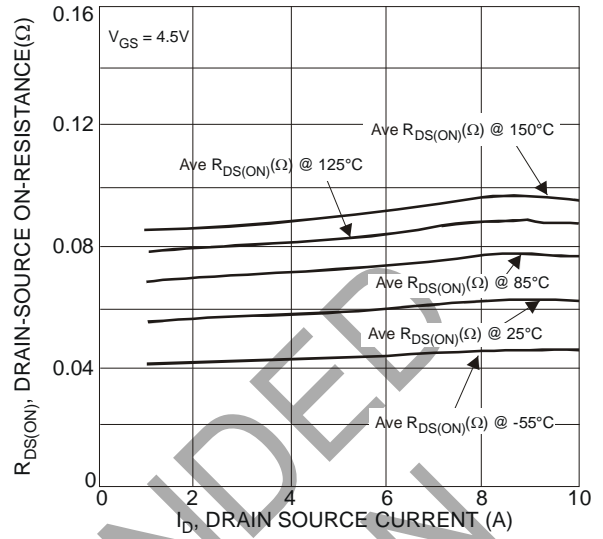


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

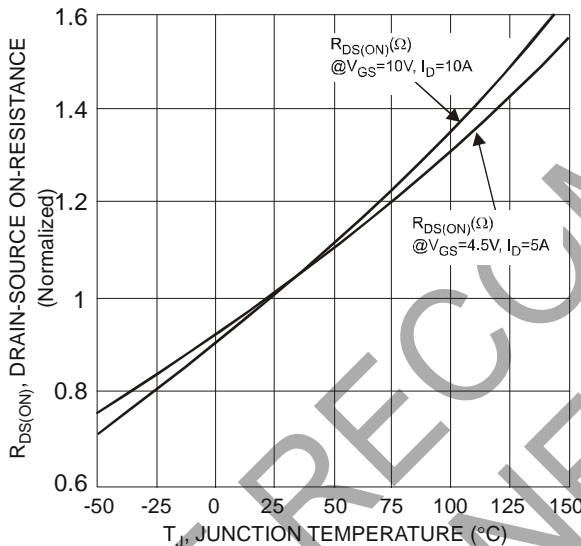


Fig. 5 On-Resistance Variation with Temperature

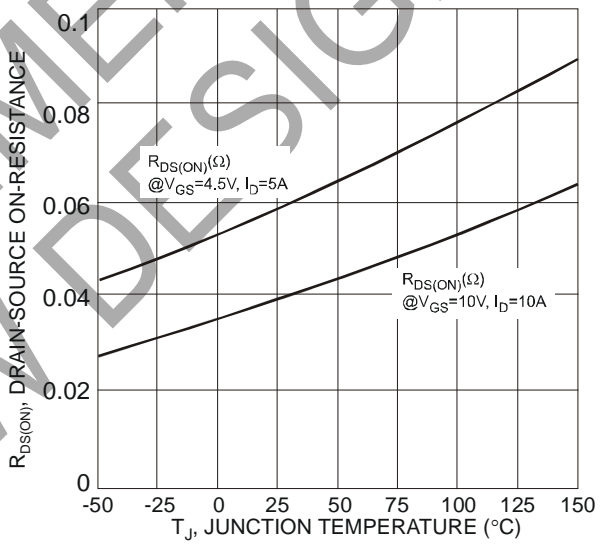


Fig. 6 On-Resistance Variation with Temperature

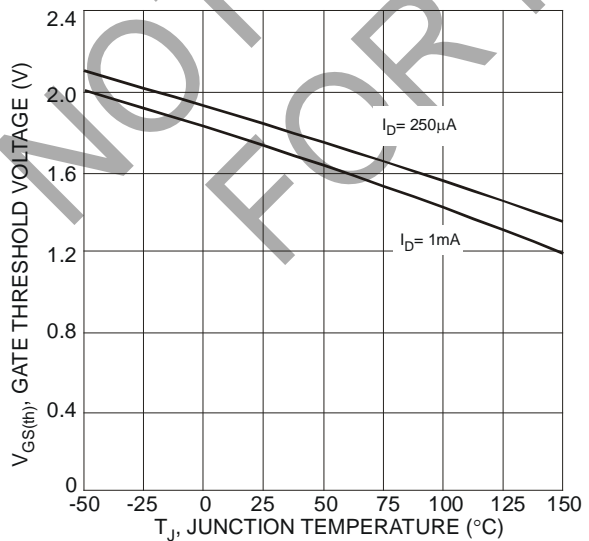


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

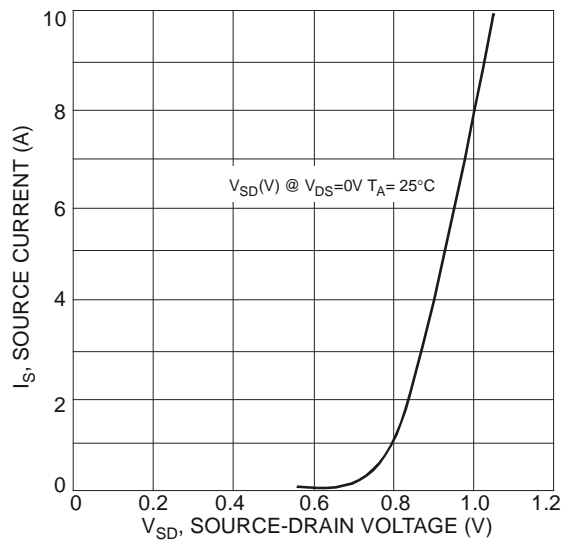
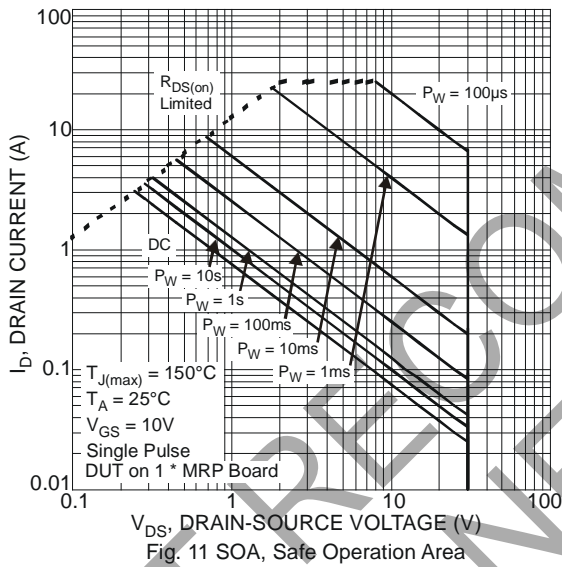
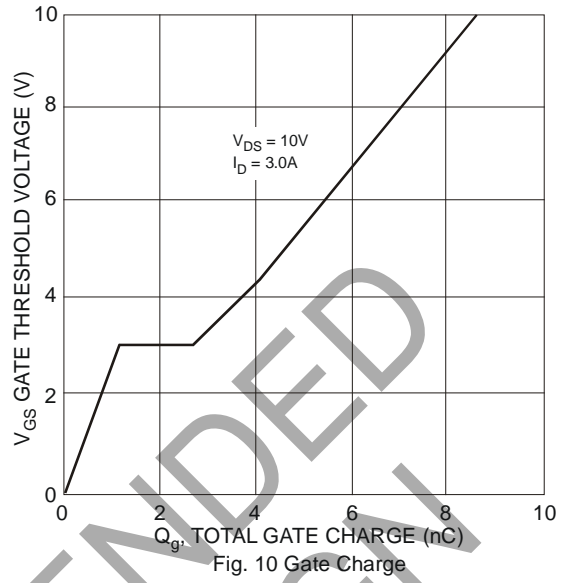
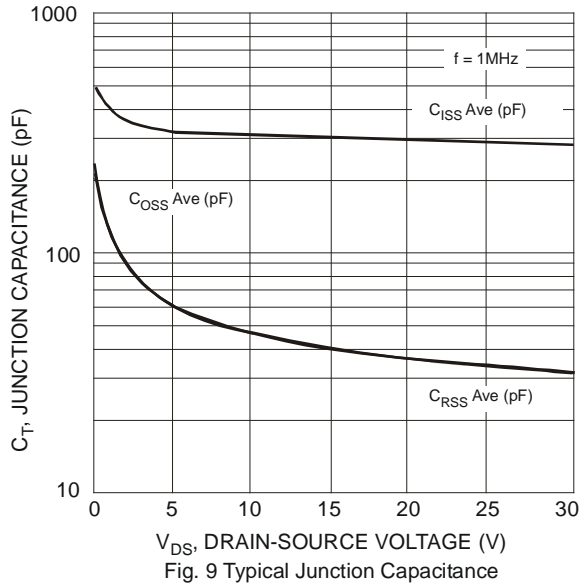


Fig. 8 Diode Forward Voltage vs. Current



NOT RECOMMENDED FOR NEW DESIGN

Electrical Characteristics – Q2 PMOS (@TA = +25°C unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1.0	μA	$V_{DS} = -24V, V_{GS} = 0V$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	—	-2.3	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	73 99	95 140	m Ω	$V_{GS} = -10V, I_D = -2.7A$ $V_{GS} = -4.5V, I_D = -2A$
Forward Transfer Admittance	$ Y_{fs} $	—	6	—	S	$V_{DS} = -5V, I_D = -2.7A$
Diode Forward Voltage	V_{SD}	—	-0.8	-1.0	V	$V_{GS} = 0V, I_S = -1A$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	350	420	pF	$V_{DS} = -15V, V_{GS} = 0V,$ $f = 1.2MHz$
Output Capacitance	C_{oss}	—	50	100		
Reverse Transfer Capacitance	C_{rss}	—	45	80		
Gate Resistance	R_g	—	17.1	—	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1MHz$
Total Gate Charge ($V_{GS} = -4.5V$)	Q_g	—	4	6	nC	$V_{DS} = -15V, V_{GS} = -4.5V, I_D = -3A$
Total Gate Charge ($V_{GS} = -10V$)	Q_g	—	7	9		
Gate-Source Charge	Q_{gs}	—	0.9	—		
Gate-Drain Charge	Q_{gd}	—	1.2	—		
Turn-On Delay Time	$t_{D(on)}$	—	4.8	—	ns	$V_{GS} = -10V, V_{DS} = -15V,$ $R_G = 6\Omega, R_L = 15\Omega$
Turn-On Rise Time	t_r	—	7.3	—		
Turn-Off Delay Time	$t_{D(off)}$	—	20	—		
Turn-Off Fall Time	t_f	—	13	—		

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

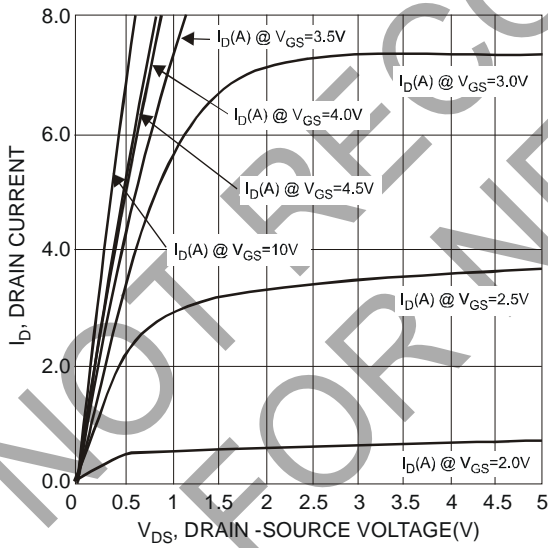


Fig. 12 Typical Output Characteristics

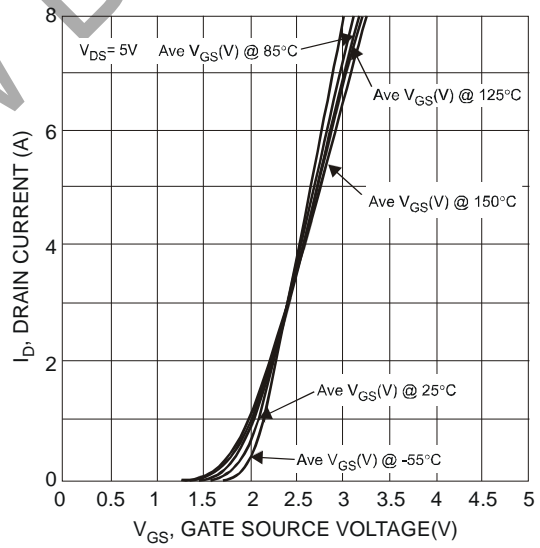


Fig. 13 Typical Transfer Characteristics

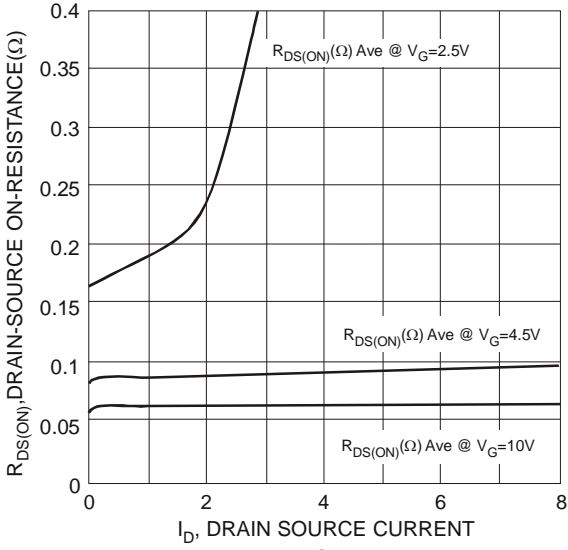


Fig. 14 Typical On-Resistance vs. Drain Current and Gate Voltage

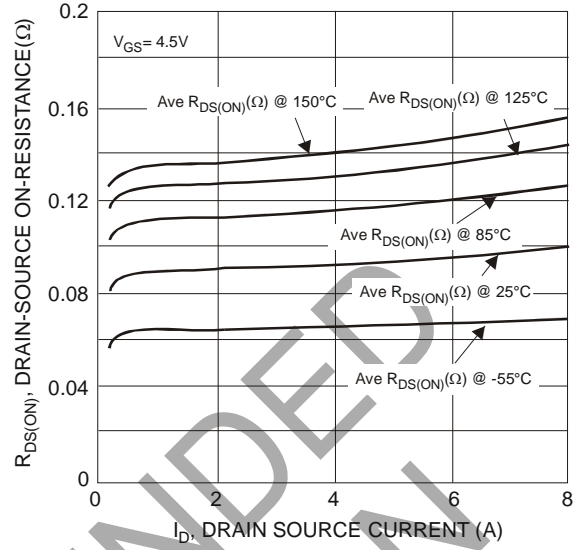


Fig. 15 Typical On-Resistance vs. Drain Current and Temperature

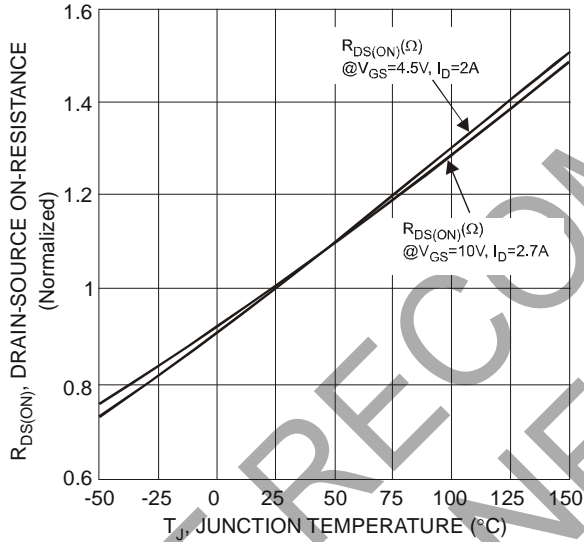


Fig. 16 On-Resistance Variation with Temperature

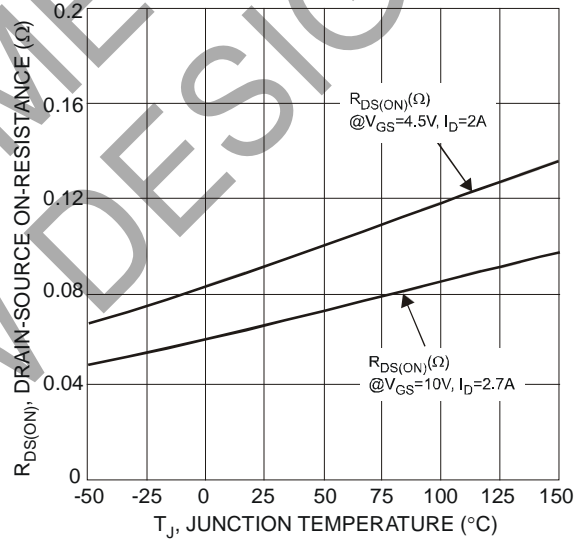


Fig. 17 On-Resistance Variation with Temperature

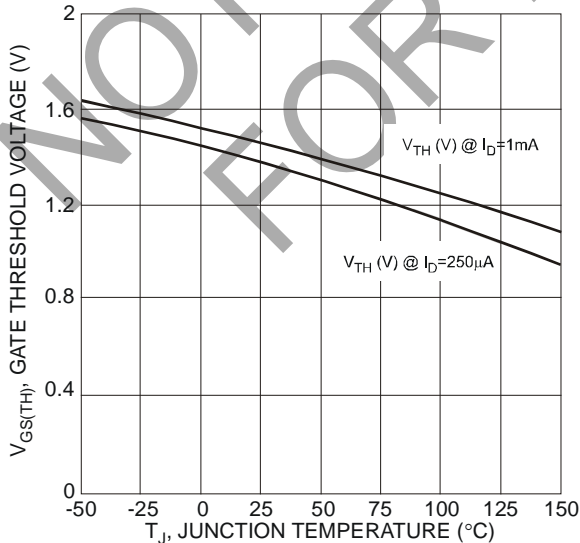


Fig. 18 Gate Threshold Variation vs. Ambient Temperature

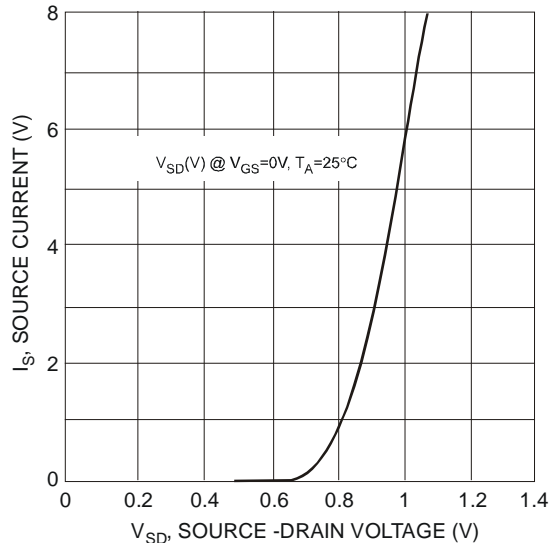
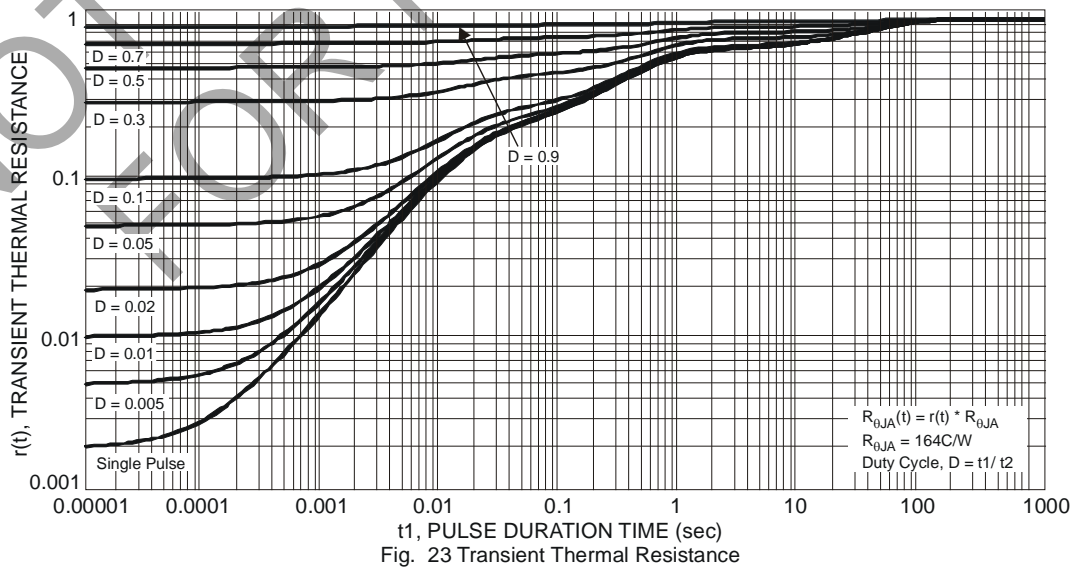
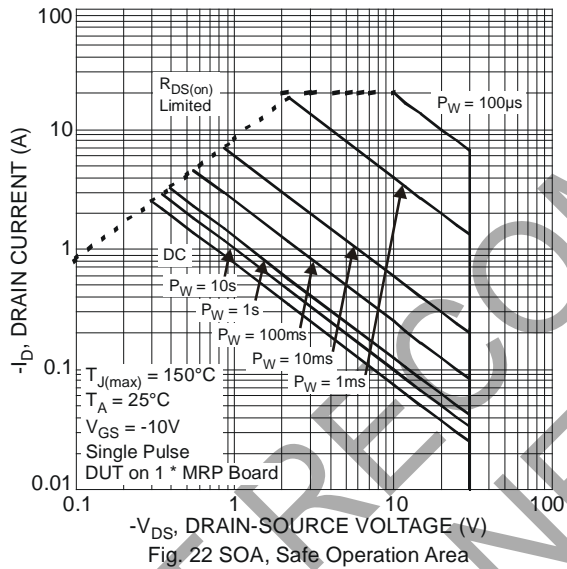
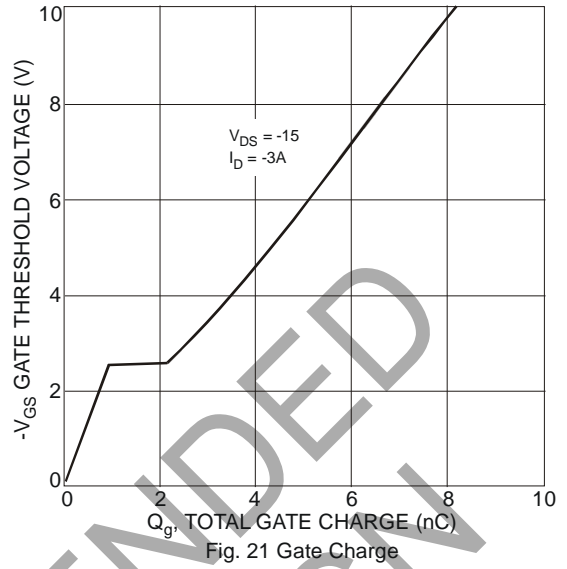
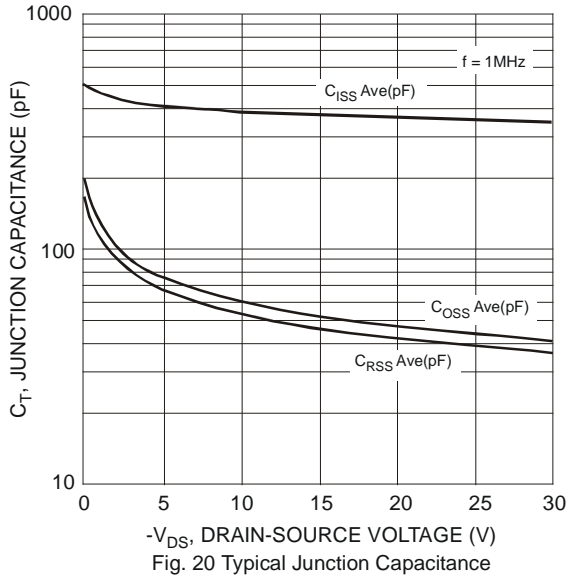
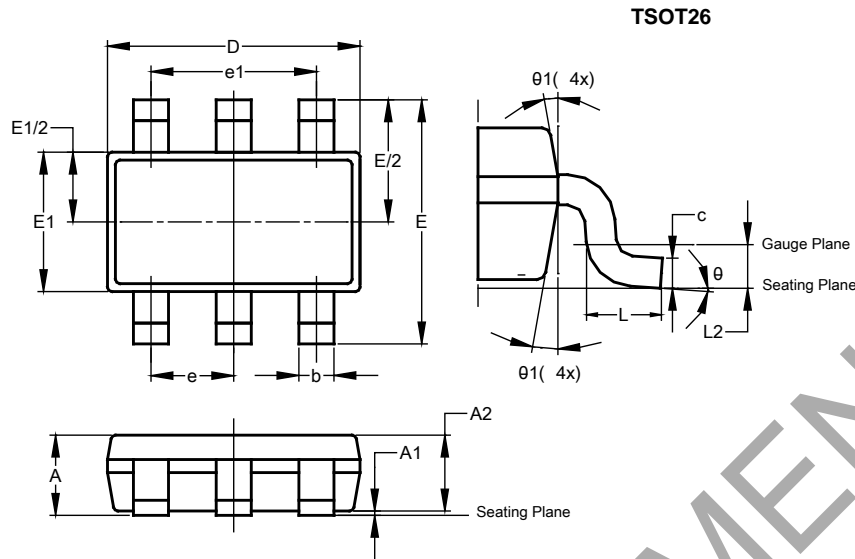


Fig. 19 Diode Forward Voltage vs. Current



Package Outline Dimensions

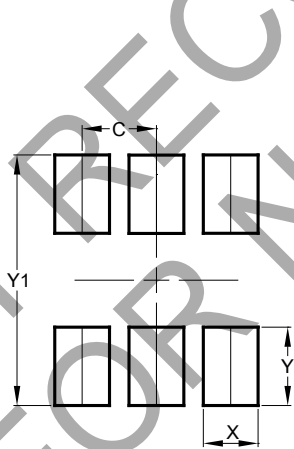
Please see <http://www.diodes.com/package-outlines.html> for the latest version.



TSOT26			
Dim	Min	Max	Typ
A	-	1.00	-
A1	0.010	0.100	-
A2	0.840	0.900	-
D	2.800	3.000	2.900
E	2.800 BSC		
E1	1.500	1.700	1.600
b	0.300	0.450	-
c	0.120	0.200	-
e	0.950 BSC		
e1	1.900 BSC		
L	0.30	0.50	-
L2	0.250 BSC		
θ	0°	8°	4°
θ_1	4°	12°	-
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

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