Features

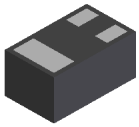
- Low On-Resistance
- Very Low Gate Threshold Voltage, 0.9V Max.
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **ESD Protected Gate**
- **Ultra Low Profile Package**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

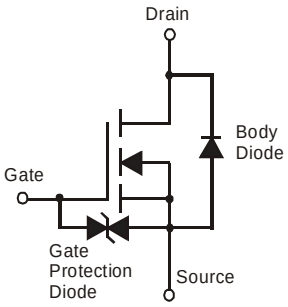
- Case: X2-DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish — NiPdAu over Copper leadframe; Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.001 grams (Approximate)

ESD PROTECTED

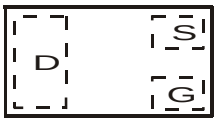
X2-DFN1006-3



Bottom View



Equivalent Circuit



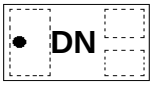
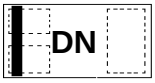
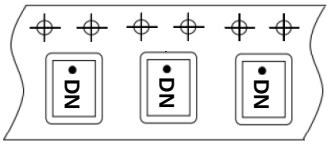
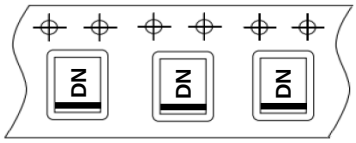
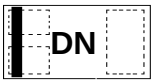
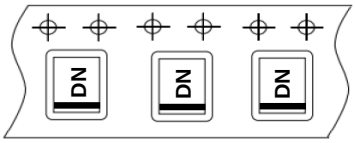
Top View
Pin-Out

Ordering Information (Note 4)

Part Number	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMN2005LP4K-7	DN	7	8	3,000
DMN2005LP4K-7B	DN	7	8	10,000

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

DMN2005LPK-7	 Top View Dot Denotes Drain Side From date code 1527 (YYWW), this changes to:  Top View Bar Denotes Gate and Source Side  
DMN2005LPK-7B	 Top View Bar Denotes Gate and Source Side DN = Part Marking Code 

Maximum Ratings (@T_A = +25°C unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	±10	V
Drain Current per element (Note 5)	Continuous Pulsed (Note 6)	I_D	300 350	mA

Thermal Characteristics (@T_A = +25°C unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	400	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	280	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-65 to +150	°C

Electrical Characteristics (@T_A = +25°C unless otherwise specified.)

Characteristic		Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (per element) (Note 7)							
Drain-Source Breakdown Voltage		BV_{DSS}	20	—	—	V	V_{GS} = 0V, I_D = 100µA
Zero Gate Voltage Drain Current		I_{DSS}	—	—	10	µA	V_{DS} = 17V, V_{GS} = 0V
Gate-Source Leakage		I_{GSS}	—	—	±5	µA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (per element) (Note 7)							
Gate Threshold Voltage		$V_{GS(th)}$	0.53	—	0.9	V	V_{DS} = V_{GS}, I_D = 100µA
Static Drain-Source On-Resistance		$R_{DS\ (ON)}$	— — — — —	0.35 0.4 0.45 0.55 0.65	1.5 1.7 1.7 3.5 3.5	Ω	V_{GS} = 4V, I_D = 10mA V_{GS} = 2.7V, I_D = 200mA V_{GS} = 2.5V, I_D = 10mA V_{GS} = 1.8V, I_D = 200mA V_{GS} = 1.5V, I_D = 1mA
Forward Transfer Admittance		$\lvert Y_{fs} \rvert$	40	—	—	mS	V_{DS} = 3V, I_D = 10mA
DYNAMIC CHARACTERISTICS							
Input Capacitance		C_{iss}	—	37.1	—	pF	V_{DS} = 10V, V_{GS} = 0V f = 1.0MHz
Output Capacitance		C_{oss}	—	6.5	—	pF	
Reverse Transfer Capacitance		C_{rss}	—	4.8	—	pF	
Switching Time	Turn-On Time	t_{on}	—	4.06	—	nS	V_{DD} = 10V, R_l = 47Ω, V_{GEN} = 4.5V, R_{GEN} = 10Ω.
	Turn-Off Time	t_{off}	—	13.7	—		

Notes: 5. Device mounted on FR-4 PCB.
6. Pulse width ≤10µS, Duty Cycle ≤1%.
7. Short duration pulse test used to minimize self-heating effect.

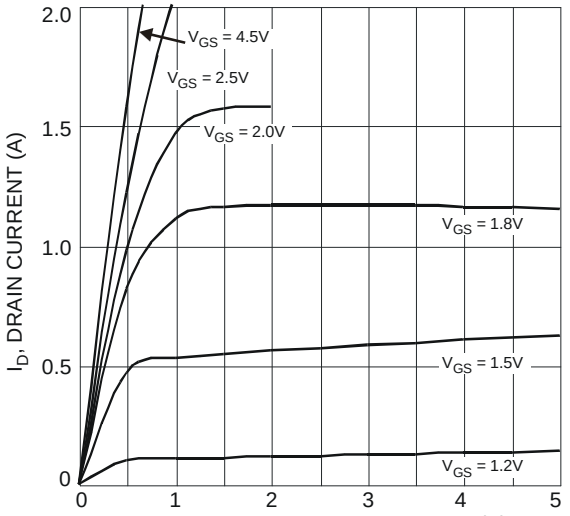


Fig. 1 Typical Output Characteristics

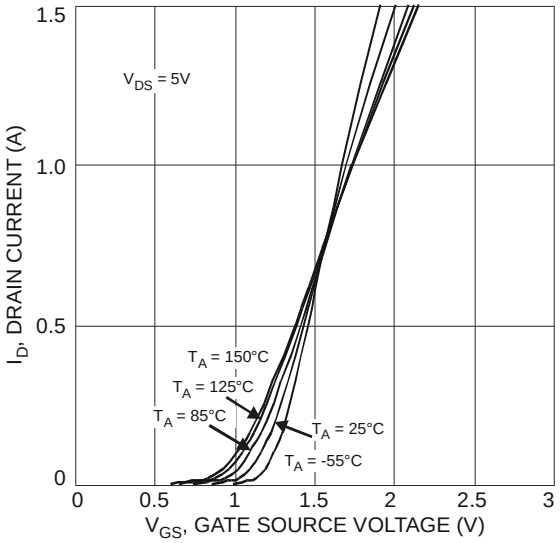


Fig. 2 Typical Transfer Characteristics

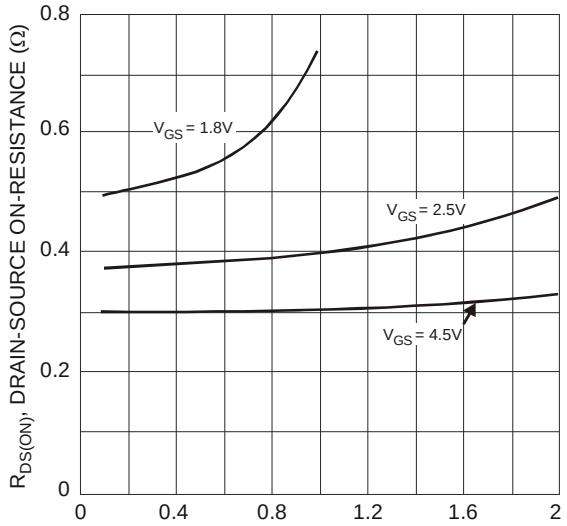


Fig. 3 Typical On-Resistance
vs. Drain Current and Gate Voltage

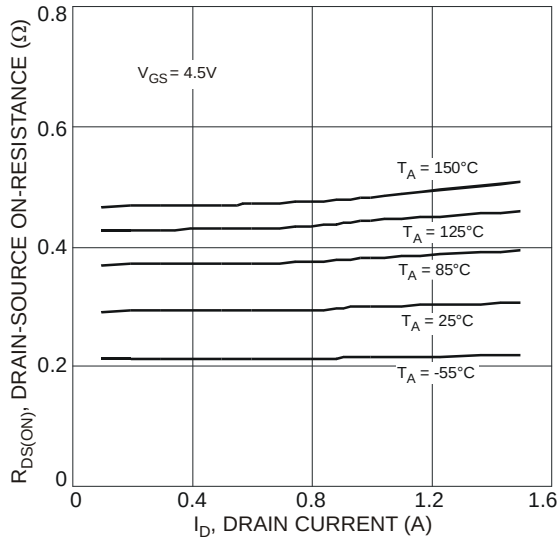


Fig. 4 Typical Drain-Source On-Resistance
vs. Drain Current and Temperature

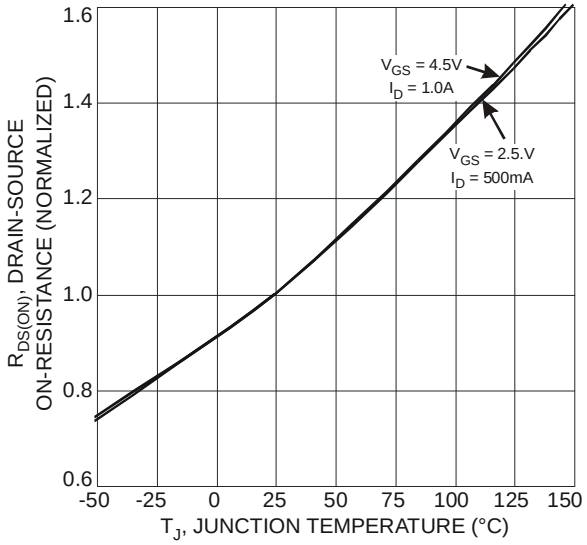


Fig. 5 On-Resistance Variation with Temperature

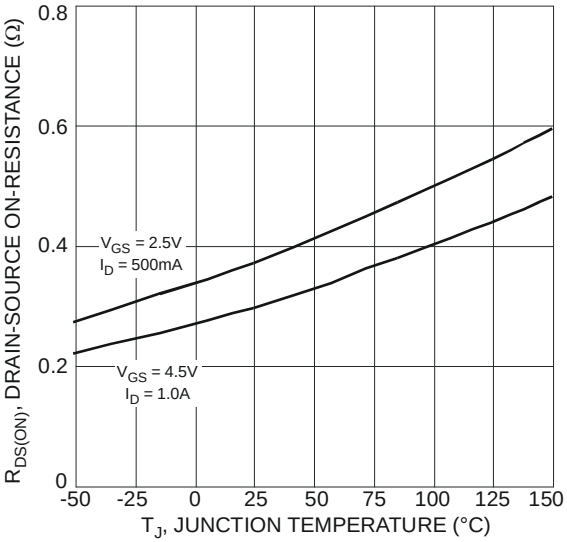


Fig. 6 On-Resistance Variation with Temperature

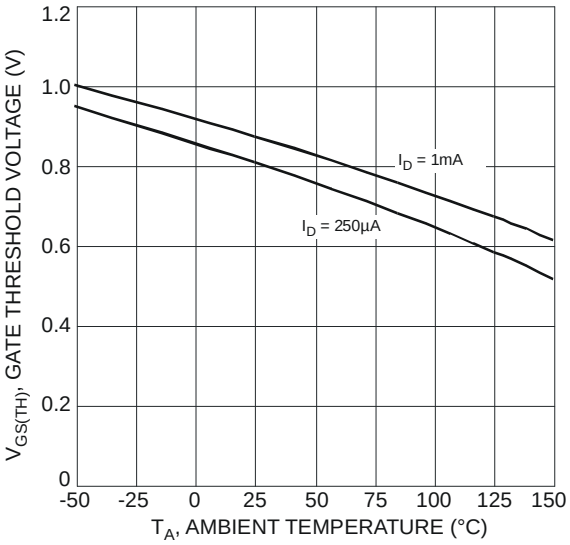


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

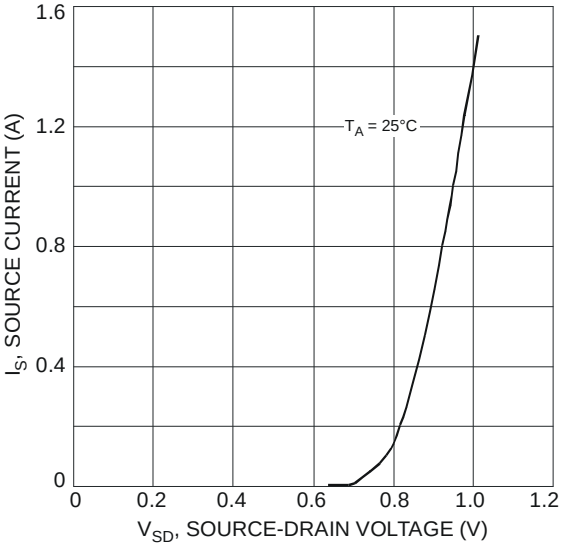


Fig. 8 Diode Forward Voltage vs. Current

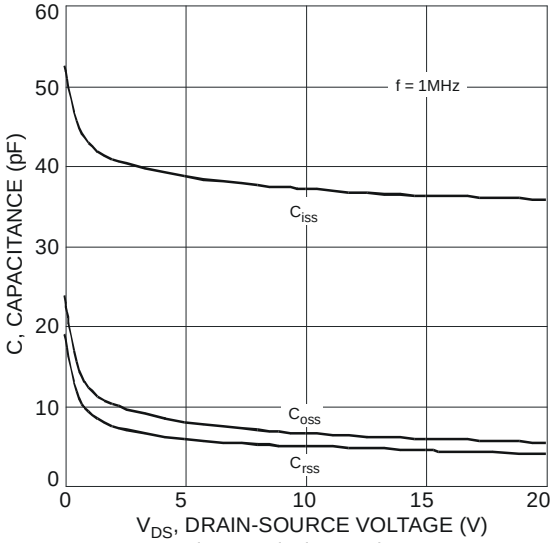
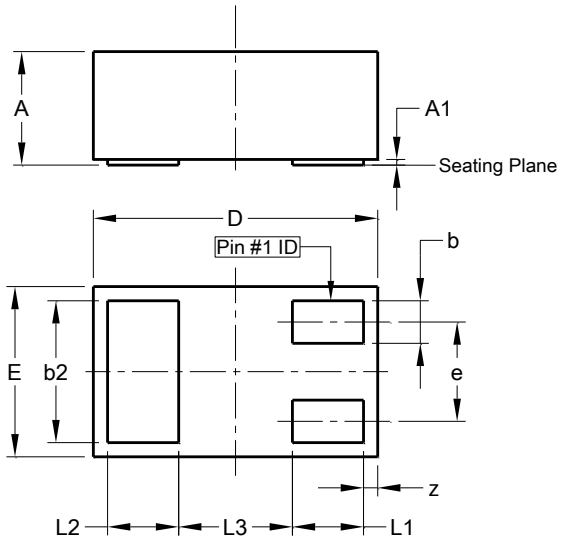


Fig. 9 Typical Capacitance

Package Outline Dimensions

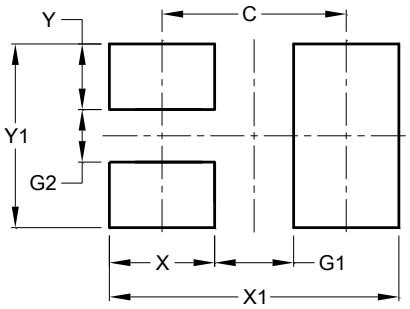
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



X2-DFN1006-3			
Dim	**Min**	**Max**	**Typ**
A	—	0.40	—
A1	0.00	0.05	0.03
b	0.10	0.20	0.15
b2	0.45	0.55	0.50
D	0.95	1.05	1.00
E	0.55	0.65	0.60
e	-	-	0.35
L1	0.20	0.30	0.25
L2	0.20	0.30	0.25
L3	-	-	0.40
z	0.02	0.08	0.05
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for latest version.



Dimensions	Value (in mm)
C	0.70
G1	0.30
G2	0.20
X	0.40
X1	1.10
Y	0.25
Y1	0.70

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