

**16-bit I2C-bus and SMBus I/O port with interrupt**

**Features**

- Operation power supply voltage from 2.3V to 5.5V
- 16-bit I/O pins which can be programmed as Input or Output
- 5V tolerant I/Os
- Polarity inversion register
- Active LOW interrupt output
- Low current consumption
- 0Hz to 400KHz clock frequency
- Noise filter on SCL/SDA inputs
- Power-on reset
- ESD protection (4KV HBM and 1KV CDM)
- Latch-up tested (exceeds 100mA)
- Offered in two different packages: TSSOP-24 and TQFN 4x4-24

**Description**

The PI4IOE5V9535 is a 24-pin device that provides 16 bits of General Purpose parallel Input/Output (GPIO) expansion for I<sup>2</sup>C-bus/SMBus applications. It includes the features such as higher driving capability, 5V tolerance, lower power supply, individual I/O configuration, and smaller packaging. It provides a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PI4IOE5V9535 consists of two 8-bit Configuration (Input or Output selection), Input, Output and Polarity Inversion (active HIGH or active LOW operation) registers. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input port or Output port register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The PI4IOE5V9535 is identical to the PI4IOE5V9555 except for the removal of the internal I/O pull-up resistor which greatly reduces power consumption when the I/Os are held LOW.

The PI4IOE5V9535 open-drain interrupt output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I2C-bus address and allow up to eight devices to share the same I2C-bus/SMBus. The fixed I2C-bus address of the PI4IOE5V9535 are the same as the PI4IOE5V9555 allowing up to eight of these devices in any combination to share the same I2C-bus/SMBus.

**Pin Configuration**

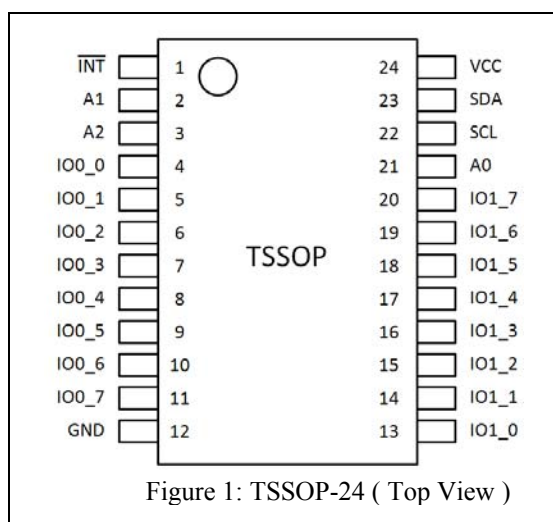


Figure 1: TSSOP-24 ( Top View )

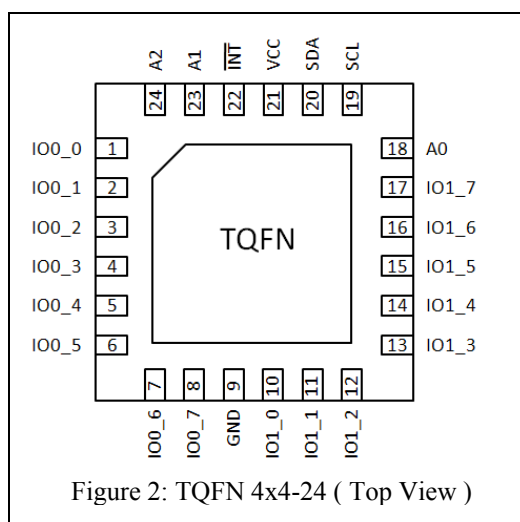


Figure 2: TQFN 4x4-24 ( Top View )

## Pin Description

Table 1: Pin Description

Pin		Name	Type	Description
TSSOP24	TQFN24			
1	22	$\overline{\text{INT}}$	O	Interrupt input (open-drain)
2	23	A1	I	Address input 1
3	24	A2	I	Address input 2
4	1	IO0_0	I/O	Port 0 input/output 0
5	2	IO0_1	I/O	Port 0 input/output 1
6	3	IO0_2	I/O	Port 0 input/output 2
7	4	IO0_3	I/O	Port 0 input/output 3
8	5	IO0_4	I/O	Port 0 input/output 4
9	6	IO0_5	I/O	Port 0 input/output 5
10	7	IO0_6	I/O	Port 0 input/output 6
11	8	IO0_7	I/O	Port 0 input/output 7
12	9	GND	G	Ground
13	10	IO1_0	I/O	Port 1 input/output 0
14	11	IO1_1	I/O	Port 1 input/output 1
15	12	IO1_2	I/O	Port 1 input/output 2
16	13	IO1_3	I/O	Port 1 input/output 3
17	14	IO1_4	I/O	Port 1 input/output 4
18	15	IO1_5	I/O	Port 1 input/output 5
19	16	IO1_6	I/O	Port 1 input/output 6
20	17	IO1_7	I/O	Port 1 input/output 7
21	18	A0	I	Address input 0
22	19	SCL	I	Serial clock line input
23	20	SDA	I	Serial data line open-drain
24	21	VCC	P	Supply voltage

\* I = Input; O = Output; P = Power; G = Ground

## Maximum Ratings

Power supply .....	-0.5V to +6.0V
Voltage on an I/O pin .....	GND-0.5V to +6.0V
Input current .....	±20mA
Output current on an I/O pin .....	±50mA
Supply current .....	150mA
Ground supply current .....	200mA
Total power dissipation .....	200mW
Operation temperature .....	-40~85°C
Storage temperature .....	-65~150°C
Maximum Junction temperature, T <sub>j</sub> (max) .....	125°C

### Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Static characteristic

VCC = 2.3 V to 5.5 V; GND = 0 V; Tamb = -40 °C to +85 °C; unless otherwise specified.

Table 2: Static characteristic

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Power supply</b>						
VCC	Supply voltage		2.3	-	5.5	V
I <sub>CC</sub>	Supply current	Operating mode; VCC = 5.5 V; no load; f <sub>SCL</sub> = 400 kHz	-	40	60	μA
		Operating mode; VCC = 2.3 V; no load; f <sub>SCL</sub> = 400 kHz		10	20	μA
I <sub>sb</sub>	Standby current	Standby mode; VCC = 5.5 V; no load; V <sub>I</sub> = GND; f <sub>SCL</sub> = 0 kHz; I/O = inputs	-	0.25	1	uA
		Standby mode; VCC = 5.5 V; no load; V <sub>I</sub> = VCC; f <sub>SCL</sub> = 0 kHz; I/O = inputs	-	0.25	1	uA
V <sub>POR</sub>	Power-on reset voltage <sup>[1]</sup>		-	1.16	1.41	V
<b>Input SCL, input/output SDA</b>						
V <sub>IL</sub>	Low level input voltage		-0.5	-	+0.3VCC	V
V <sub>IH</sub>	High level input voltage		0.7VCC	-	5.5	V
I <sub>OL</sub>	Low level output current	V <sub>OL</sub> = 0.4V	3	-	-	mA
I <sub>L</sub>	Leakage current	V <sub>I</sub> = VCC = GND	-1	-	1	μA
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = GND	-	6	10	pF

**Static Characteristic Cont.**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>I/Os</b>						
V <sub>IL</sub>	Low level input voltage		-0.5	-	+0.81	V
V <sub>IH</sub>	High level input voltage		+1.8	-	5.5	V
I <sub>OL</sub>	Low level output current	VCC = 2.3 V to 5.5 V; V <sub>OL</sub> = 0.5 V <sup>[2]</sup>	8	10	-	mA
		VCC = 2.3 V to 5.5 V; V <sub>OL</sub> = 0.7 V <sup>[2]</sup>	10	14	-	mA
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = -8mA; VCC = 2.3V <sup>[3]</sup>	1.8	-	-	V
		I <sub>OH</sub> = -10mA; VCC = 2.3V <sup>[3]</sup>	1.7	-	-	V
		I <sub>OH</sub> = -8mA; VCC = 3.0V <sup>[3]</sup>	2.6	-	-	V
		I <sub>OH</sub> = -10mA; VCC = 3.0V <sup>[3]</sup>	2.5	-	-	V
		I <sub>OH</sub> = -8mA; VCC = 4.75V <sup>[3]</sup>	4.1	-	-	V
		I <sub>OH</sub> = -10mA; VCC = 4.75V <sup>[3]</sup>	4.0	-	-	V
I <sub>LIH</sub>	High level input leakage current	VCC = 5.5V; V <sub>I</sub> = VCC	-	-	1	μA
I <sub>LIL</sub>	Low level input leakage current	VCC = 5.5V; V <sub>I</sub> = GND	-	-	-1	μA
C <sub>i</sub>	Input capacitance		-	3.7	10	pF
C <sub>o</sub>	Output capacitance		-	3.7	10	pF
<b>Interrupt <math>\overline{\text{INT}}</math></b>						
I <sub>OL</sub>	Low level output current	V <sub>OL</sub> = 0.4V	3	-	-	mA
<b>Select inputs A0,A1,A2</b>						
V <sub>IL</sub>	Low level input voltage		-0.5	-	+0.81	V
V <sub>IH</sub>	High level input voltage		+1.8	-	5.5	V
I <sub>L</sub>	Input leakage current		-1		1	μA

- Note:**  
 [1]: VCC must be lowered to 0.2 V for at least 20 us in order to reset part.  
 [2]: Each I/O must be externally limited to a maximum of 25 mA and each octal (IO0\_0 to IO0\_7 and IO1\_0 to IO1\_7) must be limited to a maximum current of 100 mA for a device total of 200 mA.  
 [3]: The total current sourced by all I/Os must be limited to 160 mA.

## Dynamic Characteristics

Table 3: Dynamic characteristics

Symbol	Parameter	Test Conditions	Standard mode I <sup>2</sup> C		Fast mode I <sup>2</sup> C		Unit
			Min	Max	Min	Max	
f <sub>SCL</sub>	SCL clock frequency		0	100	0	400	kHz
t <sub>BUF</sub>	bus free time between a STOP and START condition		4.7	-	1.3	-	μs
t <sub>HD;STA</sub>	hold time (repeated) START condition		4.0	-	0.6	-	μs
t <sub>SU;STA</sub>	set-up time for a repeated START condition		4.7	-	0.6	-	μs
t <sub>SU;STO</sub>	set-up time for STOP condition		4.0	-	0.6	-	μs
t <sub>VD;ACK</sub> <sup>[1]</sup>	data valid acknowledge time		-	3.45	-	0.9	μs
t <sub>HD;DAT</sub> <sup>[2]</sup>	data hold time		0	-	0	-	ns
t <sub>VD;DAT</sub>	data valid time		-	3.45	-	0.9	μs
t <sub>SU;DAT</sub>	data set-up time		250	-	100	-	ns
t <sub>LOW</sub>	LOW period of the SCL clock		4.7	-	1.3	-	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock		4.0	-	0.6	-	μs
t <sub>f</sub>	fall time of both SDA and SCL signals		-	300	-	300	ns
t <sub>r</sub>	rise time of both SDA and SCL signals		-	1000	-	300	ns
t <sub>SP</sub>	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
<b>Port timing</b>							
t <sub>v(Q)</sub>	Data output valid time <sup>[3]</sup>		-	200	-	200	ns
t <sub>su(D)</sub>	Data input set-up time		150	-	150	-	ns
t <sub>h(D)</sub>	Data input hold time		1	-	1	-	μs
<b>Interrupt timing</b>							
t <sub>v(INT)</sub>	Valid time on pin $\overline{\text{INT}}$		-	4	-	4	μs
t <sub>rst(INT)</sub>	Reset time on pin $\overline{\text{INT}}$		-	4	-	4	μs

**Note:**

 [1]: t<sub>VD;ACK</sub> = time for acknowledgement signal from SCL LOW to SDA (out) LOW.

 [2]: t<sub>VD;DAT</sub> = minimum time for SDA data out to be valid following SCL LOW.

 [3]: t<sub>v(Q)</sub> measured from 0.7VCC on SCL to 50% I/O output.

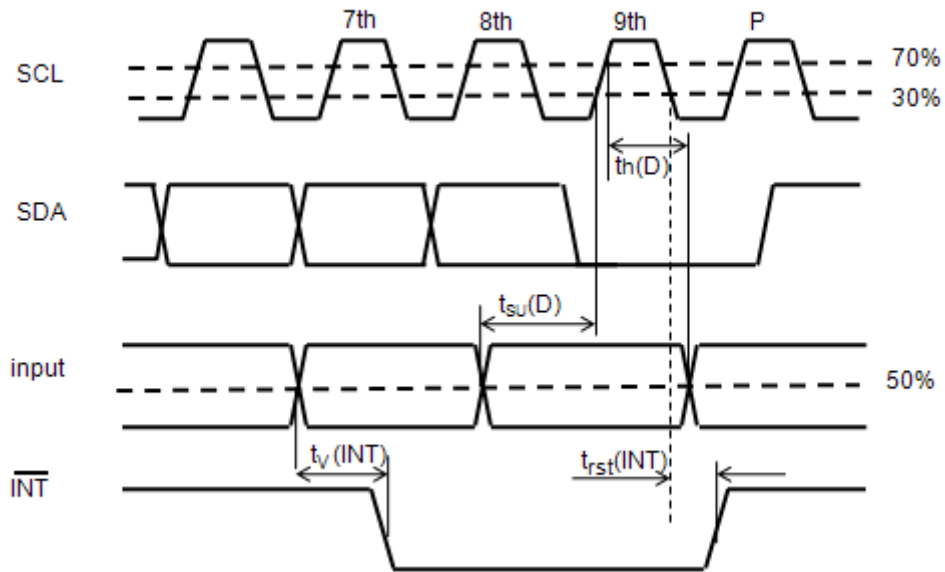
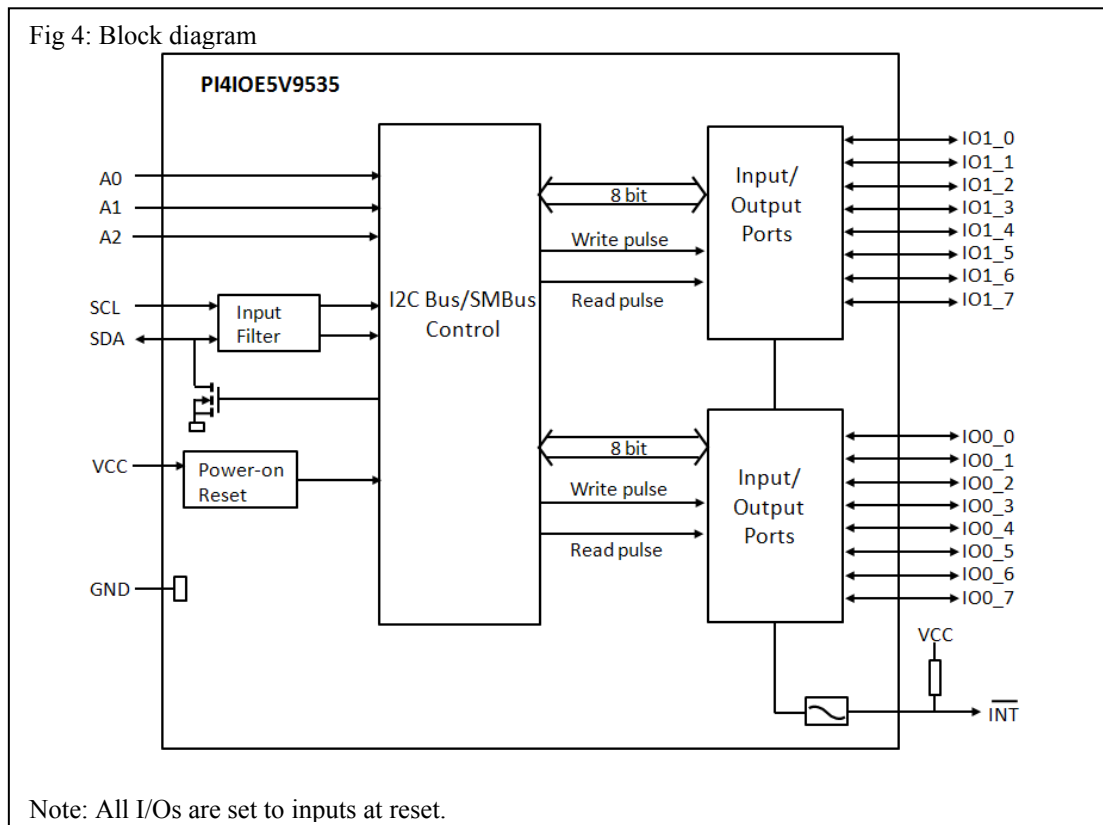


Figure 3: timing parameters for INT signal

**PI4IOE5V9535 Block Diagram**



## Details Description

### a. Device address

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Address Byte	0	1	0	0	A2	A1	A0	R/W

Note: Read “1”, Write “0”

### b. Registers

#### i. Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 4: Command byte

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity inversion port 0
5	Polarity inversion port 1
6	Configuration port 0
7	Configuration port 1

## ii. Register 0 and 1: input port registers

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value 'X' is determined by the externally applied logic level.

Table 5: Input port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 6: Input port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

## iii. Register 2 and 3: Output port registers

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 6 and 7. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 7: Output port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 8: Output port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

## iv. Register 4 and 5: Polarity inversion registers

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the Input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

Table 9: Polarity Inversion port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0



Table 10: Polarity Inversion port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

#### v. Register 6 and 7: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. Note that there is a high value resistor tied to VCC at each pin. At reset, the IOs are configured as inputs with a pull-up to VCC.

Table 11: Configuration port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 12: Configuration port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

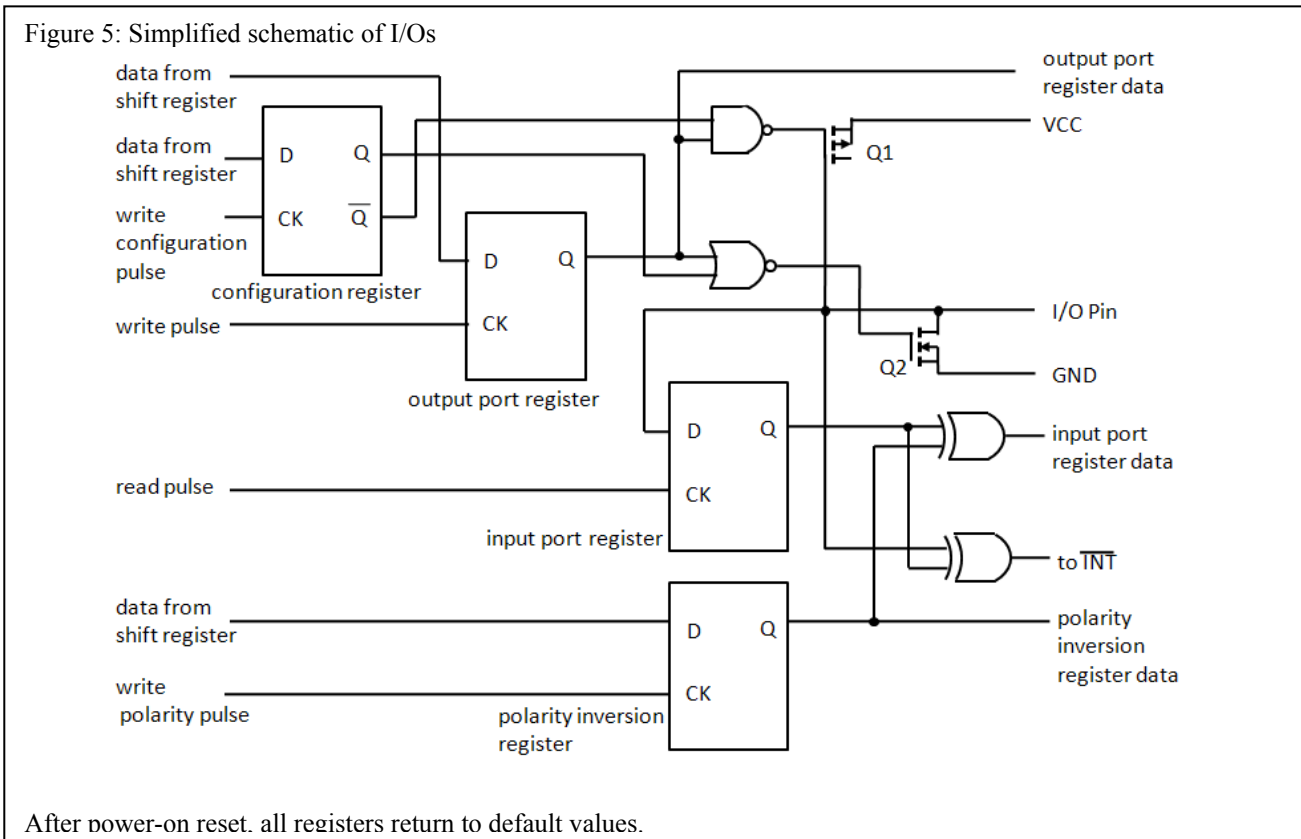
#### c. Power-on reset

When power is applied to VCC, an internal power-on reset holds the PI4IOE5V9535 in a reset condition until VCC has reached VPOR. At that point, the reset condition is released and the PI4IOE5V9535 registers and SMBus state machine will initialize to their default states. The power-on reset typically completes the reset and enables the part by the time the power supply is above VPOR. However, when it is required to reset the part by lowering the power supply, it is necessary to lower it below 0.2 V.

#### d. I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance. . The input voltage may be raised above VCC to a maximum of 5.5 V.

If the I/O is configured as an output, then on PI4IOE5V9535 either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either VCC or GND.

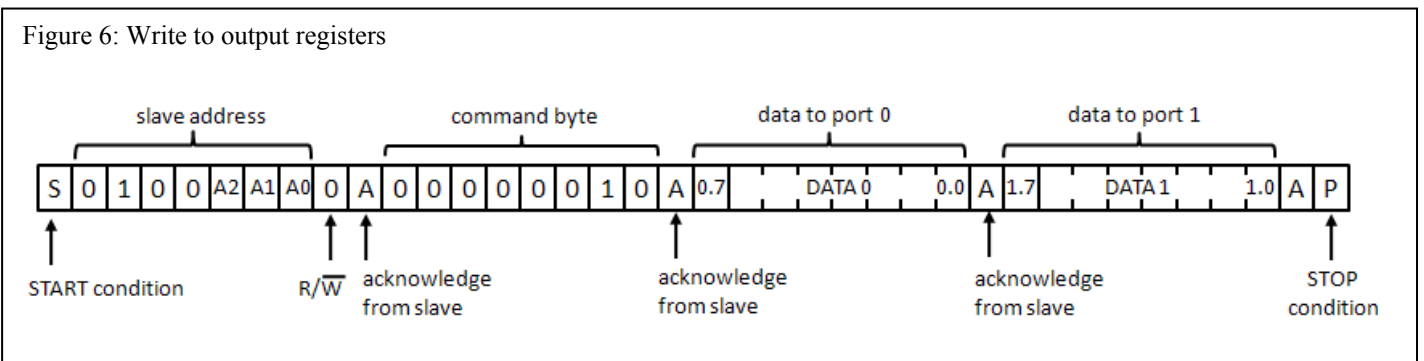


## e. Bus Transaction

### i. Writing to the port registers

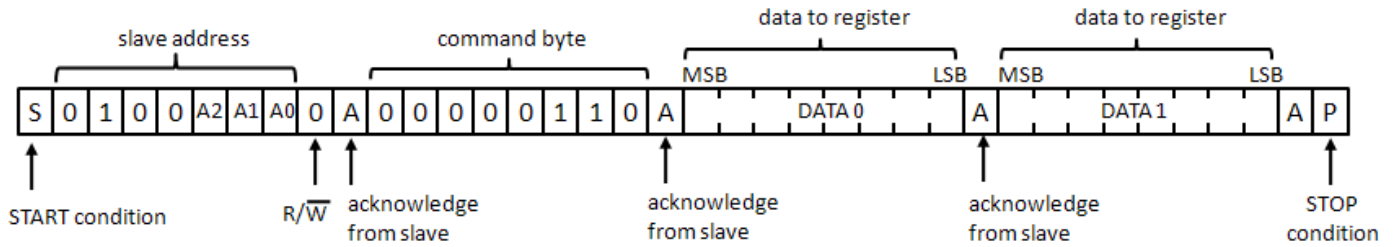
Data is transmitted to the PI4IOE5V9535 by sending the device address and setting the least significant bit to a logic 0. The command byte is sent after the address and determines which register will receive the data following the command byte. The eight registers within the PI4IOE5V9535 are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair. For example, if the first byte is sent to Output Port 1 (register 3), the next byte will be stored in Output Port 0 (register 2). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

Figure 6: Write to output registers



Write to Output port register

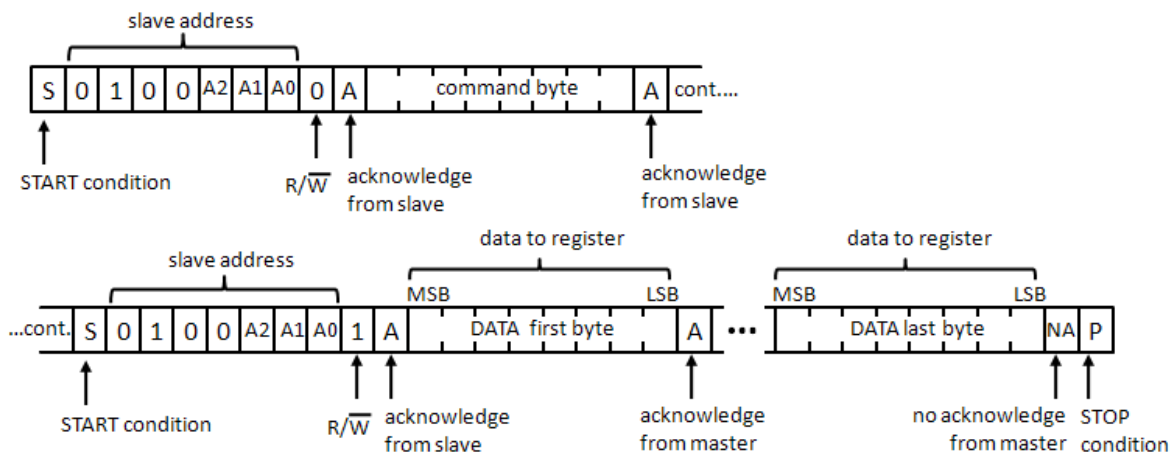
Figure 7: Write to configuration registers



ii. Reading the port registers

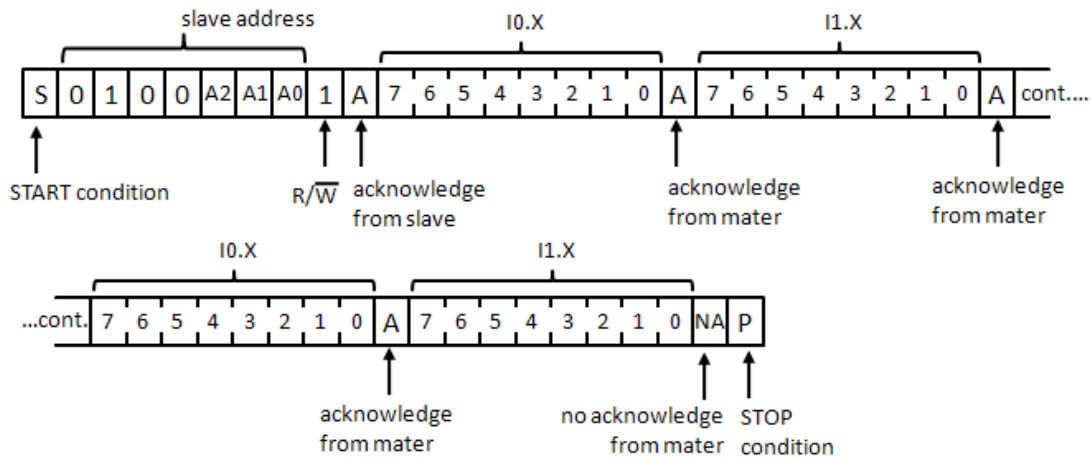
In order to read data from the PI4IOE5V9535, the bus master must first send the PI4IOE5V9535 address with the least significant bit set to a logic 0. The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the PI4IOE5V9535. Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission but the final byte received, the bus master must not acknowledge the data.

Figure 8: Read from registers



Note: Transfer can be stopped at any time by a STOP condition.

Figure 9: Read Input port register



**Note:** Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

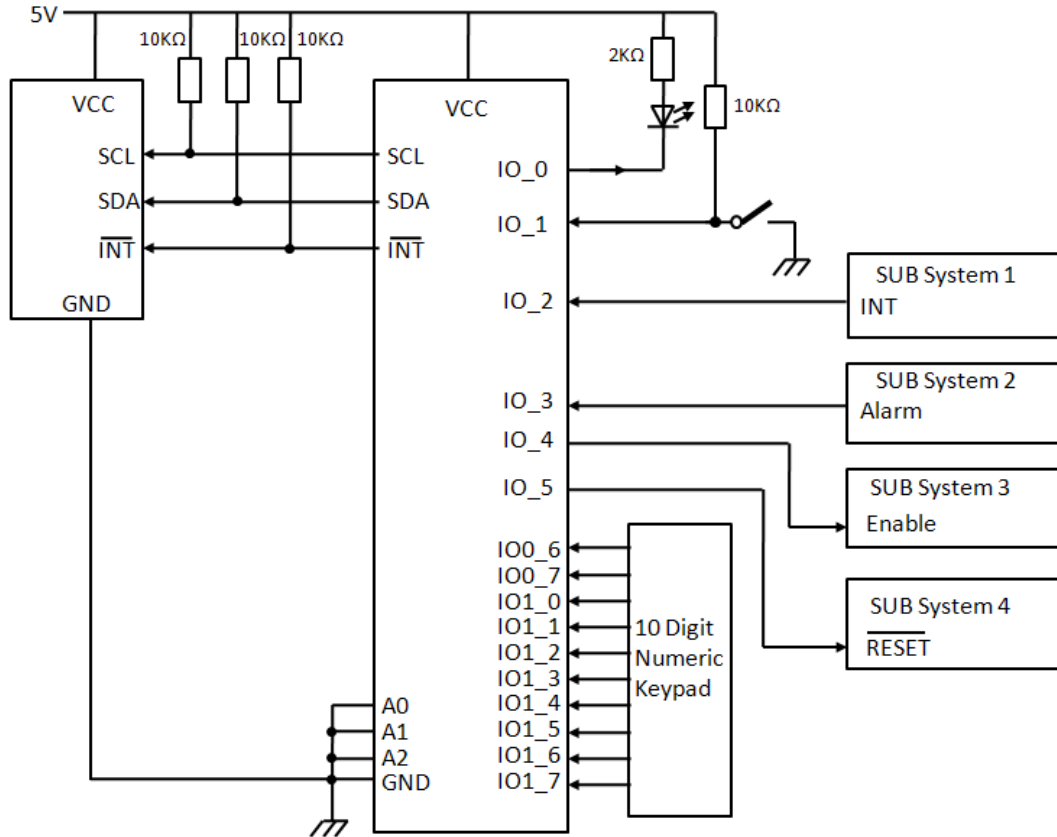
### iii. Interrupt output

The open-drain interrupt output is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read. A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

**Note:** Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

**Application Design-In Information**

Figure 10: Typical application



Device address configured as 0100 000xb for this example.

IO0\_0, IO0\_4, IO0\_5 configured as outputs.

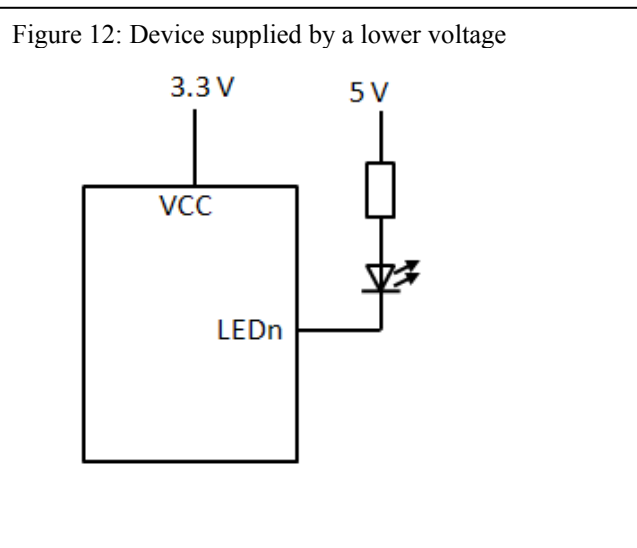
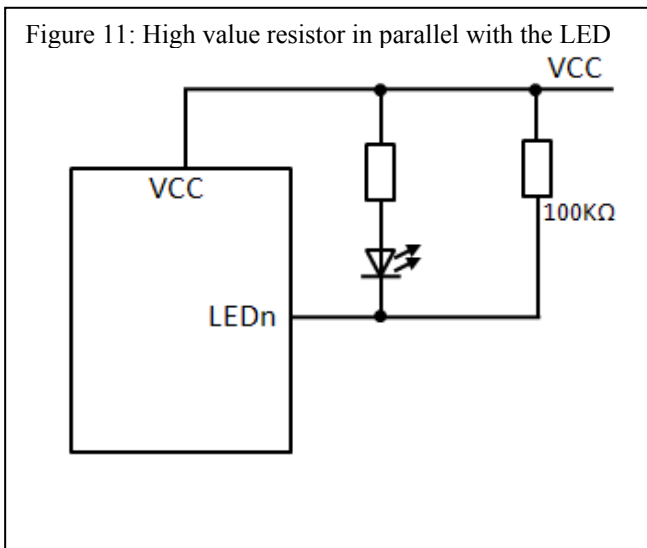
IO0\_1, IO0\_2, IO0\_3 configured as inputs.

IO0\_6, IO0\_7, and IO1\_0 to IO1\_7 configured as inputs.

## Minimizing ICC when the I/Os are used to control LEDS

When the I/Os are used to control LEDs, they are normally connected to VCC through a resistor as shown in Figure 11. Since the LED acts as a diode, when the LED is off the I/O  $V_I$  is about 1.2 V less than VCC. The supply current, ICC, increases as  $V_I$  becomes lower than VCC.

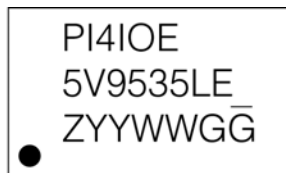
Designs need minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to VCC when the LED is off. Figure 11 shows a high value resistor in parallel with the LED. Figure 12 shows VCC less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O  $V_I$  at or above VCC and prevent additional supply current consumption when the LED is off.



## Part Marking

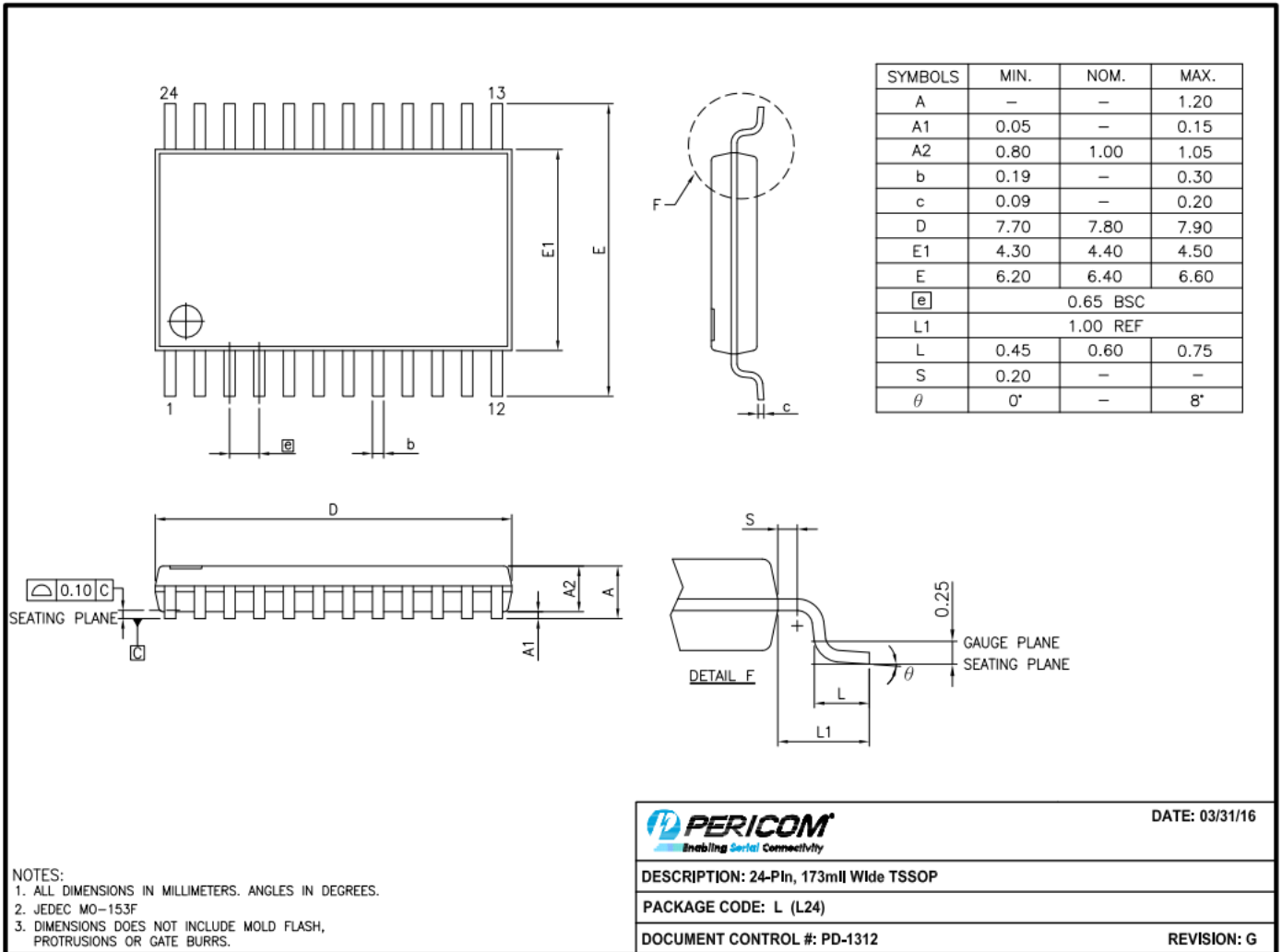


Z: Die Rev  
YYWW: Date Code (Year & Work Week)  
1st "G": Assembly Site Code  
2nd "G": Wafer Fab Site Code

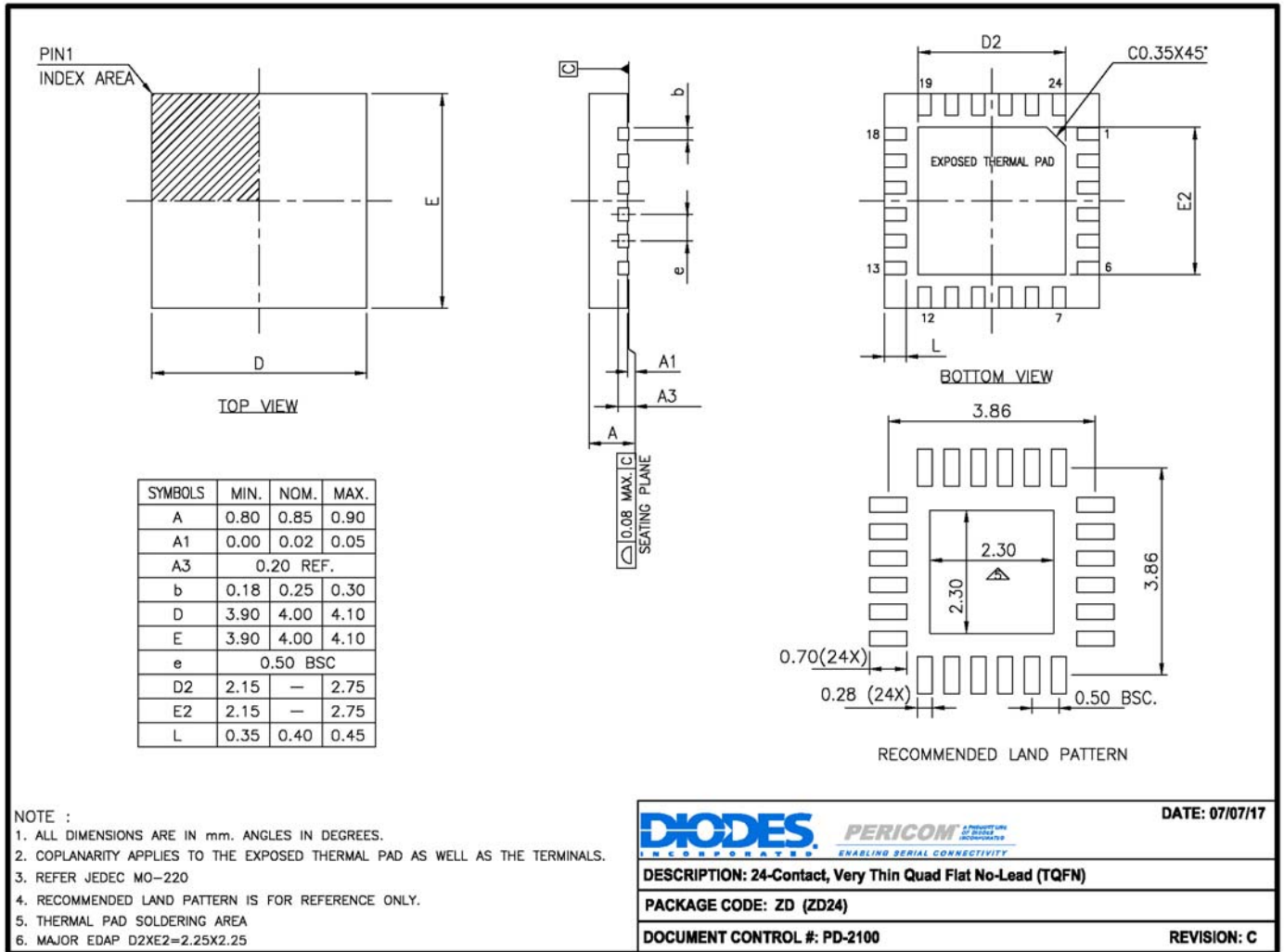


Z: Die Rev  
YYWW: Date Code (Year & Work Week)  
1st G: Assembly Site Code  
2nd G: Wafer Fab Site Code

**Packaging Mechanical**  
TSSOP-24(L)



**TQFN-24(ZD)**



17-0533

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

**Ordering Information**

Part Numbers	Package Code	Description
PI4IOE5V9535LEX	L	24-Pin, 173mil-Wide (TSSOP)
PI4IOE5V9535ZDEX	ZD	24-Contact, Very Thin Quad Flat No-Lead (TQFN)

**Notes:**

- Thermal characteristics can be found on the company web site at [www.diodes.com/design/support/packaging/](http://www.diodes.com/design/support/packaging/)
- E = Pb-free and Green
- X suffix = Tape/Reel



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  2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.
- B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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