4 CHANNEL LOW CAPACITANCE TVS DIODE ARRAY

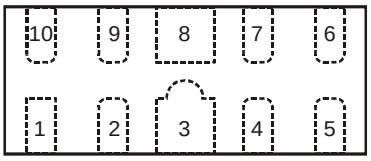
Features

- Clamping Voltage: 9V at 10A 100ns TLP; 9V at 6A 8µs/20µs
- IEC 61000-4-2 (ESD): Air – +20/-18kV, Contact – +20/-16kV
- IEC 61000-4-5 (Lightning): ±6A (8/20µs)
- 4 Channels of ESD Protection
- Low Channel Input Capacitance of 0.5pF Typical
- TLP Dynamic Resistance: 0.25Ω
- Typically Used for High Speed Ports Such as USB 2.0, DVI™, HDMI™, Ethernet Port, IEEE, MDDI, PCI Express®, SATA/ eSATA
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

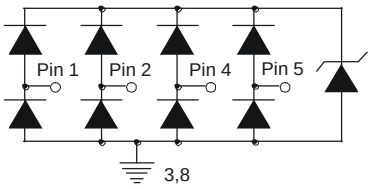
Mechanical Data

- Case: U-DFN2510-10
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: NiPdAu over Copper Leadframe (Lead-Free Plating) Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.038 grams (Approximate)

Pin #	Description
1, 2, 4, 5	I/O
6, 7, 9, 10	No Connection
3, 8	V_{SS}



Pin Description (Top View)



Device Schematic

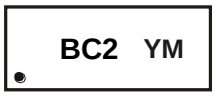
Ordering Information (Note 4)

Part Number	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DT1140-04LP-7	AEC-Q101	BC2	7	8	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

U-DFN2510-10



BC2 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: F = 2018)
M = Month (ex: 9 = September)

Date Code Key

Year	2013	2014	2015	2016	2017	2018
Code	A	B	C	D	E	F

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Current, per IEC 61000-4-5	I_{PP}	6	A	I/O to V_{SS}, 8/20µs
Peak Pulse Power, per IEC 61000-4-5	P_{PP}	60	W	I/O to V_{SS}, 8/20µs
Operating Voltage (DC)	V_{DC}	6	V	I/O to V_{SS}
ESD Protection – Contact Discharge, per IEC 61000-4-2	$V_{ESD\_CONTACT}$	+20/-16	kV	I/O to V_{SS}
ESD Protection – Air Discharge, per IEC 61000-4-2	V_{ESD_AIR}	+20/-18	kV	I/O to V_{SS}
Operating Temperature	T_{OP}	-55 to +85	°C	—
Storage Temperature	T_{STG}	-55 to +150	°C	—

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	P_D	350	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	$R_{\theta JA}$	360	°C/W

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Reverse Working Voltage	V_{RWM}	—	—	5.5	V	I_R=1mA, , I/O to V_{SS}
Reverse Current (Note 6)	I_R	—	—	50	nA	V_R = 5V, I/O to V_{SS}
Reverse Breakdown Voltage	V_{BR}	6	—	—	V	I_R = 1mA, I/O to V_{SS}
Forward Clamping Voltage	V_F	-1.0	-0.85	—	V	I_F = -15mA, I/O to V_{SS}
Holding Voltage	V_H	5.5	—	—	V	—
Reverse Clamping Voltage (Note 7)	V_C	—	6.4	—	V	I_{PP} = 1A, I/O to V_{SS}, 8/20µs
Reverse Clamping Voltage (Note 7)	V_C	—	9	10	V	I_{PP} = 6A, I/O to V_{SS}, 8/20µs
Trigger Voltage	V_{TRIG}	—	—	9.5	V	—
ESD Clamping Voltage	V_{ESD}	—	9	—	V	TLP, 10A, t_P = 100ns, I/O to V_{SS}
Dynamic Reverse Resistance	R_{DIF-R}	—	0.25	—	Ω	TLP, 10A, t_P = 100ns, I/O to V_{SS}
Dynamic Forward Resistance	R_{DIF-F}	—	0.25	—	Ω	TLP, 10A, t_P = 100ns, V_{SS} to I/O
Channel Input Capacitance	$C_{I/O}$	—	0.5	0.65	pF	$V_{I/O}$ = 2.5V, V_{SS} = 0V, f = 1MHz

Notes:
5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes Incorporated's suggested pad layout, which can be found on our website at http://www.diodes.com/package-outlines.html.
6. Short duration pulse test used to minimize self-heating effect.
7. Clamping voltage value is based on an 8x20µs peak pulse current (I_{pp}) waveform.

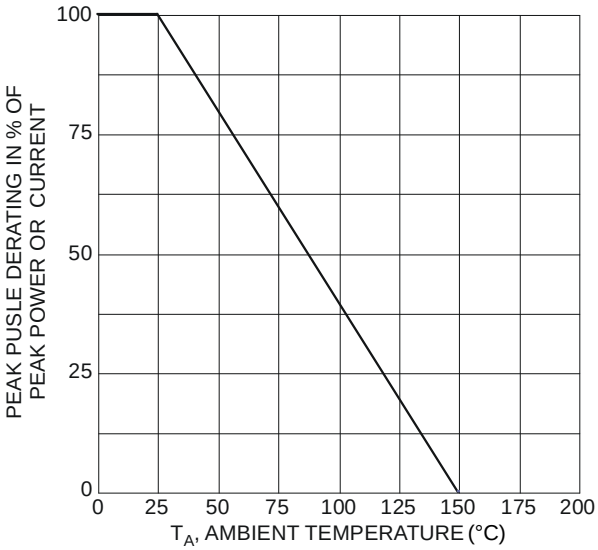


Figure 1 Pulse Derating Curve

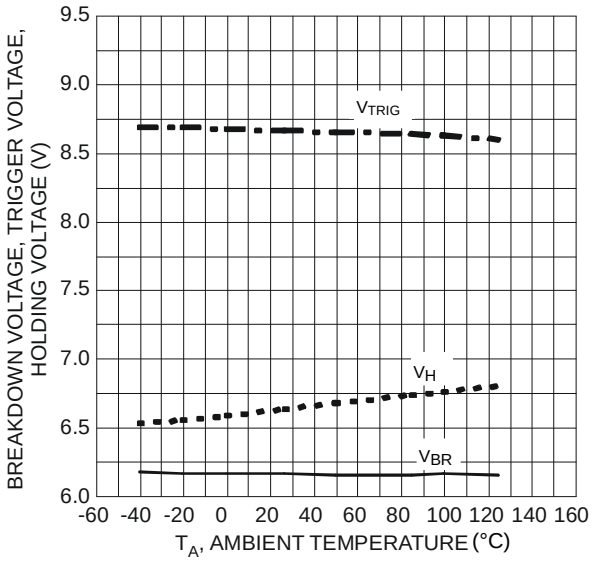


Figure 2 BV, Trigger Voltage, Holding Voltage vs. Ambient Temperature

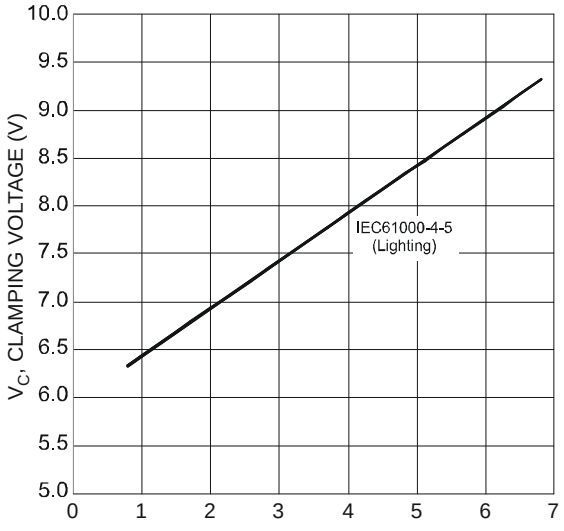


Figure 3 Clamping Voltage Characteristic

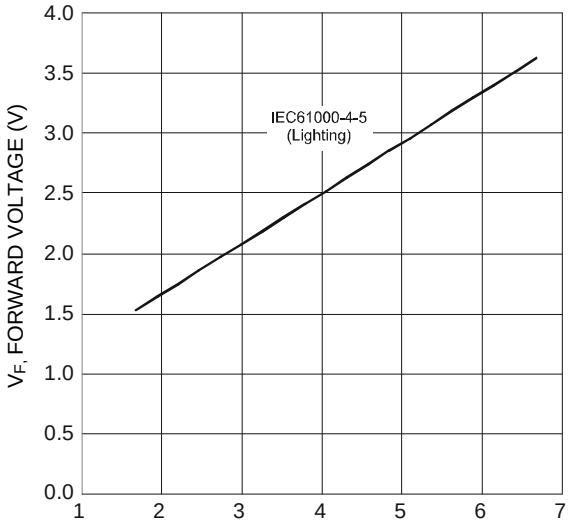


Figure 4 Forward Voltage Characteristic

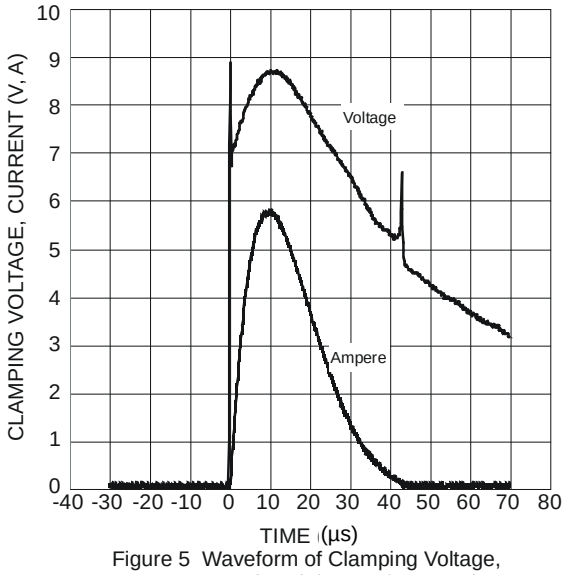


Figure 5 Waveform of Clamping Voltage, Current vs. Time (8/20µs, I/O to V_{SS})

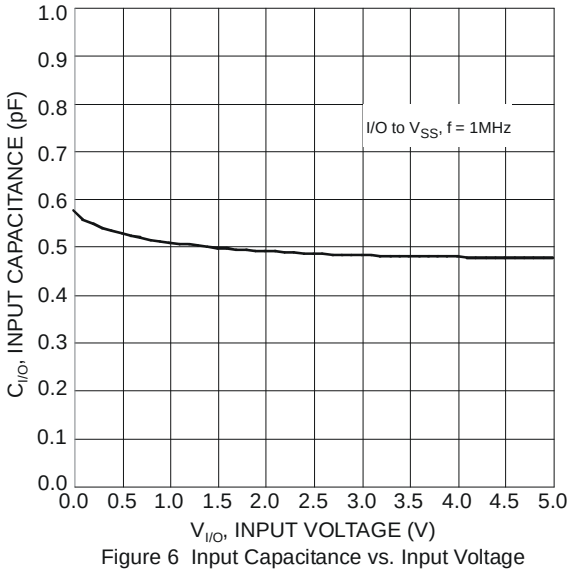


Figure 6 Input Capacitance vs. Input Voltage

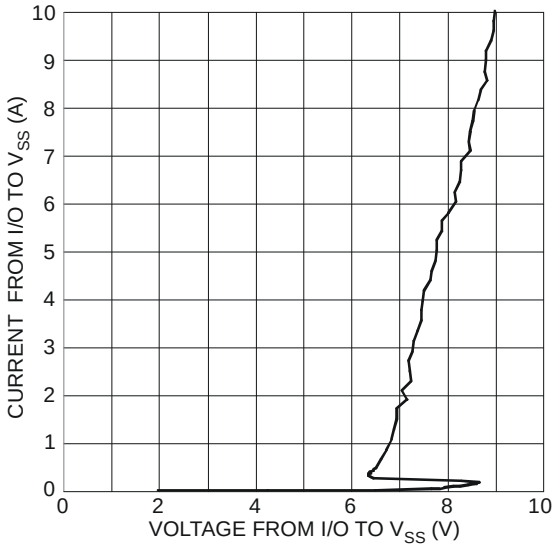


Figure 7 Current vs. Voltage

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

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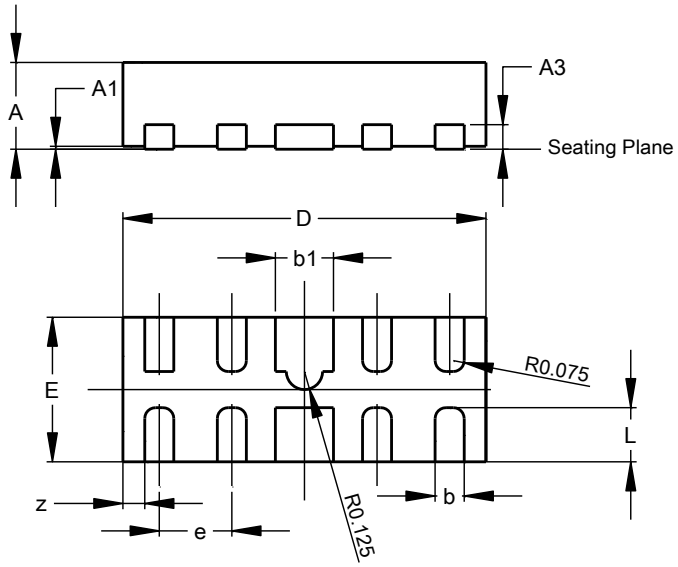

U-DFN2510-10			
Dim	**Min**	**Max**	**Typ**
A	0.545	0.605	0.575
A1	0.00	0.05	0.03
A3	-	-	0.13
b	0.15	0.25	0.20
b1	0.35	0.45	0.40
D	2.450	2.575	2.500
e	-	-	0.50
E	0.950	1.075	1.000
L	0.325	0.425	0.375
z	-	-	0.150
All Dimensions in mm			

Suggested Pad Layout

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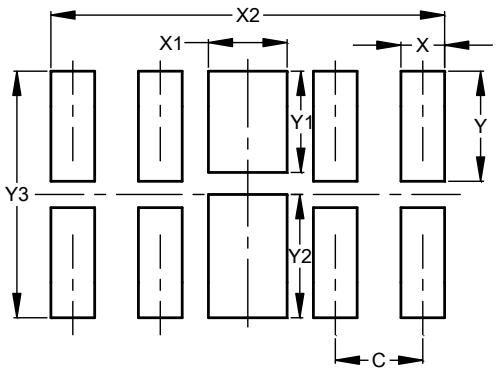

Dimensions	Value (in mm)
C	0.500
X	0.250
X1	0.450
X2	2.250
Y	0.625
Y1	0.575
Y2	0.700
Y3	1.400

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