APR34330C

SECONDARY SIDE SYNCHRONOUS RECTIFICATION SWITCHER

Description

APR34330C is a secondary side Combo IC, which combines an N-Channel MOSFET and a driver circuit designed for synchronous rectification (SR) in DCM operation. It also integrates output voltage detect function for primary side control system.

The N-Channel MOSFET has been optimized for low gate charge, low $R_{DS(ON)}$, fast switching speed and body diode reverse recovery performance.

The synchronous rectification can effectively reduce the secondary side rectifier power dissipation and provide high performance solution. By sensing MOSFET drain-to-source voltage, APR34330C can output ideal drive signal with less external components. It can provide high performance solution for 5V output voltage application.

Same as AP4341, APR34330C detects the output voltage and provides a periodical signal when the output voltage is lower than a certain threshold. By fast response to secondary side voltage, APR34330C can effectively improve the transient performance of primary side control system.

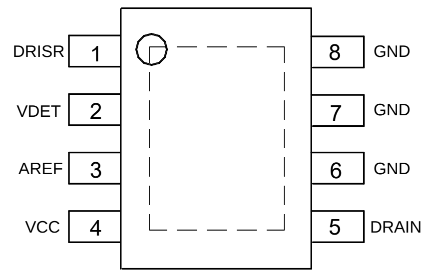
The APR34330C is available in SO-8EP package.

Features

- Synchronous Rectification for DCM Operation Flyback
- Eliminate Resonant Ring Interference
- Fast Detector of Supply Voltages
- Fewest External Components
- **Totally Lead-free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Pin Assignments

(Top View)



Note: The DRAIN pin of internal MOSFET is exposed PAD, which is at the bottom of IC (the dashed box). The secondary current should flow from GND(pin 6,7,8) to this exposed PAD.

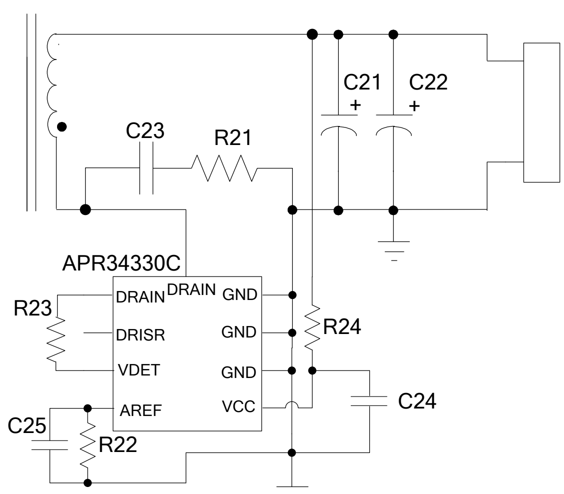
SO-8EP

Applications

- Adapters/Chargers for Cell/Cordless Phones, ADSL Modems, MP3 and Other Portable Apparatus
- Standby and Auxiliary Power Supplies

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



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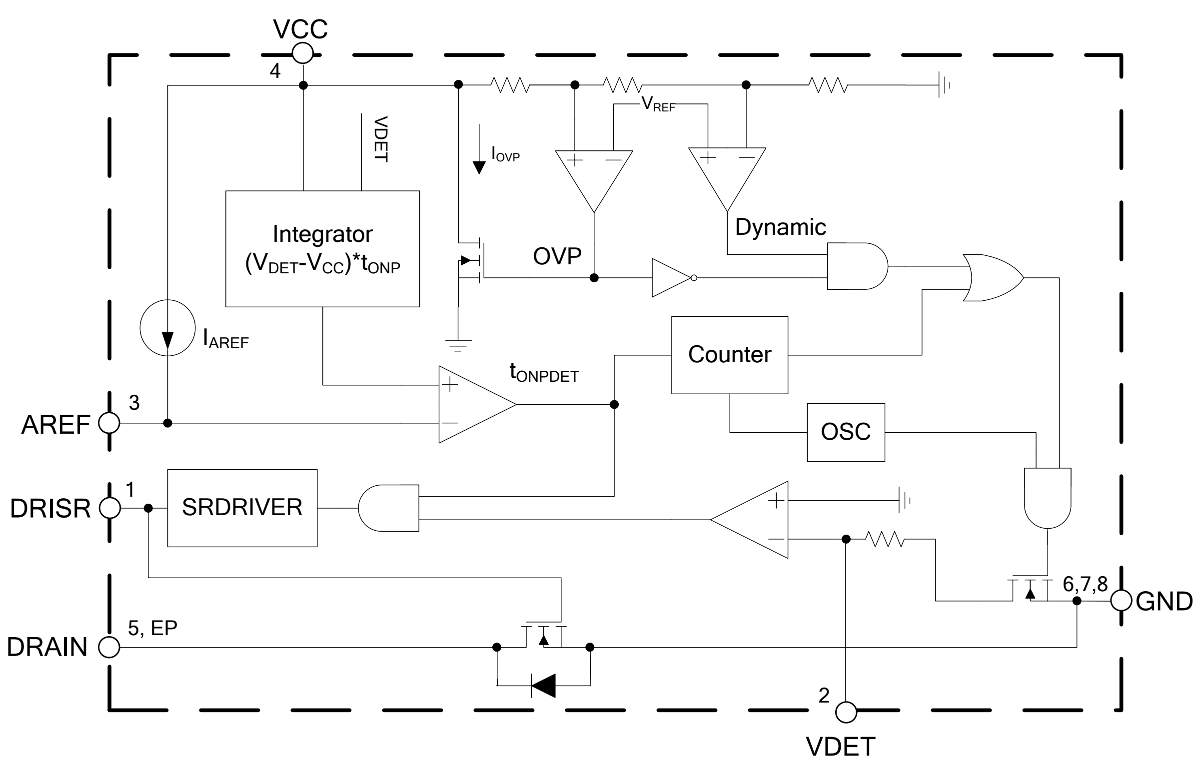
Pin Descriptions

Pin Number	Pin Name	Function
1	DRISR	Synchronous rectification MOSFET drive
2	VDET	Synchronous rectification sense input and dynamic function output, connected to DRAIN through a resistor
3	AREF	Program a voltage reference with a resistor from AREF to GND, to enable synchronous rectification MOSFET drive signal
4	VCC	Power supply, connected with system output
5	DRAIN	Drain pin of internal MOSFET. The Drain voltage signal can obtain from this pin.
6,7,8	GND	Source pin of internal MOSFET, connected to Ground
Exposed PAD	DRAIN	Drain pin of internal MOSFET. The secondary current should flow from GND (pin 6.7.8) to this DRAIN pad.

Functional Block Diagram



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Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.3 to 7.5	V
V_{DET}, V_{DRAIN}	Voltage at VDET, DRAIN Pin	-2 to 50	V
V_{AREF}, V_{DRISR}	Voltage at AREF, DRISR Pin	-0.3 to 6	V
I_D	Continuous Drain Current	15	A
I_{DM}	Pulsed Drain Current	60	A
P_D	Power Dissipation at T_A=+25ºC	2	W
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 5)	56	ºC/W
θ_{JC}	Thermal Resistance (Junction to Case) (Note 5)	14	ºC/W
T_J	Operating Junction Temperature	+150	ºC
T_{STG}	Storage Temperature	-65 to +150	ºC
T_{LEAD}	Lead Temperature (Soldering, 10 sec)	+300	ºC

Notes: 4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

5. FR-4 substrate PC board, 2oz copper, with 1 inch^2 pad layout.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	3.3	6	V
T_A	Ambient Temperature	-40	+85	ºC

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Electrical Characteristics (@T_A = +25°C, V_{CC}=5V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage (VCC Pin)						
$I_{STARTUP}$	Startup Current	V_{CC}=$V_{STARTUP}$-0.1V	–	100	150	μA
I_{OP}	Operating Current	VDET pin floating V_{CC}=$V_{TRIGGER}$+20mV	40	100	150	μA
$V_{STARTUP}$	Startup Voltage	–	2.6	3.1	3.4	V
–	UVLO	–	2.3	2.8	3.1	V
Dynamic Output Section/Oscillator Section						
$V_{TRIGGER}$	Internal Trigger Voltage	–	5.1	5.15	5.2	V
–	Duty Cycle	–	4	15	18	%
t_{OSC}	Oscillation Period	V_{CC}=5V	18	30	37.5	μs
$I_{TRIGGER}$	Internal Trigger Current	V_{CC}=$V_{TRIGGER}$, VCC/VDET pin is separately connected to a 20Ω resistor	30	60	80	mA
t_{DIS}	Minimum Period	–	18	30	37.5	ms
V_{DIS}	Discharge Voltage	–	5.13	5.3	5.38	V
I_{DIS}	Discharge Current	V_{CC}=V_{DIS}+0.1V	1.5	3	4.5	mA
V_{DIS}-$V_{TRIGGER}$	Trigger Discharger Gap	–	30	110	–	mV
V_{OVP}	Overshoot Voltage for Discharge	–	5.64	5.74	5.84	V
I_{OVP}	Overshoot Current for Discharge	V_{CC}=V_{OVP}+0.1V, VCC pin is connected to a 20Ω resistor	40	–	100	mA
Synchronous Voltage Detect						
V_{THON}	Gate Turn On Threshold	–	0	–	1	V
V_{THOFF}	Gate Turn Off Threshold	–	-25	-15	-5	mV
t_{DON}	Turn-on Delay Time	From V_{THON} to V_{DRISR}=1V	–	70	130	ns
t_{DOFF}	Turn-off Propagation Delay Time	From V_{THOFF} to V_{DRISR}=3V	–	100	150	ns
t_{RG}	Gate Turn-on Rising Time	From 1V to 3V, C_L=4.7nF	–	50	100	ns
t_{FG}	Gate Turn-off Falling Time	From 3V to 1V, C_L=4.7nF	–	50	100	ns
t_{LEB_S}	Minimum On Time	(V_{DET}-V_{CC})*t_{ONP} = 25Vμs	0.9	1.8	2.7	μs
t_{LEB_L}		(V_{DET}-V_{CC})*t_{ONP} = 50Vμs	–	–	6.5	
V_{DRISR_HIGH}	Drive Output Voltage	V_{CC}=5V	3.7	–	–	V
V_{S_MIN}	SR Minimum Operating Voltage (Note 6)	–	–	–	4.5	V
t_{OVP_LAST}	Added OVP Discharge Time	–	–	2.0	–	ms
Kqs	(Note 7)	(V_{DET}-V_{CC})*t_{ONP} = 25Vμs	0.325	–	0.515	mA*μs

Notes: 6. This item specifies the minimum SR operating voltage of V_{IN_DC}, $V_{IN\_DC} \geq N_{PS}$*V_{S_MIN}.
7. This item is used to specify the value of R_{AREF}.

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Electrical Characteristics (@T_A =+25°C, unless otherwise specified. Cont.)

MOSFET Static Characteristics

Parameters	Symbol	Conditions	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	$V_{DSS(BR)}$	V_{GS}=0V, I_D=0.25mA	50	56	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=0.25mA	–	0.85	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V, V_{GS}=0V	–	6	1000	nA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=10V, V_{DS}=0V	–	1	±10	μA
Drain to Source On-state Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=3A	–	32	36	mΩ
		V_{GS}=4.5V, I_D=15A	–	36	42	

MOSFET Dynamic Characteristics

Parameters	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	–	661	–	pF
Output Capacitance	C_{oss}		–	52	–	
Reverse Transfer Capacitance	C_{rss}		–	45	–	
Gate to Source Charge	Q_{gs}	V_{GS}=0V to 10V, V_{DD}=25V, I_D=15A	–	1.4	–	nC
Gate to Drain Charge (Miller Charger)	Q_{gd}		–	2.9	–	
Total Gate Charge	Q_g	V_{GS}=4.5V	–	7.5	–	
Gate Resistance	R_g	–	–	2.15	–	Ω

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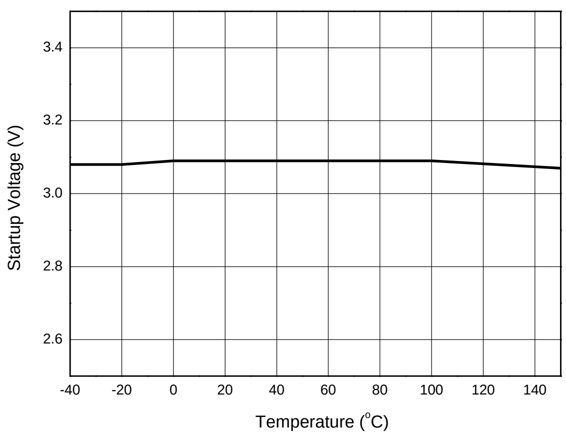
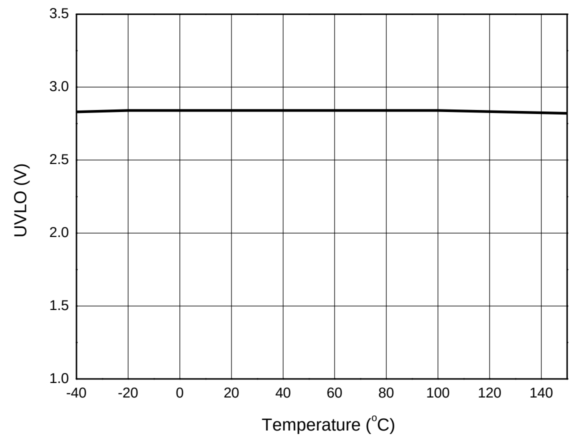
Performance Characteristics

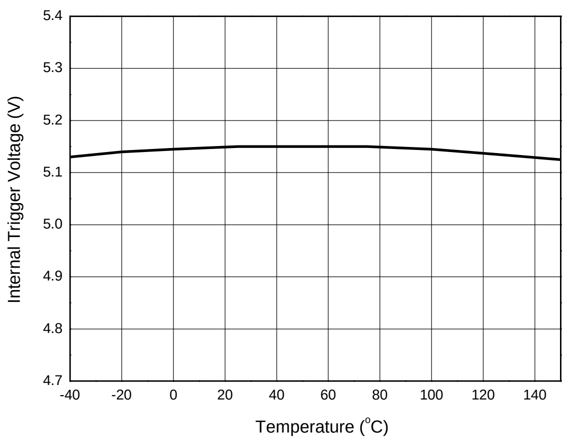
Startup Voltage vs. Temperature



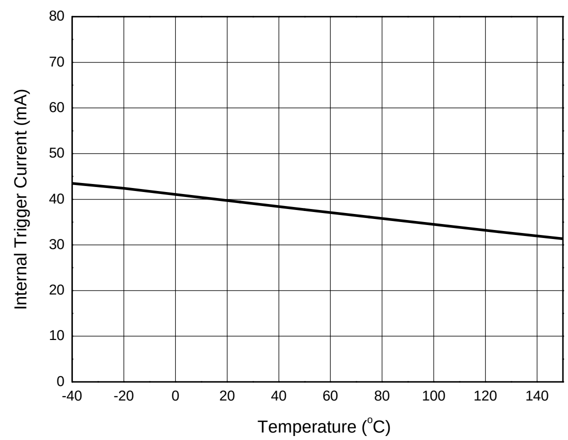
UVLO vs. Temperature



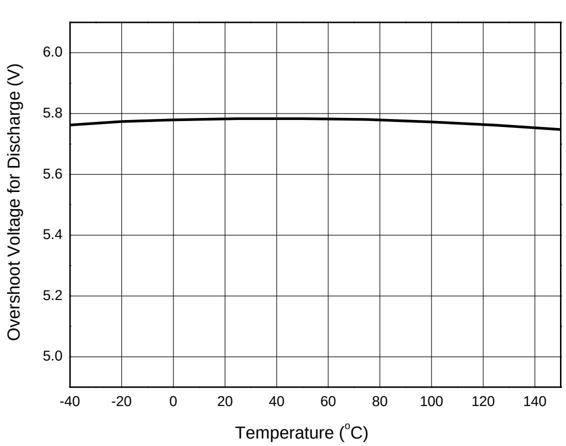
Internal Trigger Voltage vs. Temperature



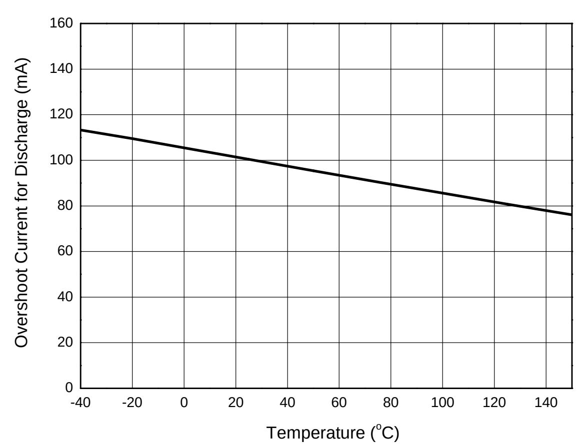
Internal Trigger Current vs. Temperature



Overshoot Voltage for Discharge vs. Temperature



Overshoot Current for Discharge vs. Temperature



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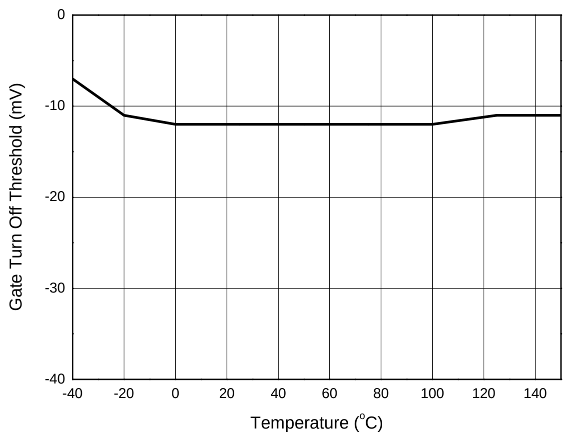
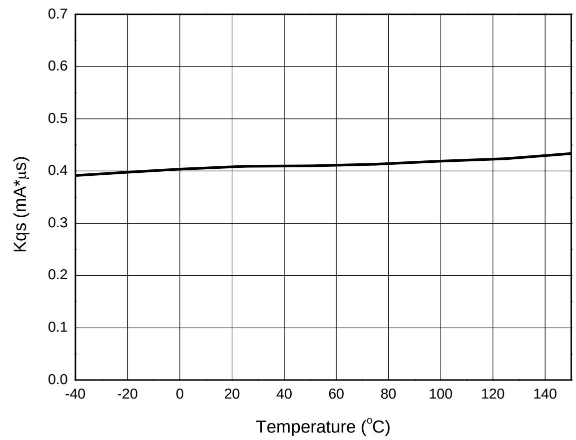
Performance Characteristics (Cont.)

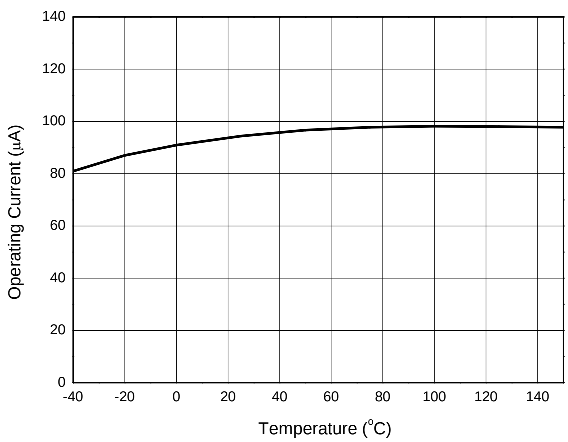
Gate Turn Off Threshold vs. Temperature



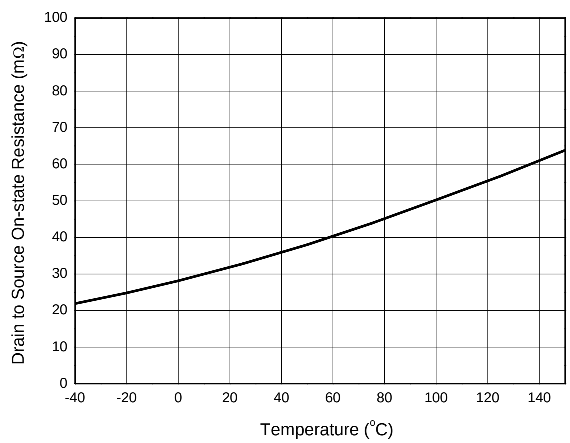
Kqs (See Note 7) vs. Temperature



Operating Current vs. Temperature



Drain to Source On-state Resistance vs. Temperature



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Output Voltage Detect Function Description

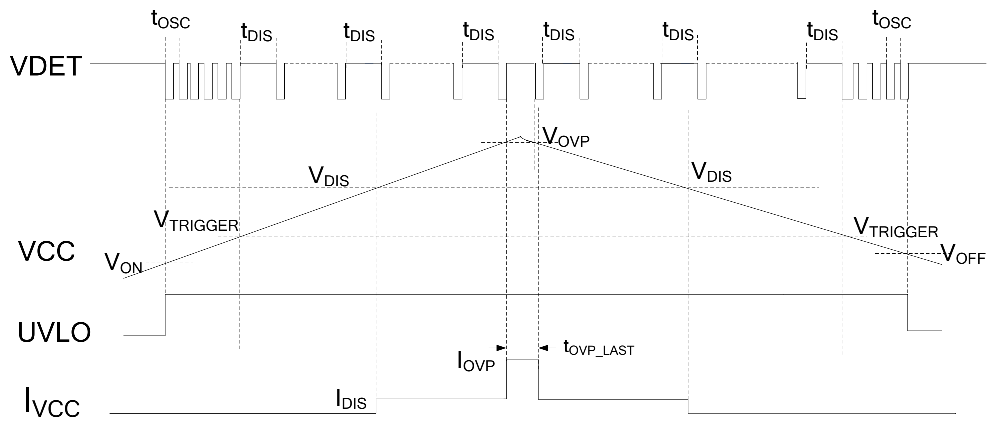

Figure 1. Typical Waveforms of APR34330C

When V_{CC} is beyond power-on voltage (V_{ON}), the APR34330C starts up. The VDET pin asserts a periodical pulse and the oscillation period is t_{OSC}. When V_{CC} is beyond the trigger voltage ($V_{TRIGGER}$), the periodical pulse at VDET pin is discontinued. When V_{CC} is beyond the discharge voltage (V_{DIS}), the discharge circuit will be enabled, and a 3mA current (I_{DIS}) will flow into VCC pin. When V_{CC} is higher than the overshoot voltage (V_{OVP}), the APR34330C will enable a discharge circuit, the discharge current (I_{OVP}) will last t_{OVP_LAST} time. After the t_{OVP_LAST} time, APR34330C will stop the discharge current and detect V_{CC} voltage again. If V_{CC} is still higher than V_{OVP}, the t_{OVP_LAST} time discharge current will be enabled again. Once the OVP discharge current is asserted, the periodical pulse at VDET pin will be disabled.

When the V_{CC} falls below the power-off voltage (V_{OFF}), the APR34330C will shut down.

Operation Description

MOSFET Driver

The operation of the SR is described with timing diagram shown in Figure 2. APR34330C monitors the MOSFET drain-source voltage. When the drain voltage is lower than the turn-on threshold voltage V_{THON}, the IC outputs a positive drive voltage after a turn-on delay time (t_{DON}). The MOSFET will turn on and the current will transfer from the body diode into the MOSFET's channel.

In the process of drain current decreasing linearly toward zero, the drain-source voltage rises synchronically. When it rises over the turn off threshold voltage V_{THOFF}, APR34330C pulls the drive signal down after a turn-off delay (t_{DOFF}).

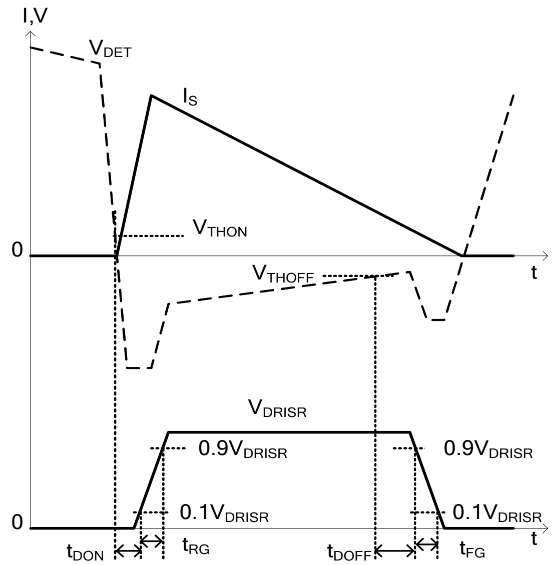

Figure 2. Typical Waveforms of APR34330C

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Operation Description (Cont.)

Minimum On Time

When the controlled MOSFET gate is turned on, some ringing noise is generated. The minimum on-time timer blanks the V_{THOFF} comparator, keeping the controlled MOSFET on for at least the minimum on time. If V_{THOFF} falls below the threshold before minimum on time expires, the MOSFET will keep on until the end of the minimum on time.

The minimum on time is in direct proportion to the $(V_{DET}-V_{CC})*t_{ONP}$. When $(V_{DET}-V_{CC})*t_{ONP}$=5V*5µs, the minimum on time is about 1.8µs.

The Value and Meaning of AREF Resistor

As to DCM operation Flyback converter, after secondary rectifier stops conduction the primary MOSFET Drain-to-source ringing waveform is resulted from the resonant of primary inductance and equivalent switch device output capacitance. This ringing waveform probably leads to Synchronous Rectifier error conduction. To avoid this fault happening, APR34330C has a special function design by means of volt-second product detecting. From the sensed voltage of VDET pin to see, the volt-second product of voltage above VCC at primary switch on time is much higher than the volt-second product of each cycle ringing voltage above V_{CC}. Therefore, before every time Synchronous Rectifier turning on, APR34330C judges if the detected volt-second product of VDET voltage above V_{CC} is higher than a threshold and then turn on synchronous Rectifier. The purpose of AREF resistor is to determine the volt-second product threshold. APR34330C has a parameter, Kqs, which converts R_{AREF} value to volt-second product,

$$Area2 = R_{AREF} * Kqs$$

In general, Area1 and Area3 value depend on system design and are always fixed after system design frozen. As to BCD PSR design, the Area1 value changes with primary peak current value and Area3 value generally keeps constant at all of conditions. So the AREF resistor design should consider the worst case, the minimum primary peak current condition. Since of system design parameter distribution, Areas1 and Area3 have moderate tolerance. So Area2 should be designed between the middle of Area1 and Area3 to keep enough design margin.

Note: To keep the volt-second product threshold stable, a capacitor is suggested to parallel with AREF resistor. And the recommended value of this capacitor is 100nF.

$$Area3 < R_{AREF} * Kqs < Area1$$

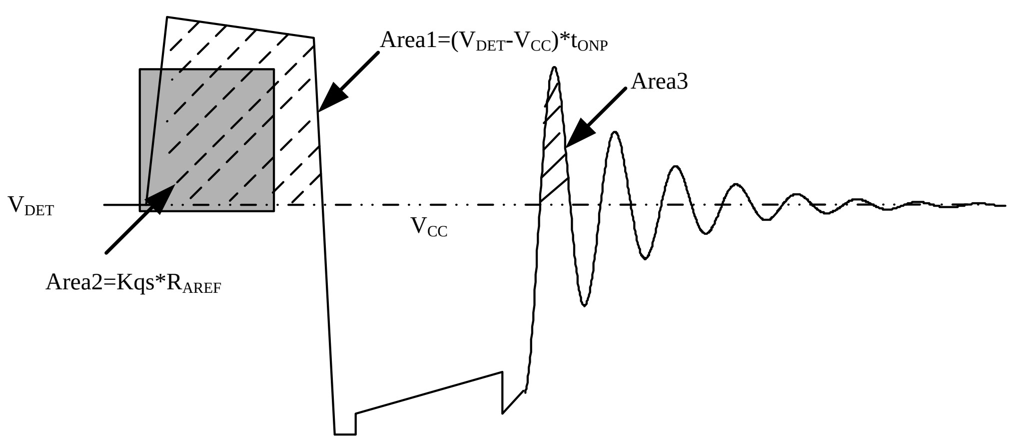

Figure 3. AREF Function

SR Minimum Operating Voltage

APR34330C sets a minimum SR operating voltage by comparing the difference between V_{DET} and output voltage (V_{CC}). The value of $V_{DET}–V_{CC}$ must be higher than its internal reference, then APR34330C will begin to integrate the area of $(V_{DET}–V_{CC})*t_{ONP}$. If not, the area integrating will not begin and the SR driver will be disabled.

SR Turning off Timing Impact on PSR CV Sampling

As to synchronous rectification on Flyback power system, SR MOSFET need to turn off in advance of secondary side current decreasing to zero to avoid current flowing reversely. When SR turns off in advance, the secondary current will flow through the body diode. The SR turning off time is determined by the V_{THOFF} at a fixed system. When V_{THOFF} is more close to zero, the SR turning on time gets longer and body diode conduction time gets shorter. Since of the different voltage drop between SR MOSFET and body diode, the PSR feedback signal V_{FB} appears a voltage jump at the time of SR MOSFET turning off. If the PSR CV sampling time t_{SAMPLE} is close to even behind this voltage jump time, there will be system unstable operation issue or the lower output voltage issue.

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Operation Description (Cont.)

To ensure stable operating of system, it must be met:

$t_{BODYDIODE} < t_{ONS} * (1 - t_{SAMPLE})$

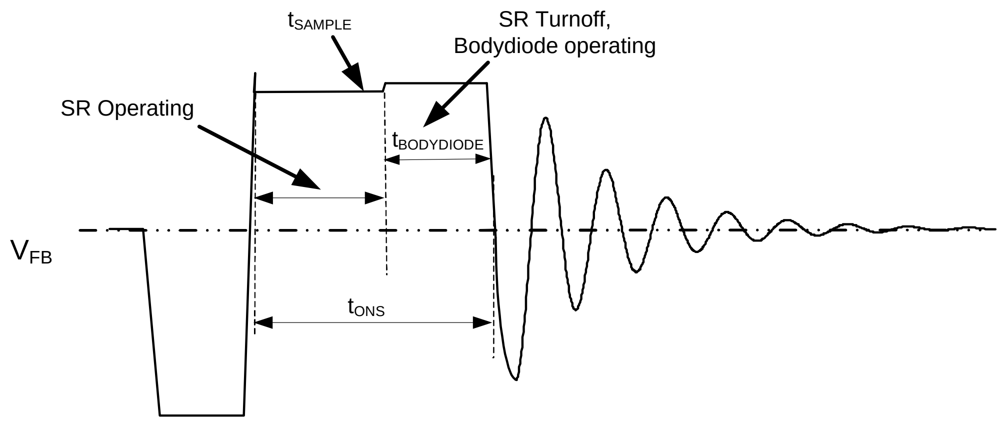
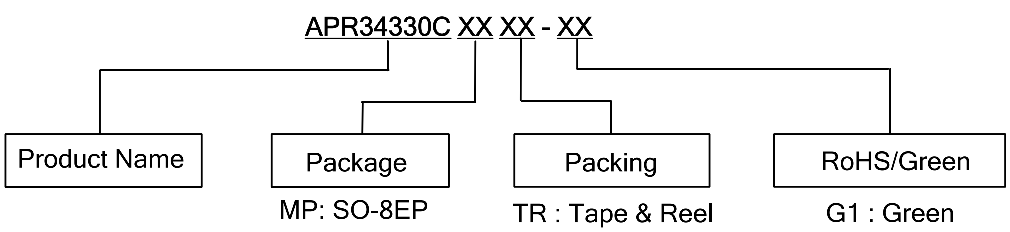


Figure 4. SR Turning off Timing Impact on PSR CV Sampling

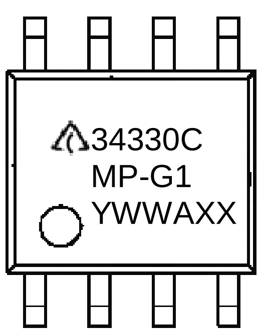
Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing
SO-8EP	-40 to +85°C	APR34330CMPTR-G1	34330CMP-G1	4000/Tape & Reel

Marking Information

(Top View)



First and Second Lines: Logo and Marking ID
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch No.

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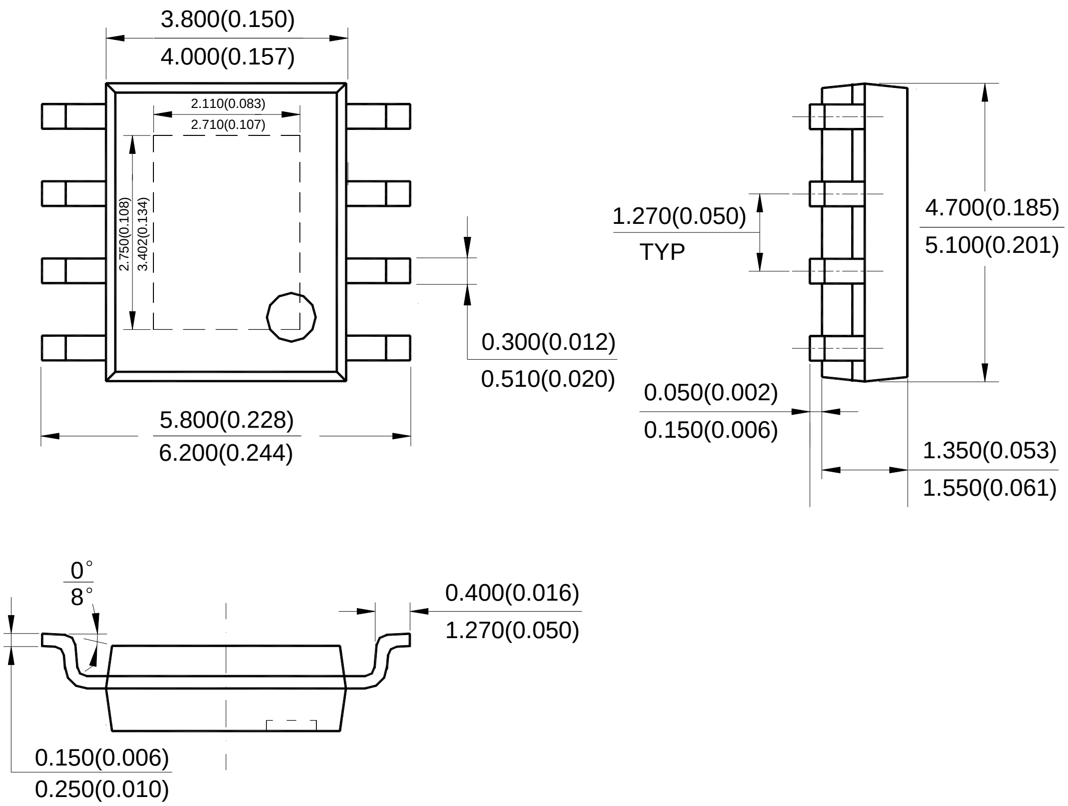
Package Outline Dimensions (All dimensions in mm(inch).)

(1) Package Type: SO-8EP



Note: Eject hole, oriented hole and mold mark is optional.

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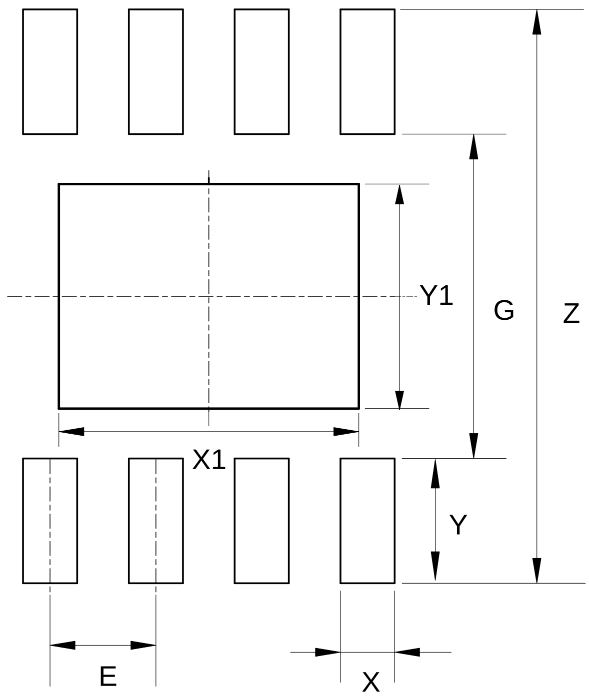
Suggested Pad Layout

(1) Package Type: SO-8EP



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	X1 (mm)/(inch)	Y1 (mm)/(inch)	E (mm)/(inch)
Value	6.900/0.272	3.900/0.154	0.650/0.026	1.500/0.059	3.600/0.142	2.700/0.106	1.270/0.050

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