

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _A = +25°C
20V	0.4Ω @ V _{GS} = 4.5V	1.3A
	0.5Ω @ V _{GS} = 2.5V	1.2A
	0.7Ω @ V _{GS} = 1.8V	1.0A

Features and Benefits

- Footprint of just 0.6mm² – Thirteen Times Smaller than SOT23
- 0.4mm Profile – Ideal for Low Profile Applications
- Low Gate Threshold Voltage
- Fast Switching Speed
- **ESD Protected Gate**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DMN2451UFB4Q is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**

<https://www.diodes.com/quality/product-definitions/>

Description and Applications

This MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

- Load Switch

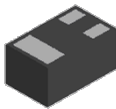
Mechanical Data

- Case: X2-DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Lead-Frame. Solderable per MIL-STD-202, Method 208 @4
- Weight: 0.001 grams (Approximate)

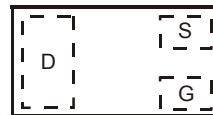


ESD Protected Gate

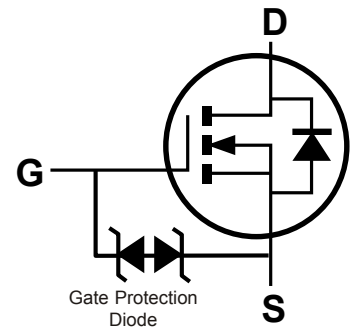
X2-DFN1006-3



Bottom View



Top View
Internal Schematic




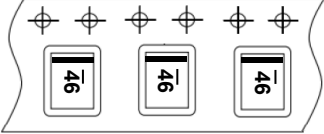
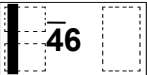
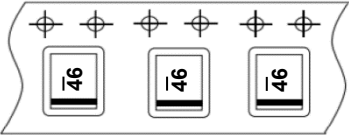
Equivalent Circuit

Ordering Information (Note 4)

Part Number	Marking	Reel Size (inches)	Tape Width (mm)	Tape Pitch (mm)	Packaging
DMN2451UFB4Q-7B	46	7	8	2	10,000/Reel
DMN2451UFB4Q-7R	46	7	8	4	3,000/Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

<p>DMN2451UFB4Q-7R</p>	<div style="text-align: center;">  <p>Top View Bar Denotes Gate and Source Side</p> </div> <div style="text-align: right; margin-top: 20px;"> <p>$\overline{46}$ = Part Marking Code</p> </div> <div style="text-align: center; margin-top: 20px;">  </div>
<p>DMN2451UFB4Q-7B</p>	<div style="text-align: center;">  <p>Top View Bar Denotes Gate and Source Side</p> </div> <div style="text-align: right; margin-top: 20px;"> <p>$\overline{46}$ = Part Marking Code</p> </div> <div style="text-align: center; margin-top: 20px;">  </div>

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	20	V
Gate-Source Voltage			V_{GSS}	± 12	V
Continuous Drain Current (Note 6) $V_{GS} = 4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	I_D	1.3	A
		$T_A = +70^\circ\text{C}$		1.0	
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)			I_{DM}	3	A

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	0.66	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	189	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)	P_D	1.1	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	113	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	—	—	100	nA	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 1.0	μA	$V_{GS} = \pm 4.5\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.5	—	1.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	0.26	0.4	Ω	$V_{GS} = 4.5\text{V}, I_D = 600\text{mA}$
		—	0.35	0.5		$V_{GS} = 2.5\text{V}, I_D = 500\text{mA}$
		—	0.5	0.7		$V_{GS} = 1.8\text{V}, I_D = 350\text{mA}$
		—	—	—		$V_{GS} = 0\text{V}, I_S = 150\text{mA}$
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	$V_{GS} = 0\text{V}, I_S = 150\text{mA}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	32	—	pF	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	5.5	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	3.7	—	pF	
Gate Resistance	R_g	—	86	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	3.4	—	nC	$V_{DS} = 10\text{V}, I_D = 250\text{mA}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	—	6.4	—	nC	
Gate-Source Charge	Q_{gs}	—	0.4	—	nC	
Gate-Drain Charge	Q_{gd}	—	1.3	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	5.5	—	ns	$V_{DD} = 10\text{V}, V_{GS} = 4.5\text{V}, R_L = 47\Omega, R_g = 10\Omega, I_D = 200\text{mA}$
Turn-On Rise Time	t_R	—	2.9	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	11	—	ns	
Turn-Off Fall Time	t_F	—	12	—	ns	

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 25mm X 25mm square copper plate.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

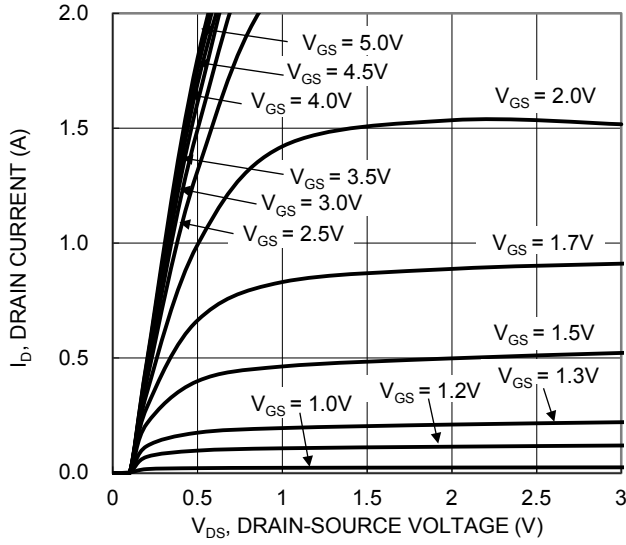


Figure 1. Typical Output Characteristic

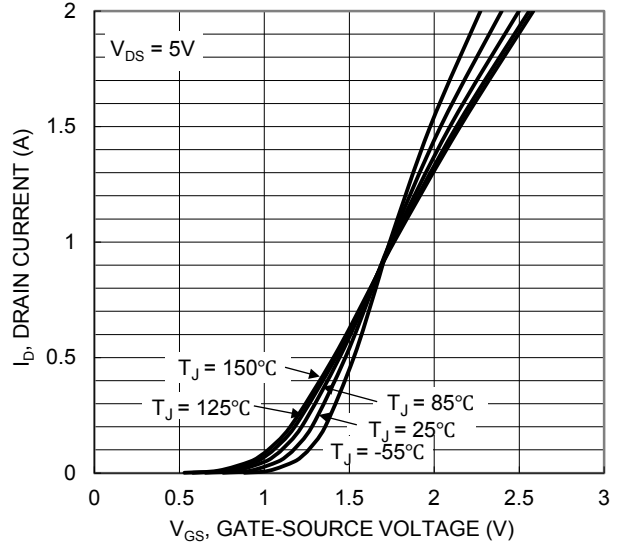


Figure 2. Typical Transfer Characteristic

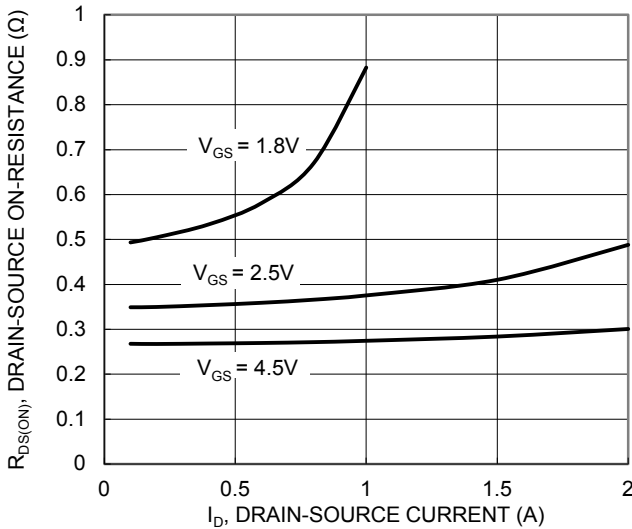


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

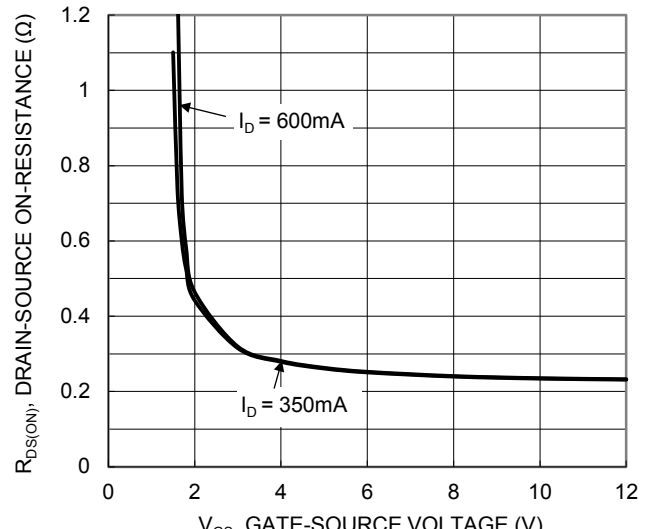


Figure 4. Typical Transfer Characteristic

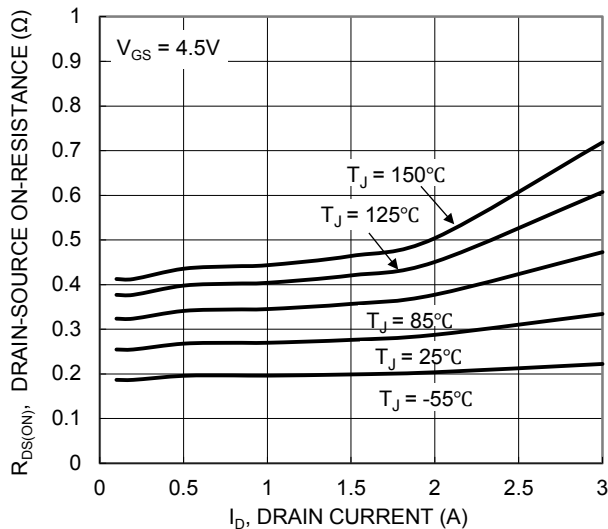


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

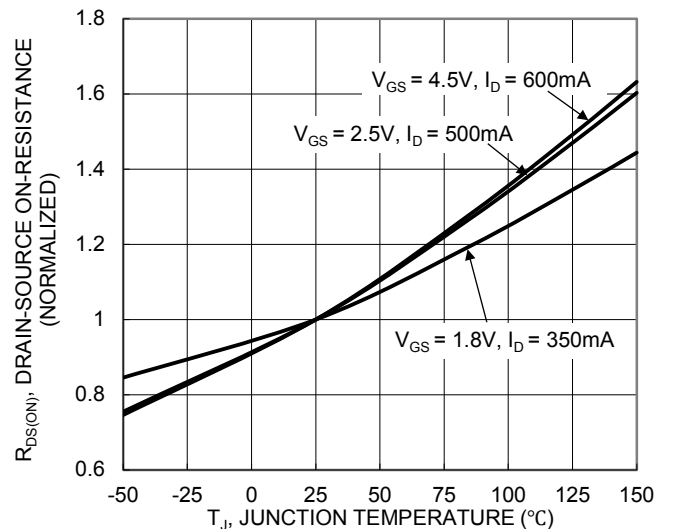


Figure 6. On-Resistance Variation with Junction Temperature

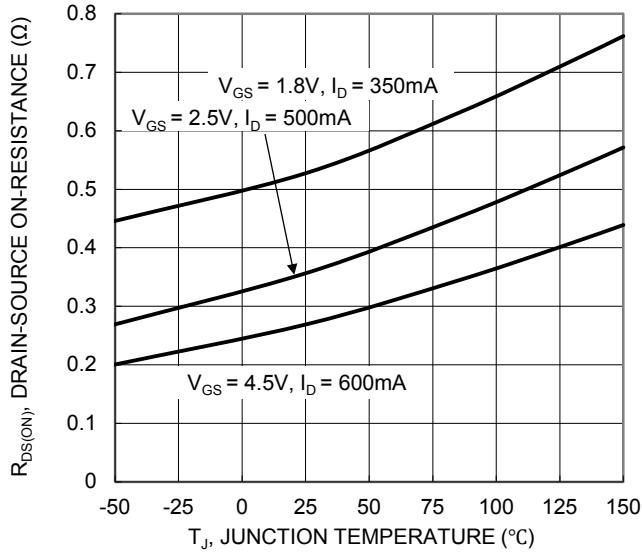


Figure 7. On-Resistance Variation with Junction Temperature

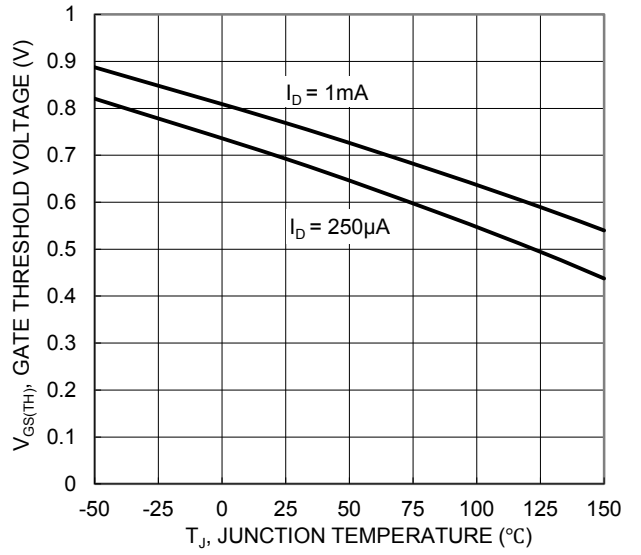


Figure 8. Gate Threshold Variation vs. Junction Temperature

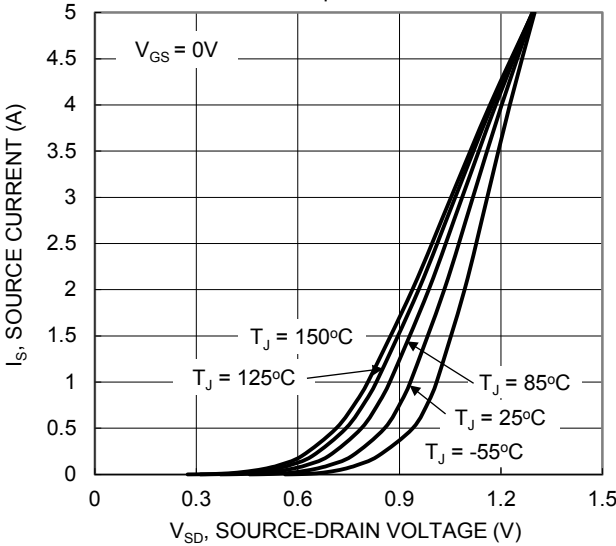


Figure 9. Diode Forward Voltage vs. Current

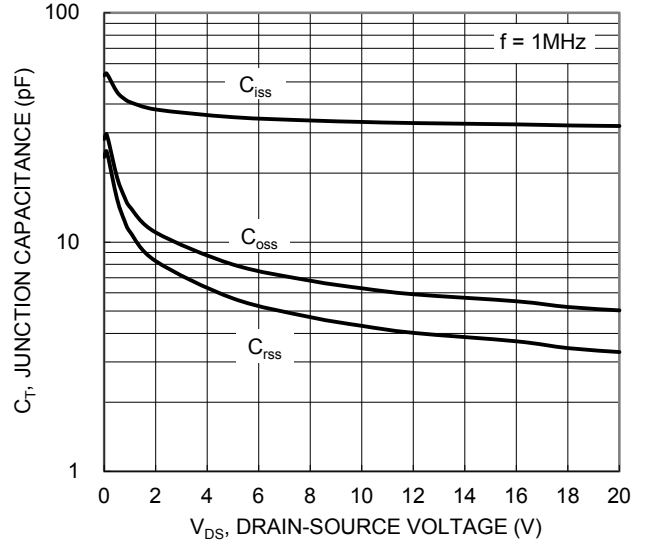


Figure 10. Typical Junction Capacitance

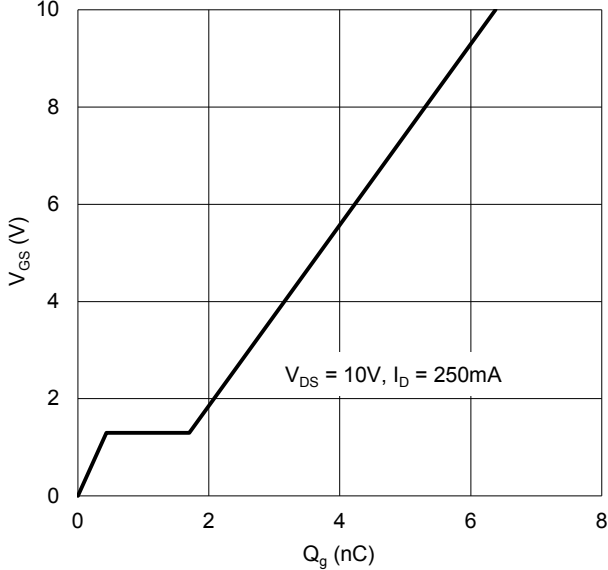


Figure 11. Gate Charge

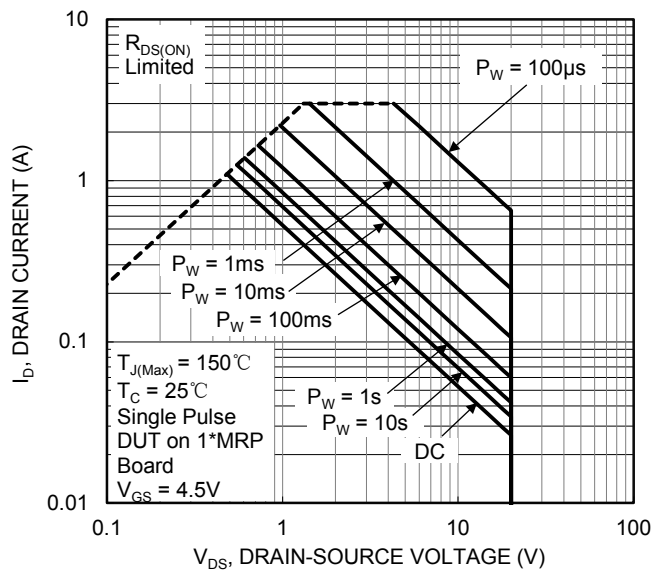


Figure 12. SOA, Safe Operation Area

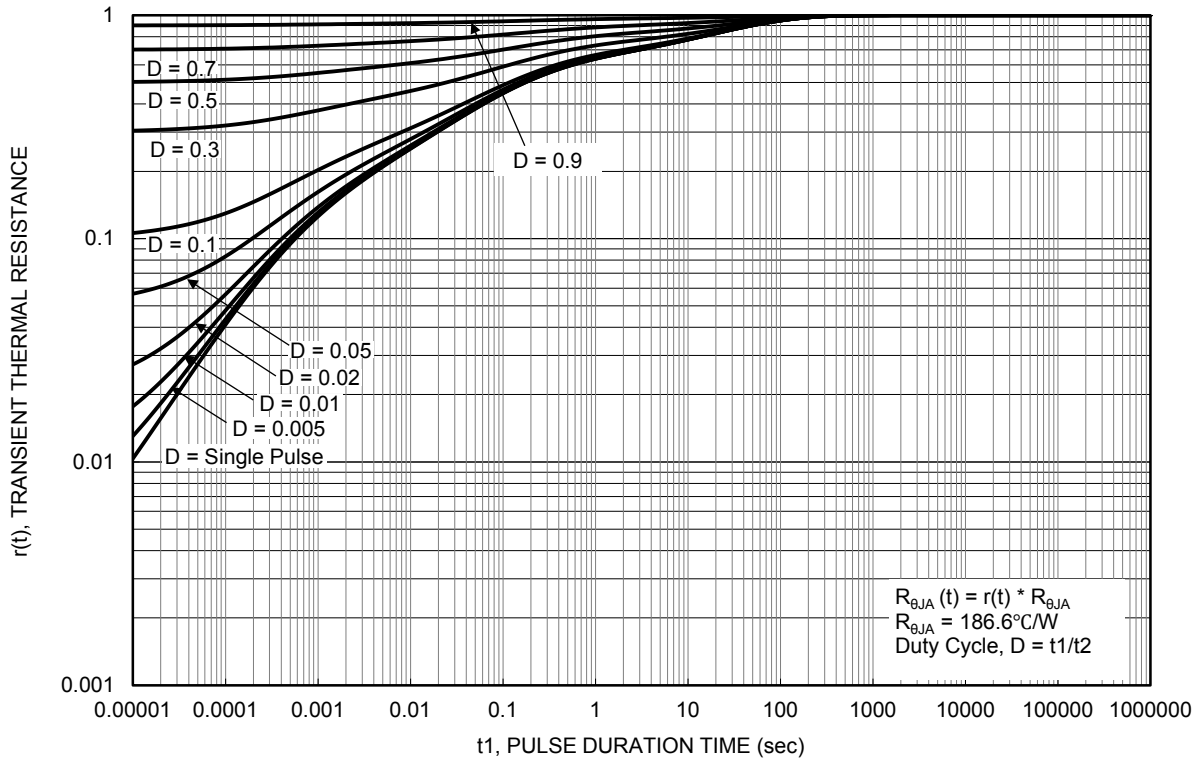
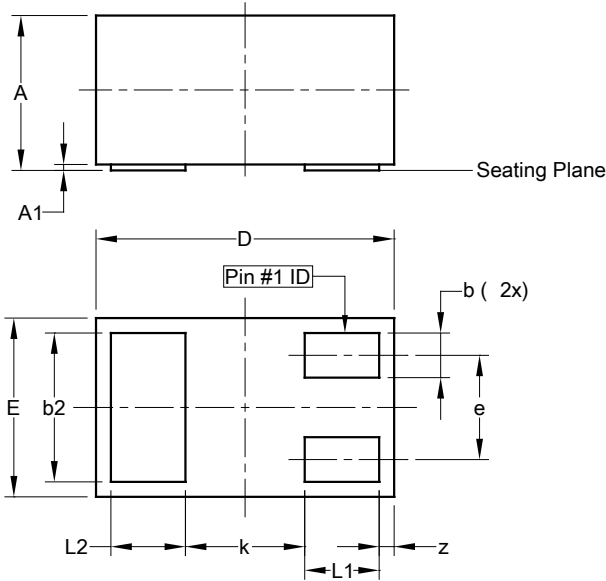


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DFN1006-3

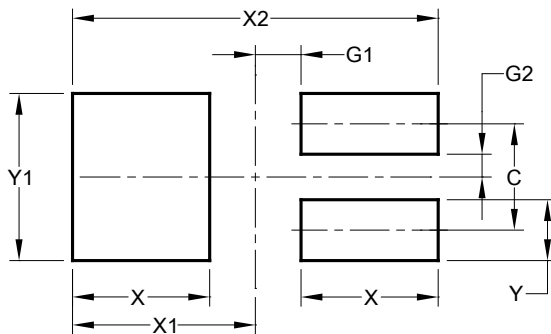


X2-DFN1006-3			
Dim	Min	Max	Typ
A	—	0.40	—
A1	0.00	0.05	0.03
b	0.10	0.20	0.15
b2	0.45	0.55	0.50
D	0.95	1.05	1.00
E	0.55	0.65	0.60
e	-	-	0.35
L1	0.20	0.30	0.25
L2	0.20	0.30	0.25
k	-	-	0.40
z	0.02	0.08	0.05
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DFN1006-3



Dimensions	Value (in mm)
C	0.350
G1	0.150
G2	0.075
X	0.450
X1	0.600
X2	1.200
Y	0.200
Y1	0.550

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