

**DUAL 24V N-CHANNEL ENHANCEMENT MODE MOSFET**  
**PowerDI3333-8 (Type UXC)**
**Product Summary**

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> max	I <sub>D</sub> T <sub>A</sub> = +25°C
24V	7mΩ @ V <sub>GS</sub> = 10V	50
	8mΩ @ V <sub>GS</sub> = 4.5V	47
	10mΩ @ V <sub>GS</sub> = 3.7V	42
	12mΩ @ V <sub>GS</sub> = 2.5V	38

**Description**

This new generation MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

**Applications**

- Power Management Functions
- Analog Switch

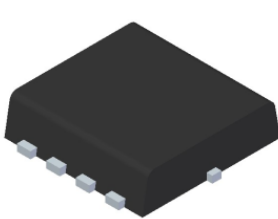
**Features**

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

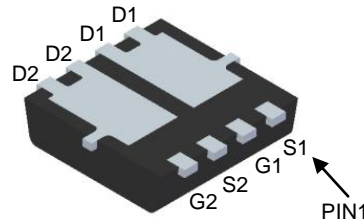
**Mechanical Data**

- Case: PowerDI<sup>®</sup> 3333-8 (Type UXC)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 <sup>Ⓔ3</sup>
- Weight: 0.072 grams (Approximate)

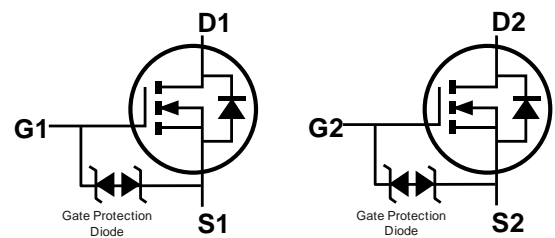
PowerDI3333-8 (Type UXC)



Top View



Bottom View

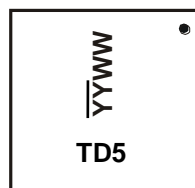


Equivalent Circuit

**Ordering Information** (Note 4)

Part Number	Case	Packaging
DMT2005UDV-7	PowerDI3333-8 (Type UXC)	2,000/Tape & Reel
DMT2005UDV-13	PowerDI3333-8 (Type UXC)	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

**Marking Information**


TD5 = Product Type Marking Code  
 YYWW = Date Code Marking  
 YY = Last Two Digits of Year (ex: 18 for 2018)  
 WW = Week Code (01 to 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V <sub>DSS</sub>	24	V
Gate-Source Voltage			V <sub>GSS</sub>	±12	V
Continuous Drain Current (Note 7) V <sub>GS</sub> = 10V	Steady State	T <sub>C</sub> = +25°C T <sub>C</sub> = +70°C	I <sub>D</sub>	50 40	A
Maximum Body Diode Forward Current (Note 7)			I <sub>S</sub>	30	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I <sub>DM</sub>	70	A
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)			I <sub>SM</sub>	70	A
Avalanche Current (Note 8) L = 0.1mH			I <sub>AS</sub>	26	A
Avalanche Energy (Note 8) L = 0.1mH			E <sub>AS</sub>	34	mJ

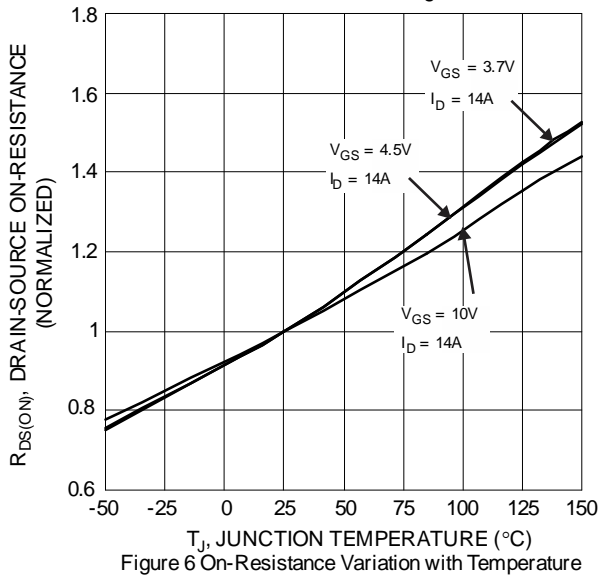
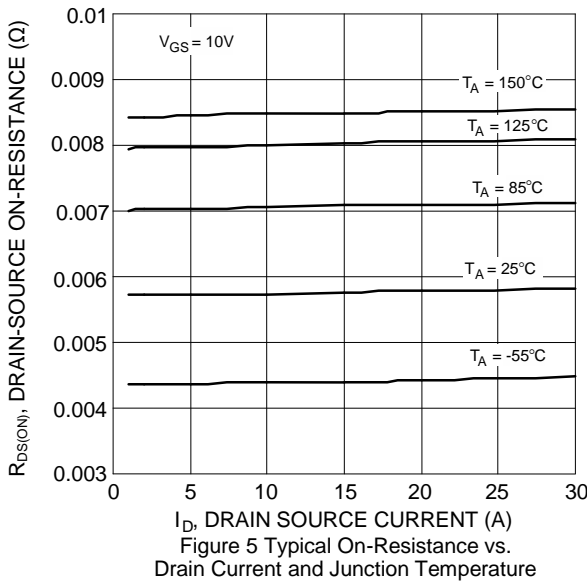
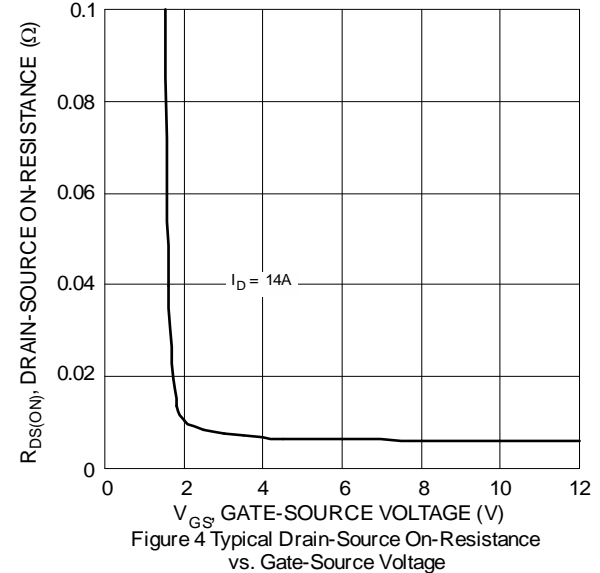
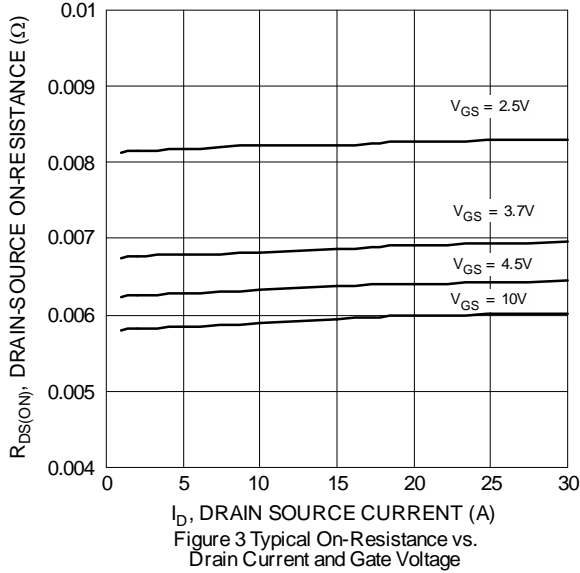
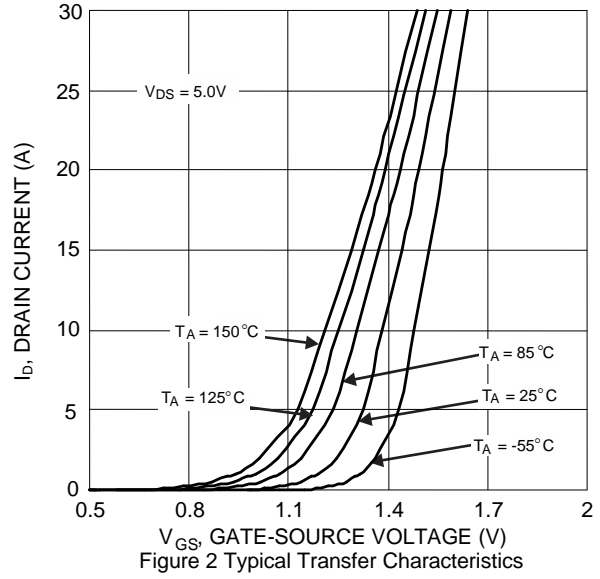
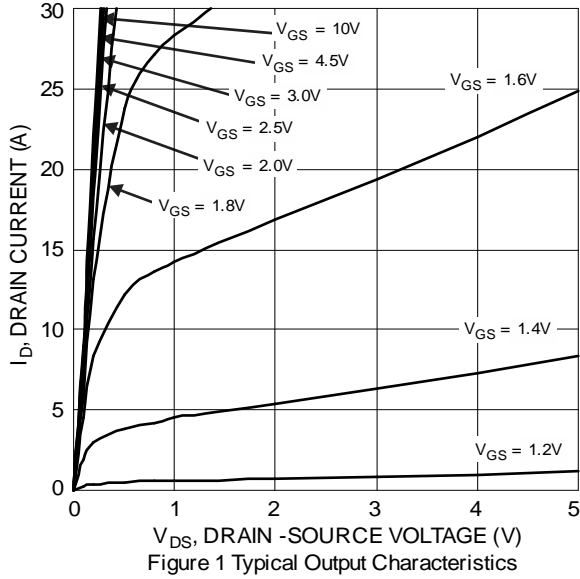
**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T <sub>A</sub> = +25°C	P <sub>D</sub>	0.9	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	R <sub>θJA</sub>	141	°C/W
Total Power Dissipation (Note 6)	T <sub>A</sub> = +25°C	P <sub>D</sub>	1.9	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	R <sub>θJA</sub>	66	°C/W
Thermal Resistance, Junction to Case (Note 7)		R <sub>θJC</sub>	4.8	°C/W
Operating and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 9)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	24	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA
Zero Gate Voltage Drain Current (T <sub>J</sub> = +25°C)	I <sub>DSS</sub>	—	—	1	µA	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±10	µA	V <sub>GS</sub> = ±10V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 9)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	0.5	—	1.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	5.9	7.0	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 14A
		—	6.3	8.0		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 14A
		—	6.7	10.0		V <sub>GS</sub> = 3.7V, I <sub>D</sub> = 14A
		—	8.9	12.0		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 13A
Diode Forward Voltage	V <sub>SD</sub>	—	0.7	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1A
<b>DYNAMIC CHARACTERISTICS (Note 10)</b>						
Input Capacitance	C <sub>iss</sub>	—	2,060	—	pF	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	547	—		
Reverse Transfer Capacitance	C <sub>rss</sub>	—	517	—		
Gate Resistance	R <sub>G</sub>	—	1.6	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Q <sub>g</sub>	—	24.8	—	nC	V <sub>DD</sub> = 10V, I <sub>D</sub> = 5A
Total Gate Charge (V <sub>GS</sub> = 10V)	Q <sub>g</sub>	—	46.7	—		
Gate-Source Charge	Q <sub>gs</sub>	—	3	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	9.6	—		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	3.7	—	ns	V <sub>DD</sub> = 10V, V <sub>GS</sub> = 10V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = 5A
Turn-On Rise Time	t <sub>R</sub>	—	7.2	—		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	37.5	—		
Turn-Off Fall Time	t <sub>F</sub>	—	23.3	—		
Reverse Recovery Time	t <sub>RR</sub>	—	19.9	—	ns	I <sub>F</sub> = 5A, di/dt = 100A/µs
Reverse Recovery Charge	Q <sub>RR</sub>	—	9.0	—	nC	

- Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
  6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
  7. Thermal resistance from junction to soldering point (on the exposed drain pad).
  8. I<sub>AS</sub> and E<sub>AS</sub> ratings are based on low frequency and duty cycles to keep T<sub>J</sub> = +25°C.
  9. Short duration pulse test used to minimize self-heating effect.
  10. Guaranteed by design. Not subject to product testing.



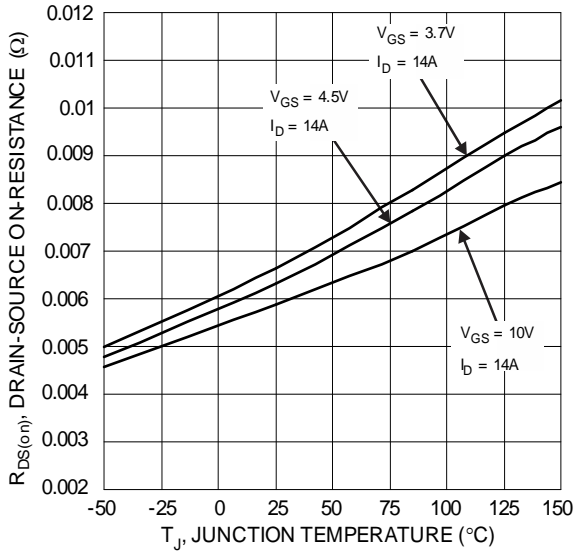


Figure 7 On-Resistance Variation with Junction Temperature

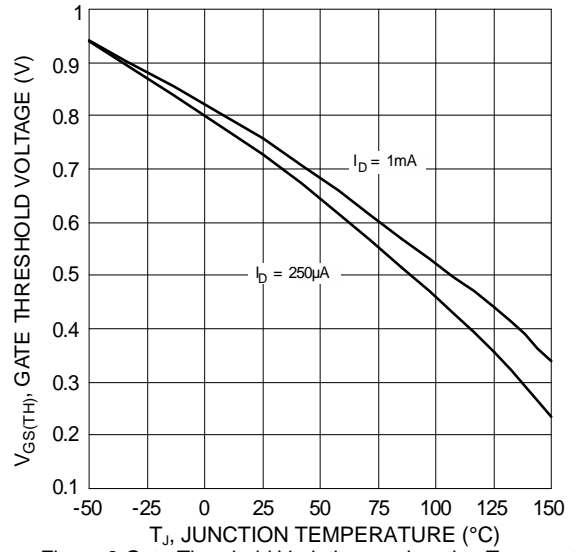


Figure 8 Gate Threshold Variation vs. Junction Temperature

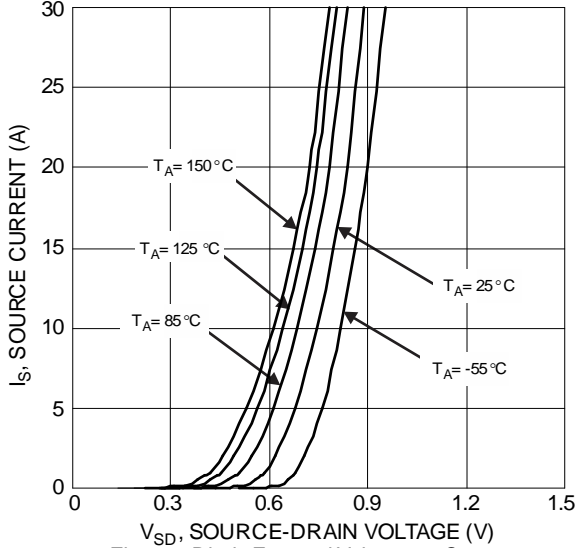


Figure 9 Diode Forward Voltage vs. Current

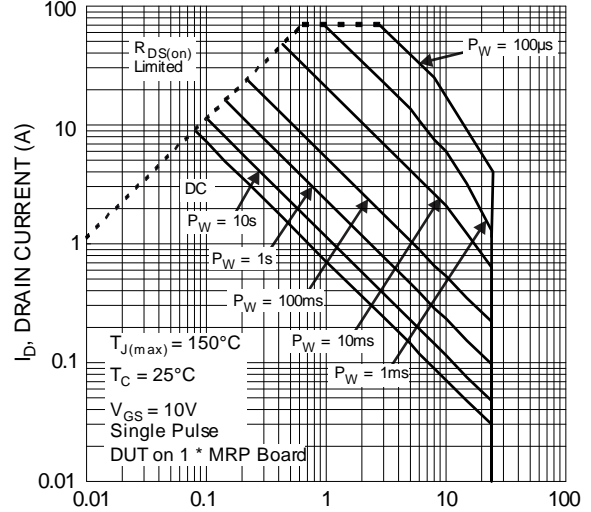


Figure 10 SOA, Safe Operation Area

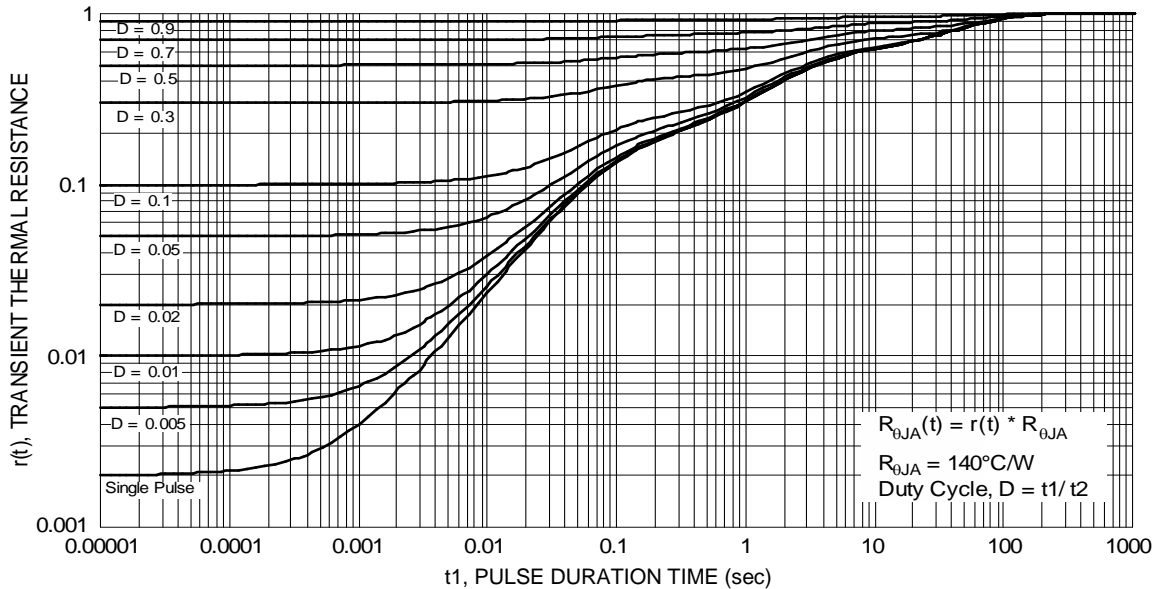
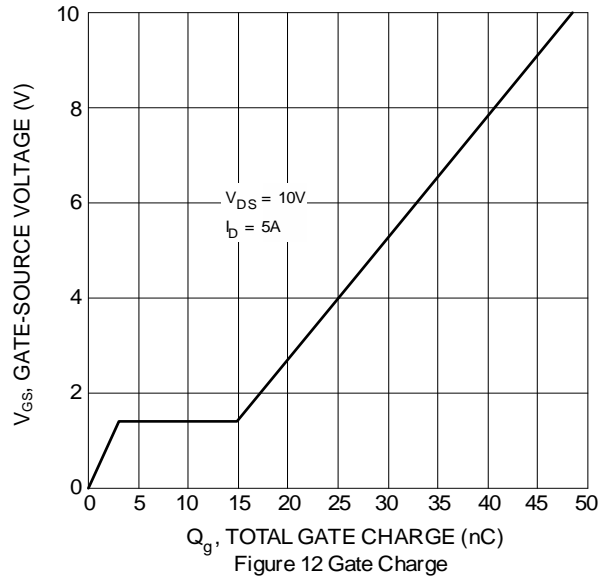


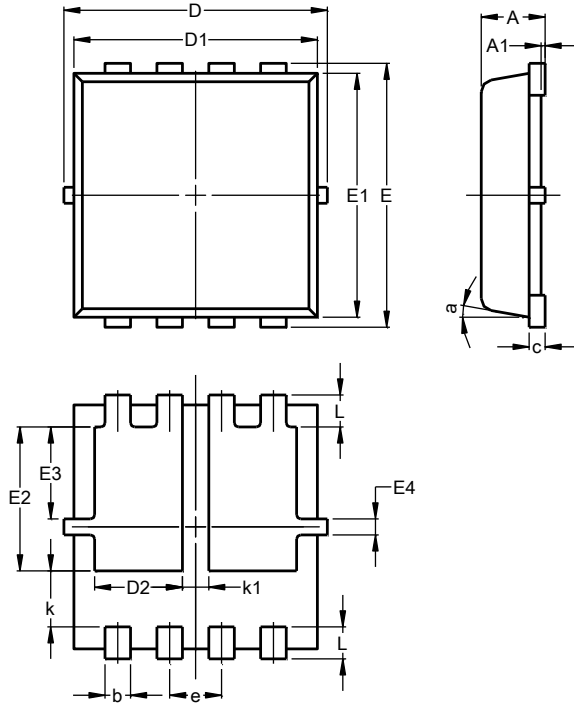
Figure 11. Transient Thermal Resistance



**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**PowerDI3333-8 (Type UXC)**

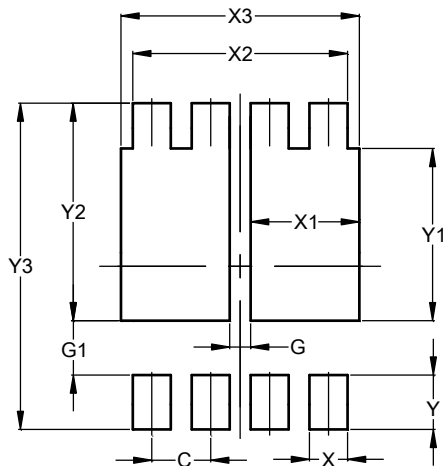


PowerDI3333-8 (Type UXC)			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	--
b	0.25	0.40	0.32
c	0.10	0.25	0.15
D	3.20	3.40	3.30
D1	2.95	3.15	3.05
D2	0.90	1.30	1.10
E	3.20	3.40	3.30
E1	2.95	3.15	3.05
E2	1.60	2.00	1.80
E3	0.95	1.35	1.15
E4	0.10	0.30	0.20
e	--	--	0.65
L	0.30	0.50	0.40
k	0.50	0.90	0.70
k1	0.13	0.53	0.33
a	0°	12°	10°
<b>All Dimensions in mm</b>			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**PowerDI3333-8 (Type UXC)**



Dimensions	Value (in mm)
C	0.650
G	0.230
G1	0.600
X	0.420
X1	1.200
X2	2.370
X3	2.630
Y	0.600
Y1	1.900
Y2	2.400
Y3	3.600

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