

PI6C48545

3.3V Low Skew 1-to-4 LVTTTL/LVCMOS to LVDS Fanout Buffer

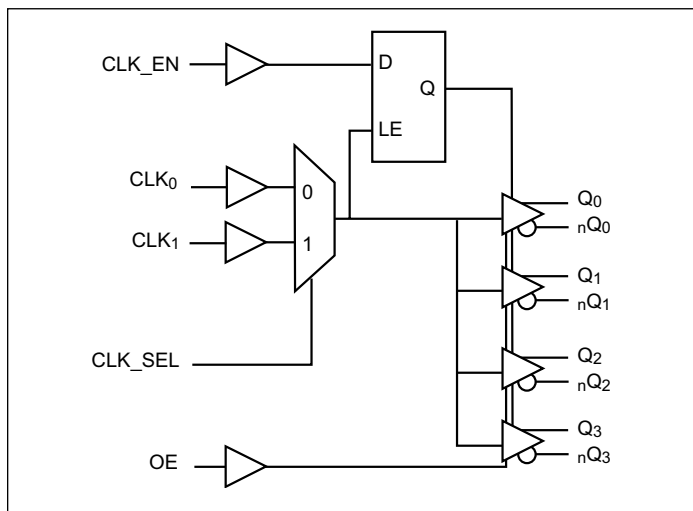
Features

- Maximum operation frequency: 650 MHz
- 4 pair of differential LVDS outputs
- Selectable CLK₀ and CLK₁ inputs
- CLK₀, CLK₁ accept LVCMOS, LVTTTL input level
- Output Skew: 40ps (maximum)
- Part-to-part skew: 300ps (maximum)
- Propagation delay: 2.2ns (maximum)
- 3.3V power supply
- Pin-to-pin compatible to ICS8545
- Operating Temperature: -40°C to 85°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.
- Packaging (Pb-free & Green):
- 20-pin TSSOP (L)

Description

The PI6C48545 is a high-performance low-skew LVDS fanout buffer. PI6C48545 features two selectable single-ended clock inputs and translate to four LVDS outputs. The CLK₀ and CLK₁ inputs accept LVCMOS or LVTTTL signals. The outputs are synchronized with input clock during asynchronous assertion/deassertion of CLK_EN pin. PI6C48545 is ideal for single-ended LVTTTL/LVCMOS to LVDS translations. Typical clock translation and distribution applications are data-communications and telecommunications.

Block Diagram



Control Input Function Table

Inputs				Outputs	
OE	CLK_EN	CLK_SEL	Selected Source	Q ₀ :Q ₃	nQ ₀ :nQ ₃
1	0	0	CLK ₀	Disabled: Low	Disabled: High
1	0	1	CLK ₁	Disabled: Low	Disabled: High
1	1	0	CLK ₀	Enabled	Enabled
1	1	1	CLK ₁	Enabled	Enabled
0	x	x		HiZ	HiZ

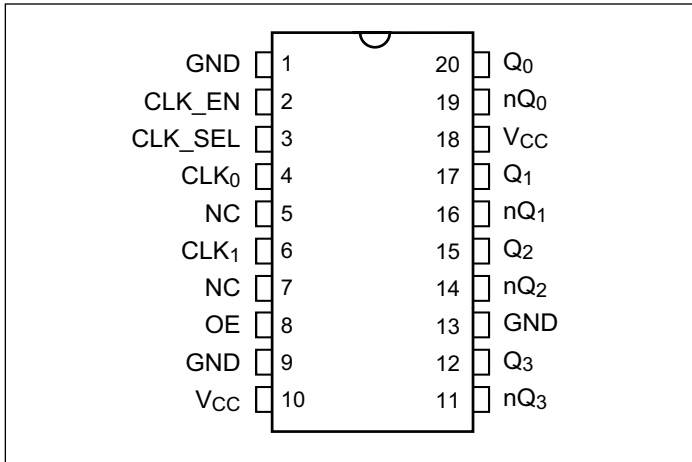
Notes:

1. After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show below.

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, “Green” and Lead-free.
3. Halogen- and Antimony-free “Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Name	Pin #	Type	Description
GND	1, 9, 13	P	Connect to Ground
CLK_EN	2	I_PU	Synchronizing clock enable. When high, clock outputs follow clock input. When low, Qx outputs are forced low, nQx outputs are forced high. LVCMOS/LVTTL level with 80kΩ pull up.
CLK_SEL	3	I_PD	Clock select input. When high, selects CLK ₁ input. When low, selects CLK ₀ input. LVCMOS/LVTTL level with 80kΩ pull down.
CLK ₀	4	I_PD	LVCMOS / LVTTL clock input
CLK ₁	6	I_PD	LVCMOS / LVTTL clock input
NC	5, 7		No internal connection.
OE	8	I_PU	Output Enable. Controls outputs Q ₀ , nQ ₀ through Q ₃ , nQ ₃ .
VCC	10, 18	P	Connect to 3.3V.
Q ₃ , nQ ₃	12, 11	O	Differential output pair, LVDS interface level.
Q ₂ , nQ ₂	15, 14	O	Differential output pair, LVDS interface level.
Q ₁ , nQ ₁	17, 16	O	Differential output pair, LVDS interface level.
Q ₀ , nQ ₀	20, 19	O	Differential output pair, LVDS interface level.

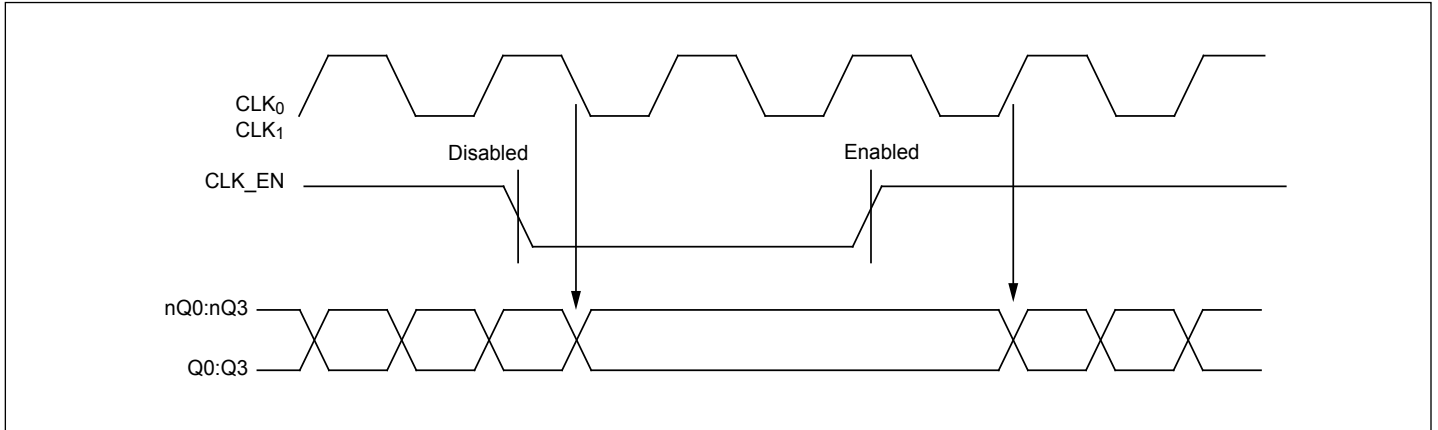
Notes:

1. I = Input, O = Output, P = Power supply connection, I_PD = Input with pull down, I_PU = Input with pull up.

Pin Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C _{IN}	Input Capacitance			6		pF
R _{pullup}	Input Pullup Resistance			80		kΩ
R _{pulldown}	Input Pulldown Resistance			80		

CLK_EN Timing Diagram



Clock Input Function Table

Inputs	Outputs	
CLK ₀ or CLK ₁	Q ₀ :Q ₃	nQ ₀ :nQ ₃
0	LOW	HIGH
1	HIGH	LOW

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature	-55 to +150°C
Supply Voltage to Ground Potential (V_{DD} , V_{DDO})	-0.5 to +4.6V
Inputs (Referenced to GND).....	-0.5 to $V_{DD}+0.5V$
Clock Output (Referenced to GND)	-0.5 to $V_{DD}+0.5V$
Latch up	200mA
ESD Protection (Input)	2000V min (HBM)
Junction Temperature	150°C max

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Temperature		-40		85	°C
I_{CC}	Power Supply Current				60	mA

LVC MOS/LVTTL DC Characteristics ($T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 3.135\text{V}$ to 3.465V unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	CLK ₀ , CLK ₁ , CLK_EN, CLK_SE, OE	2		$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	CLK ₀ , CLK ₁	-0.3		1.3	V
		CLK_EN, CLK_SEL, OE	-0.3		0.8	V
I_{IH}	Input High Current	CLK ₀ , CLK ₁ , CLK_SEL	$V_{IN} = V_{CC} = 3.465\text{V}$		150	uA
		CLK_EN, OE	$V_{IN} = V_{CC} = 3.465\text{V}$		5	uA
I_{IL}	Input Low Current	CLK ₀ , CLK ₁ , CLK_SEL	$V_{IN} = 0\text{V}$, $V_{CC} = 3.465\text{V}$	-5		uA
		CLK_EN, OE	$V_{IN} = 0\text{V}$, $V_{CC} = 3.465\text{V}$	-150		uA

LVDS DC Characteristics ($T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 3.135\text{V}$ to 3.465V unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage		200	280	360	mV
ΔV_{OD}	V_{OD} Magnitude Change			0	40	
V_{OS}	Offset Voltage		1.125	1.3	1.475	V
ΔV_{OS}	V_{OS} Magnitude Change			5	25	mV
I_{OZ}	High Impedance Leakage Current		-10		+10	uA
I_{OFF}	Power OFF Leakage		-20	±1	+20	
I_{OSD}	Differential Output Short Circuit Current			-3.5	-5	mA
I_{OS}	Output Short Circuit Current			-3.5	-5	
V_{OH}	Output Voltage High			1.34	1.6	V
V_{OL}	Output Voltage Low		0.9	1.06		

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AC Characteristics ($T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 3.135\text{V}$ to 3.465V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{\max}	Output Frequency				650	MHz
t_{Pd}	Propagation Delay ⁽¹⁾		0.8		2.2	ns
$T_{sk(o)}$	Output-to-output Skew ⁽²⁾				40	ps
$T_{sk(pp)}$	Part-to-part Skew ⁽³⁾				300	
t_r/t_f	Output Rise/Fall time	20% - 80%	100		300	
odc	Output duty cycle		48		52	%

Notes:

1. Measured from the $V_{CC}/2$ of the input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
3. Defined as skew between outputs on different parts operating at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
4. All parameters are measured at 500MHz unless noted otherwise

Part Marking

<p>PI6C 48545LE CYYWWXX</p> <p>○</p>
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C: Die Rev

YY: Year

WW: Workweek

1st X: Assembly Code

2nd X: Fab Code

PI6C48545

Packaging Mechanical: 20-TSSOP (L)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
C	0.09	—	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	—	—
θ	0°	—	8°

NOTES:
 1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
 2. JEDEC MO-153F
 3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

		DATE: 03/31/16
DESCRIPTION: 20-Pin, 173mil Wide TSSOP		
PACKAGE CODE: L (L20)		
DOCUMENT CONTROL #: PD-1311	REVISION: G	

16-0074

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Ordering Code	Package Code	Package Description
PI6C48545LEX	L	20-pin, 173-mil Wide (TSSOP)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
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3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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