

P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

V _{(BR)DSS}	R _{DS(on) max}	I _D T _A = +25°C
2017	$16m\Omega$ @ $V_{GS} = -20V$	-7.3A
-30V	20mΩ @ V _{GS} = -10V	-6.0A

Description

This new generation MOSFET has been designed to minimize the onstate resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- DC-DC Converters
- Power management functions
- Backlighting

Features

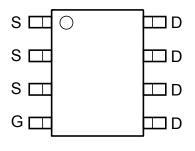
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

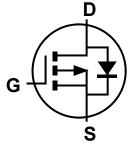
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 @3
- Weight: 0.074 grams (approximate)







Top View Internal Schematic



Equivalent circuit

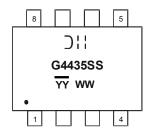
Ordering Information (Note 4)

Part Number	Case	Packaging
DMG4435SSS-13	SO-8	2500 / Tape & Reel

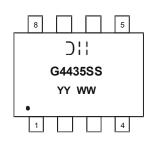
Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

⊃¦¦ = Manufacturer's Marking G4435SS = Product Type Marking Code YYWW = Date Code Marking YY or \overline{YY} = Year (ex: 13 = 2013) WW = Week (01 - 53)

YY = Date Code Marking for SAT (Shanghai Assembly/ Test site) YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage	V_{GSS}	±25	V		
Continuous Davis Compant (Nata 5) V	Steady State	T _A = +25°C T _A = +70°C	I _D	-7.3 -5.7	Α
Continuous Drain Current (Note 5) V_{GS} = -20 $t < 10s$ $T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$		• •	I _D	-10 -7.5	Α
Pulsed Drain Current (Note 6)			I _{DM}	-80	Α

Thermal Characteristics

Characteristic	Symbol	Value	Unit	
Power Dissipation (Note 5)	$T_A = +25$ °C	0	2.5	W
Fower Dissipation (Note 5)	T _A = +70°C	P_D	1.5	W
Thermal Desigtance, Junction to Ambient &T. = 125°C	Steady state	Б	96.5	°C/W
Thermal Resistance, Junction to Ambient @T _A = +25°C	t < 10s	$R_{\theta JA}$	55	°C/W
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	-30	_	_	V	$V_{GS} = 0V$, $I_D = -1mA$	
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	_	_	-1.0	μA	V _{DS} = -30V, V _{GS} = 0V	
Gate-Source Leakage	I _{GSS}	_	-	±100	nA	V _{GS} = ±25V, V _{DS} = 0V	
ON CHARACTERISTICS (Note 7)				•			
Gate Threshold Voltage	V _{GS(th)}	-1.0	-1.7	-2.5	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
			13	16		$V_{GS} = -20V, I_D = -11A$	
Static Drain-Source On-Resistance	R _{DS (ON)}	_	15	20	mΩ	V _{GS} = -10V, I _D = -10A	
			21	29		V _{GS} = -5V, I _D = -5A	
Forward Transfer Admittance	Y _{fs}	_	22	_	S	V _{DS} = -5V, I _D = -10A	
Diode Forward Voltage	V_{SD}	_	-0.74	-1.0	V	V _{GS} = 0V, I _S = -1A	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C _{iss}	_	1614	_	pF		
Output Capacitance	Coss	_	226	_	pF	$V_{DS} = -15V, V_{GS} = 0V,$ f = 1.0MHz	
Reverse Transfer Capacitance	Crss	_	214	_	pF	1 - 1.0ivii iz	
Gate Resistance	Rg	_	6.8	_	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz	
Total Gate Charge at 10V	Qg	_	35.4	_	nC	V _{GS} = -10V, V _{DS} = -15V, I _D = -10A	
Total Gate Charge at 5V	Qg	_	18.9	_	nC		
Gate-Source Charge	Q _{gs}	_	4.6	_	nC	$V_{GS} = -5V, V_{DS} = -15V,$ $I_{D} = -10A$	
Gate-Drain Charge	Q _{gd}	_	5.7	_	nC		
Turn-On Delay Time	t _{D(on)}	_	8.6	_	ns		
Turn-On Rise Time	t _r	_	12.7	_	ns	V _{DS} = -15V, V _{GS} = -10V,	
Turn-Off Delay Time	t _{D(off)}	_	44.9	_	ns	$R_L = 1.5\Omega$, $R_{GEN} = 3\Omega$,	
Turn-Off Fall Time	t _f	_	22.8	_	ns	1	

Notes: 5. Device mounted on 1in. x 1in. FR-4 PCB with 2oz. Copper, and the testing is based on the t<10s. The value in any given application depends on the user's specific board design.

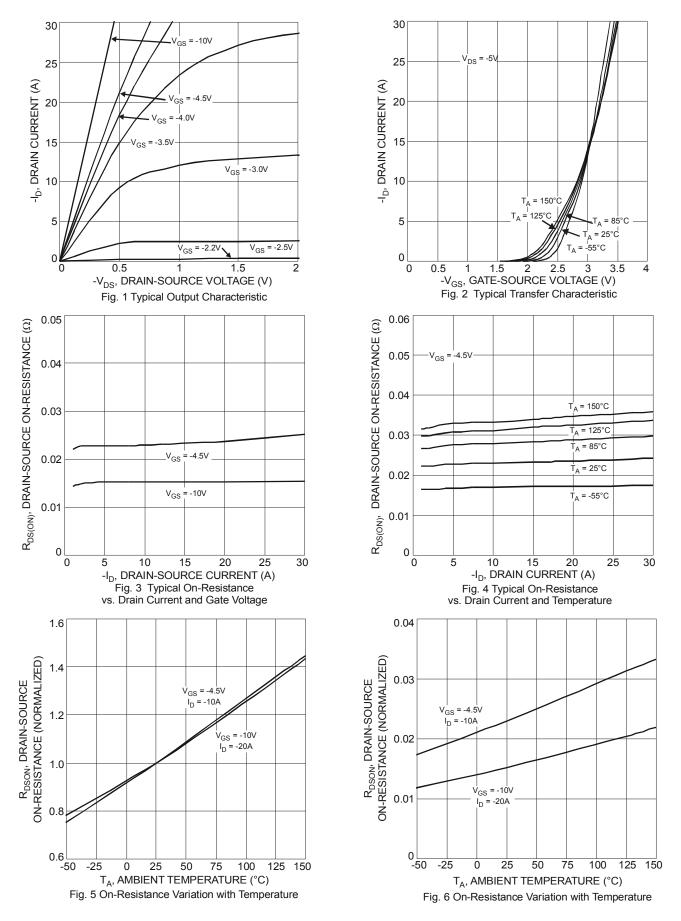
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^{6.} Repetitive rating, pulse width limited by junction temperature.

^{7.} Short duration pulse test used to minimize self-heating effect.

^{8.} Guaranteed by design. Not subject to production testing.







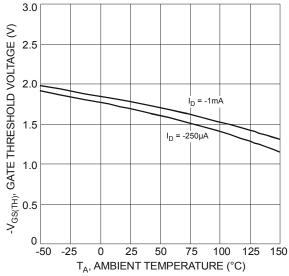
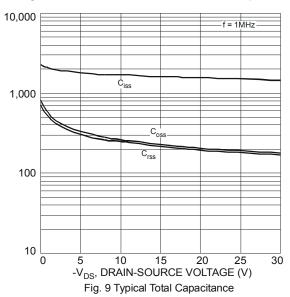


Fig. 7 Gate Threshold Variation vs. Ambient Temperature



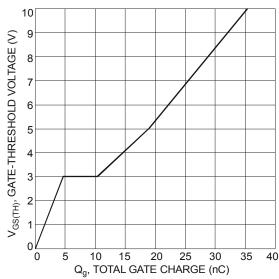
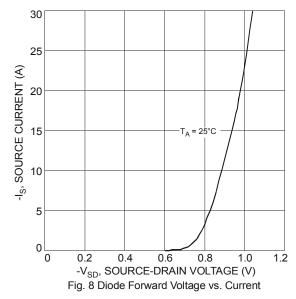


Fig. 11 Gate Threshold Voltage vs. Total Gate Charge



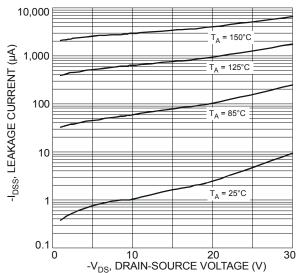
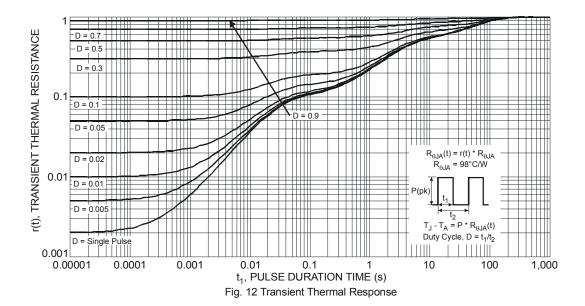


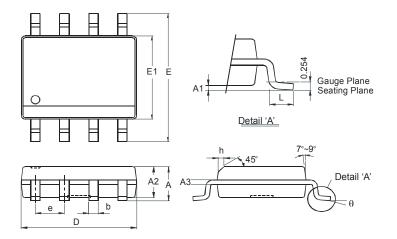
Fig. 10 Typical Leakage Current vs. Drain-Source Voltage





Package Outline Dimensions

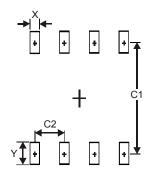
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SO-8				
Dim	Min	Max		
Α	-	1.75		
A1	0.10	0.20		
A2	1.30	1.50		
A3	0.15	0.25		
b	0.3	0.5		
D	4.85	4.95		
Е	5.90	6.10		
E1	3.85	3.95		
е	1.27 Typ			
h	-	0.35		
L	0.62	0.82		
θ	0°	8°		
All Dimensions in mm				

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Х	0.60
Υ	1.55
C1	5.4
C2	1.27



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