

**3.3V, 1-port, SATA Gen 3i ReDriver™ with Adjustable Equalization/Pre-Emphasis**

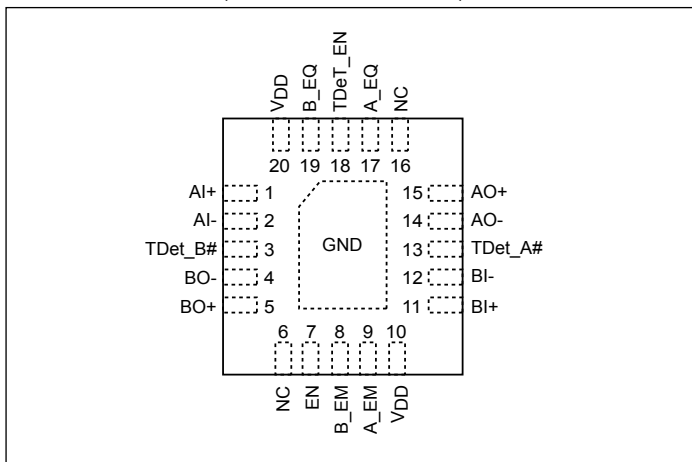
**Features**

- Supports SATA Gen 3i.
- Two 6Gbps differential signal pairs
- 100Ω Differential CML I/O's
- Input signal level detect and squelch for each channel
- OOB Support
- Automatic HDD Rate detection for output swing/emphasis setting
- Termination detect indication
  - Power saving mode control to Host or HDD
- Adjustable Receiver Equalization
- Selectable Output Pre-emphasis and Swing Control
- High impedance I/O termination in standby mode
- ESD +/-8kV
- Low Power Operation: 254mW typical
- Auto-Slumber Mode: 36mW typical
- HDD unplugged: 3.6mW
- Power down Stand-by Mode: 0.7mW max
- Supply Voltage: 3.3V ±10%
- Industrial Temperature Range: -40°C to 85°C
- Packaging: 20-TQFN (4x4mm)

**Applications**

- Notebook, desktop, docking station, Set Top Box, Server Workstation, Data Storage

**Pin Diagram (Top Side View)**



**Description**

The PI3EQX6741ST is a low power, signal SATA Gen 3i 6Gbps ReDriver™. The device provides programmable equalization and output emphasis, to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI3EQX6741ST supports two 100Ω Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

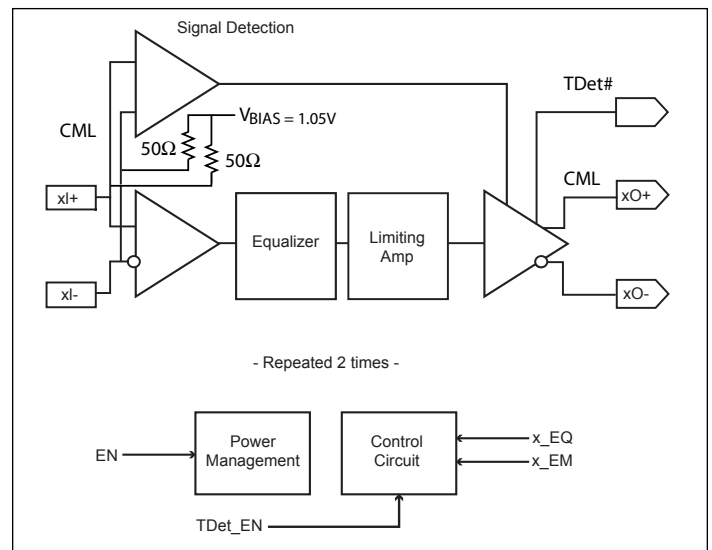
The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver.

A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independently. When the channels are enabled (EN=1) and operating, that channel's input signal level (on xI+/-) determines whether the output is active. If the input signal level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage.

Termination Detect indication (TDet\_A# or TDet\_B#) provides indication when the load is connected i.e. HDD or Host. This can be used as control to go into power saving mode by either the host or HDD.

In addition to signal conditioning, when EN = 0, the device enters a low power standby mode.

**Block Diagram**



## Pin Description

Standard Mode Pin #	Pin Name	Type	Description
9	A_EM	Input	Output emphasis adjustment for channel A. (See Configuration Table) Digital control with 200K $\Omega$ pull-up resistor.
17	A_EQ	Input	Channel A Equalization adjustment is active. (See Configuration Table) Tri-level input pin with 100K $\Omega$ pull-up and 100K $\Omega$ pull-down resistors.
1 2	AI+ AI-	Input	CML input forward channel A with internal 50 $\Omega$ pull-up resistors connected to VBIAS (100 $\Omega$ differential).
15 14	AO+ AO-	Output	CML output channel A with internal 50 $\Omega$ pull-up resistors connected to VBIAS (100 $\Omega$ differential).
8	B_EM	Input	Output emphasis adjustment for channel B. (See Configuration Table) Digital control with 200K $\Omega$ pull-up resistor.
19	B_EQ	Input	Tri-level input pin with 100K $\Omega$ pull-up and 100K $\Omega$ pull-down resistors. (See Configuration Table)
11 12	BI+ BI-	Input	CML input return channel B with internal 50K $\Omega$ pull-up, resistor connected to VBIAS (100 $\Omega$ differential).
5 4	BO+ BO-	Output	Positive CML output channel B with internal 50 $\Omega$ pull-up resistor connected to VBIAS (100 $\Omega$ differential).
7	EN	Input	Chip Enable "High" provides normal operation. "Low" for power down mode. With internal 200K $\Omega$ pull-up resistor.
Center Pad	GND	GND	Supply ground.
10, 20	VDD	Power	3.3V supply voltage $\pm$ 10%
3	TDet_B#	Output	Termination detect output for channel B-Active Low, open drain. Low: HDD Termination present. High: HDD Termination NOT present.
13	TDet_A#	Output	Termination detect output for channel A-Active Low, open drain. Low: HDD Termination present. High: HDD Termination NOT present.
18	TDet_EN	Input	Termination Detect Enable (200K $\Omega$ internal pull-up resistor) High: Enable Termination Detect for eSATA application or hot plug Device application Low: Disable Termination Detect for internal SATA application.
6, 16	NC		No Connection internally.

### Configuration Table - Output Pre-emphasis/Swing Setting

A_EM/B_EM	3 Gb/s	6 Gb/s
0	550mV pp	650mV pp
1	550mV pp + 3dB Pre-emphasis	650mV pp + 1.5dB Pre-emphasis

### Configuration Table - Input Equalizer

A_EQ/B_EQ	1.5 Gb/s	3 Gb/s	6Gb/s
0	1 dB	2.5 dB	3 dB
floating	2.5 dB	5 dB	6 dB
1	4 dB	7.5 dB	9 dB

### Termination Detect Feature:

Termination Detect is a power saving feature. The user can enable TDet\_EN (set to High) for eSATA application as it would save more power when there is no external HDD connection. But for internal SATA application, TDet\_EN should be set to LOW because internal HDD is always on and termination is always there.

When Redriver doesn't detect Host or HDD termination, there will be about 12us detect pulse width with 50us detect period at the output of ReDriver. Once the termination is detected, the detect period will change to about 40ms. Anyway when the signal is detected at the input of redriver, there will not be any detect pulse at both the output side of redriver.

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	-65°C to +150°C
Supply Voltage to Ground Potential.....	-0.5V to +4.6V
DC SIG Voltage .....	-0.5V to V <sub>DD</sub> +0.5V
Output Current .....	-25mA to +25mA
Power Dissipation Continuous .....	500mW
Operating Temperature .....	-40°C to +85°C
ESD, Human Body Model .....	-8kV to 8kV

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## AC/DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Units
V <sub>DD</sub>	Power Supply Voltage		3.0		3.6	V
P <sub>STANDBY</sub>	Supply Power, Standby	EN = 0		0.07	0.7	mW
P <sub>UNPLUG</sub>	Supply Power, HDD unplugged	No HDD attached, TDet_EN = High		3.6	11	
P <sub>SLUMBER</sub>	Supply Power, Slumber	TDet_EN = Low		36	50	
P <sub>ACTIVE</sub>	Supply Power, Active	EN = 1 A/B_EM=0 DIFFP-P ≥ V <sub>TH</sub> -SD		254	317	
I <sub>DD</sub> -STANDBY	Supply Current Standby	EN = 0		0.02	0.2	mA
I <sub>DD</sub> -UNPLUG	Supply Current, HDD unplugged	No HDD attached, TDet_EN = High		1	3	
I <sub>DD</sub> -SLUMBER	Supply Current Slumber	TDet_EN = Low		11	14	
I <sub>DD</sub> -ACTIVE	Supply Current Active	EN = 1, input = 600mVppd, A/B_EM=0		77	88	
t <sub>PD</sub>	Latency	From input to output		0.7		ns

### CML Receiver Input

Z <sub>RX</sub> -DC	DC Input Impedance		40	50	60	Ohm
Z <sub>RX</sub> -DIFF-DC	DC Differential Input Impedance		80	100	120	
V <sub>RX</sub> -DIFFp-p	Differential Input Peak-to-peak Voltage		0.2		1.2	V
V <sub>RX</sub> -CM-ACP	AC Peak Common Mode Input Voltage				150	mV
V <sub>TH</sub> -SD	Signal detect Threshold	EN = 1	50		200 <sup>(2)</sup>	mVppd

Note:

1. Typical values are at V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 25°C ambient and maximum loading.
2. Using Compliance test at 1.5Gbps, 3Gbps and 6Gbps. Also using OOB (OOB is formed by ALIGNp primitive or D24.3) test patterns at 1.5Gbps. The ALIGN primitive (K28.5+D10.2+D27.3 = 0011111010+0101010101+0010011100). The D24.3 = 00110011001100110011.

**AC/DC Electrical Characteristics (CML Receiver Input continued)**

Symbol	Parameter	Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Units
RL <sub>dd11_RX</sub>	RX differential mode return loss	75MHz-300MHz 300MHz-600MHz 600MHz-1.2GHz 1.2GHz-2.4GHz 2.4GHz-3.0GHz 3.0 GHz-5.0GHz	18 14 10 8 3 1			dB
RL <sub>cc11_RX</sub>	RX common mode return loss	150MHz – 300MHz 300MHz – 600MHz 600MHz – 1.2GHz 1.2GHz – 2.4GHz 2.4GHz – 3.0GHz 3.0GHz – 5.0GHz	3 5 2 2 1 1			dB
RL <sub>dc11_RX</sub>	RX impedance balance	150MHz – 300MHz 300MHz – 600MHz 600MHz – 1.2GHz 1.2GHz – 2.4GHz 2.4GHz – 3.0GHz 3.0GHz – 5.0GHz	30 30 20 10 4 4			dB

**CML Transmitter Output (100Ω differential)<sup>(3)</sup>**

Z <sub>TX-DIFF-DC</sub>	DC Differential TX Impedance		80	100	120	Ohm
V <sub>TX-DIFFp-p</sub>	Differential Peak-to-peak Output Voltage	V <sub>TX-DIFFp-p</sub> = 2 *  V <sub>TX-D</sub>				
		SATA2	450		700	
		SATA3	550		750	mV
V <sub>TX-C</sub>	Common-Mode Voltage	V <sub>TX-D+</sub> + V <sub>TX-D-</sub>  /2	0.5		1.2	V
t <sub>F</sub> , t <sub>R</sub>	Transition Time	20% to 80% <sup>(3)</sup> 0dB Pre-emphasis	40		150	ps
V <sub>amp_bal</sub>	TX amplitude imbalance	3G only; HFTP, MFTP			10	%
T <sub>skew</sub>	TX differential skew	1.5G and 3G; HFTP, MFTP			20	ps
V <sub>cm_ac</sub>	TX AC common mode voltage	3G only; MFTP			50	mVpp
V <sub>TX-Pre-Ratio-max</sub>	Max TX Pre-emphasis Level			3 1.5		dB
RL <sub>dd11_TX</sub>	TX differential mode return loss	150MHz – 300MHz 300MHz – 600MHz 600MHz – 1.2GHz 1.2GHz – 2.4GHz 2.4GHz – 3.0GHz 3.0 GHz – 5.0GHz	14 8 6 6 3 1			dB
C <sub>TX</sub>	AC Coupling Capacitor		2	4.7	12	nF
T <sub>J</sub>	Total Jitter	FR4 Input Trace	18" 36"		0.16 0.24	UI
D <sub>J</sub>	Deterministic Jitter	FR4 Input Trace	18" 36"		0.11 0.19	UI

**Note:**

3. Recommended output coupling capacitor is 4.7nF to 12nF (on each output)

### AC/DC Electrical Characteristics

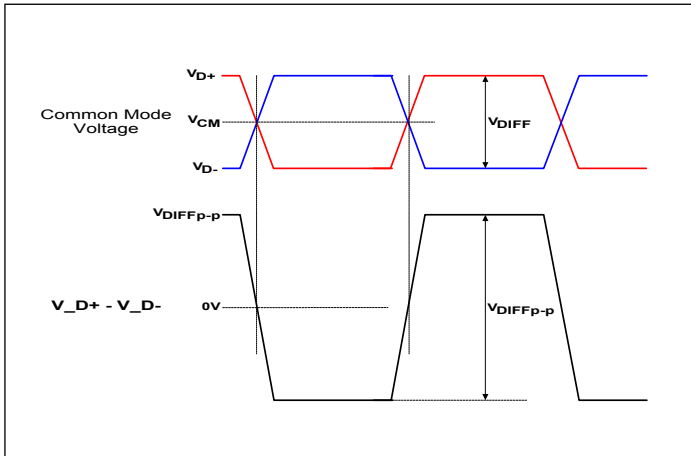
Symbol	Parameter	Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Units
RL <sub>cc11_TX</sub>	TX common mode return loss	150MHz – 300MHz	5			dB
		300MHz – 600MHz	5			
		600MHz – 1.2GHz	2			
		1.2GHz – 2.4GHz	2			
		2.4GHz – 3.0GHz	1			
		3.0 GHz – 5.0GHz	1			
RL <sub>dc11_TX</sub>	TX impedance balance	150MHz – 300MHz	30			dB
		300MHz – 600MHz	20			
		600MHz – 1.2GHz	10			
		1.2GHz – 2.4GHz	10			
		2.4GHz – 3.0GHz	4			
		3.0 GHz – 5.0GHz	4			

### LVC MOS Control Pins

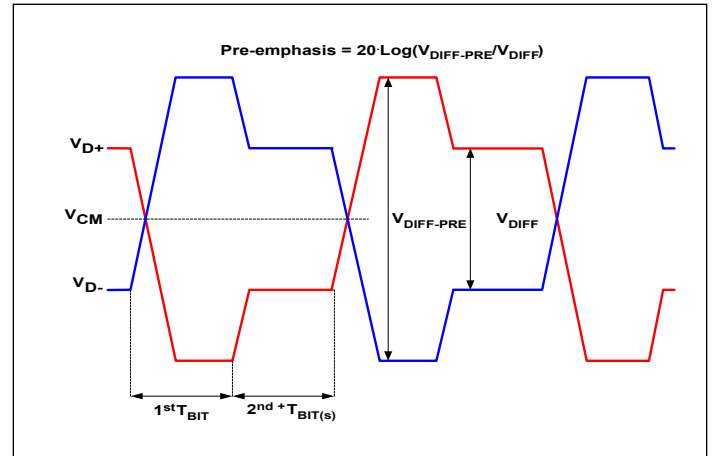
V <sub>IH</sub>	Input High Voltage (Bi-Level)		0.65 × V <sub>DD</sub>			V
V <sub>IL</sub>	Input Low Voltage (Bi-Level)				0.35 × V <sub>DD</sub>	
I <sub>IH</sub>	Input High Current				100	μA
I <sub>IL</sub>	Input Low Current		-100			
V <sub>OL</sub>	DC Output Logic Low	I <sub>OL</sub> = 4 mA			0.4	V
V <sub>IH</sub>	Input High Voltage (Tri-Level)		0.8 × V <sub>DD</sub>			V
V <sub>IL</sub>	Input Low Voltage (Tri-Level)				0.2 × V <sub>DD</sub>	V

### Auto Slumber Mode Entry/Exit Time

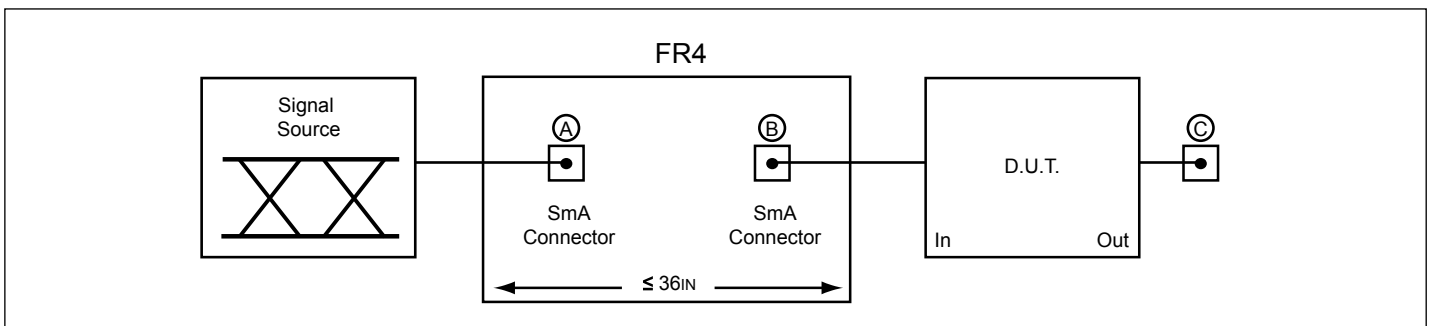
Symbol	Parameter	Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Units
T <sub>SlumberON</sub>	Entry time to Slumber Mode	Electrical Idle at Input (See Figure)		10	20	μS
T <sub>SlumberOFF</sub>	Exit time from Slumber Mode	After first signal activity (See Figure)		6	20	ns



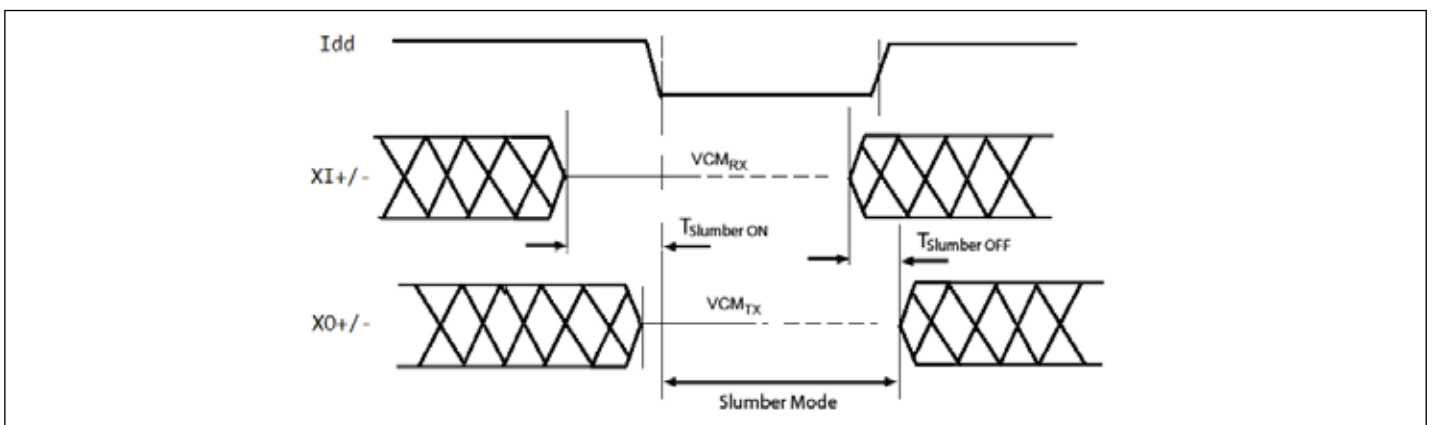
**Definition of Differential Voltage and Differential Voltage Peak-to-Peak**



**Definition of Pre-emphasis**

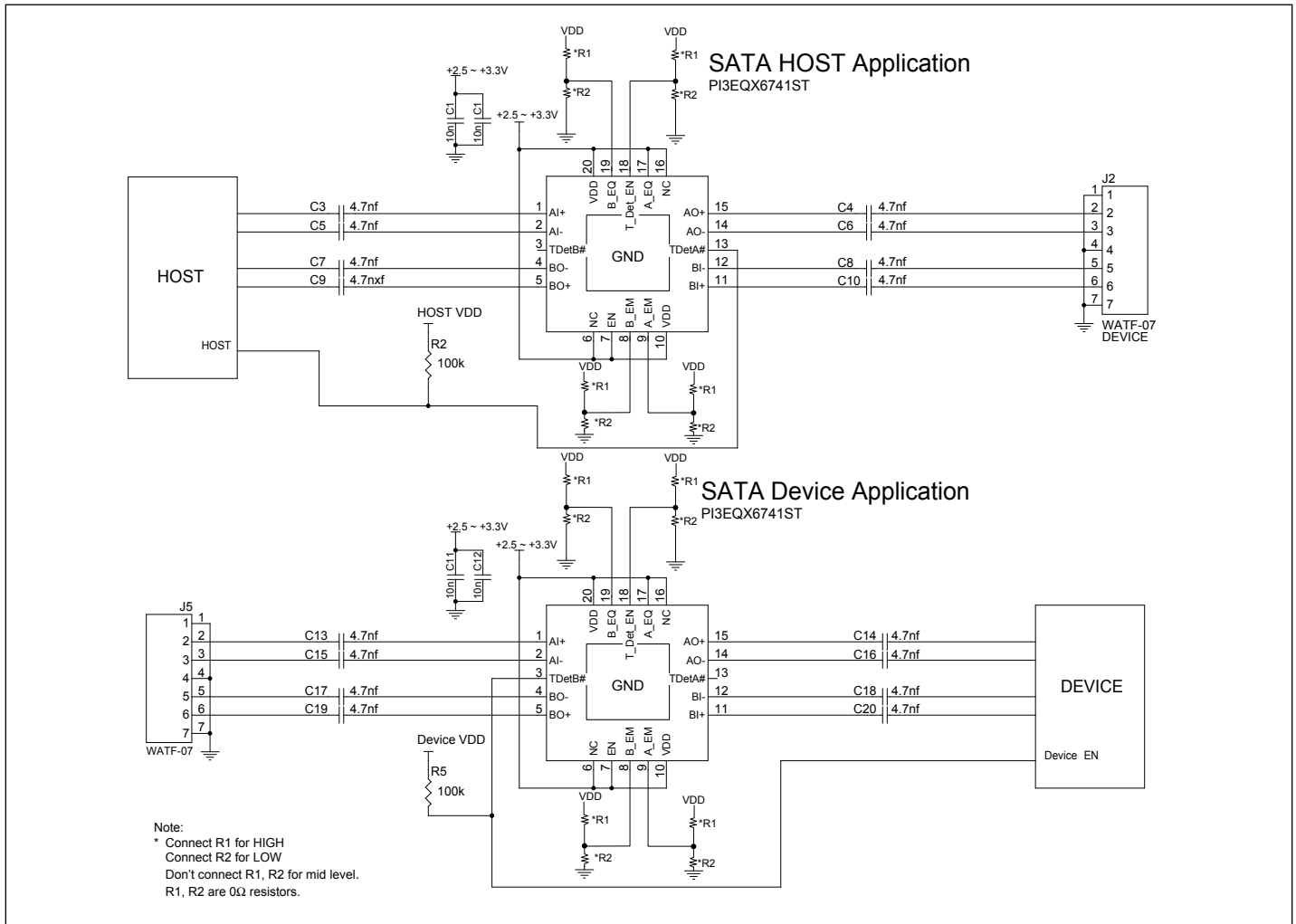


**Test Condition Referenced in the Electrical Characteristic Table**



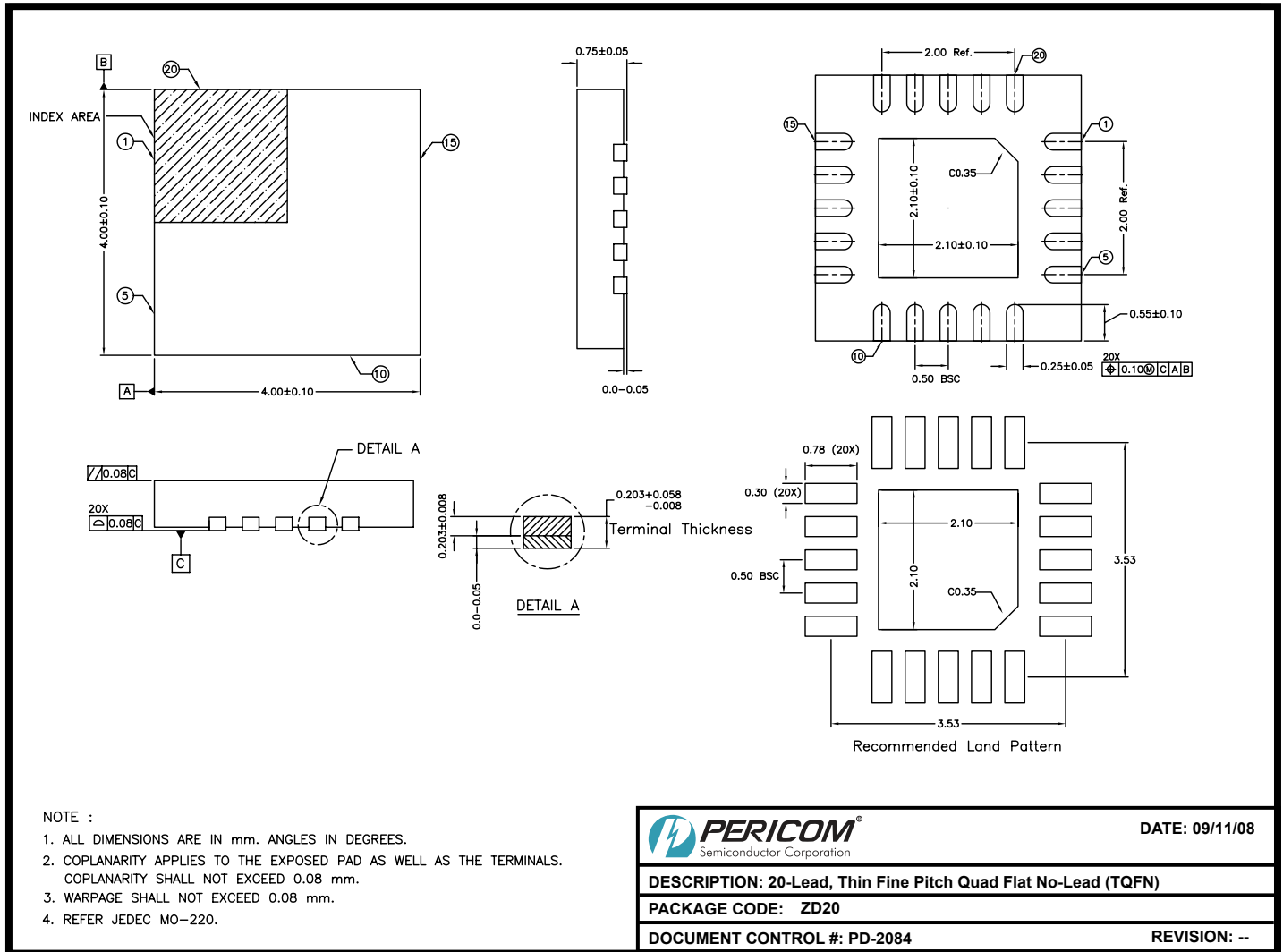
**Auto Slumber Mode Entry and Exit Timing**

**Application Schematic**





**Packaging Mechanical: 20-contact TQFN (ZD)**



08-0456

Note: For latest package info, please check: <http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/>

**Ordering Information**

Ordering Number	Package Code	Package Description
PI3EQX6741STZDE	ZD	20-Lead, Thin Fine Pitch Quad Flat No-Lead (TQFN)
PI3EQX6741STZDEX	ZD	20-Lead, Thin Fine Pitch Quad Flat No-Lead (TQFN), Tape & Reel

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- E = Pb-free and Green
- X suffix = Tape/Reel

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