PI3EQX1204-C

12.5Gbps 4-Channel, SAS3, 10GbE ReDriver with Linear Equalization

Features

- 1-to-12.5Gbps serial link with linear equalizer
- Supports SATA Gen1/Gen2/Gen3, SAS2/3, 10GbE, and XAUI protocol
- Supports 4 differential channels
- Handles up to 34dB channel loss (42" FR4 trace, 10 meters, or SAS3 cable)
- Independent channel configuration of receiver equalization, output swing and flat gain
- Rate and coding agnostic
- Transparent to link training, OOB, Idle
- 260mW per channel power dissipation with 700 mVpp output swing
- Pin strap and I^2C selectable device programming
- 4-bit selectable address bit for I^2C
- Supply Voltage: 3.3V±0.3V
- Industrial Temperature Range: -40°C to 85°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 42-contact TQFN (9mm x3.5mm)

Application

- Rack Server
- JBOD Storage

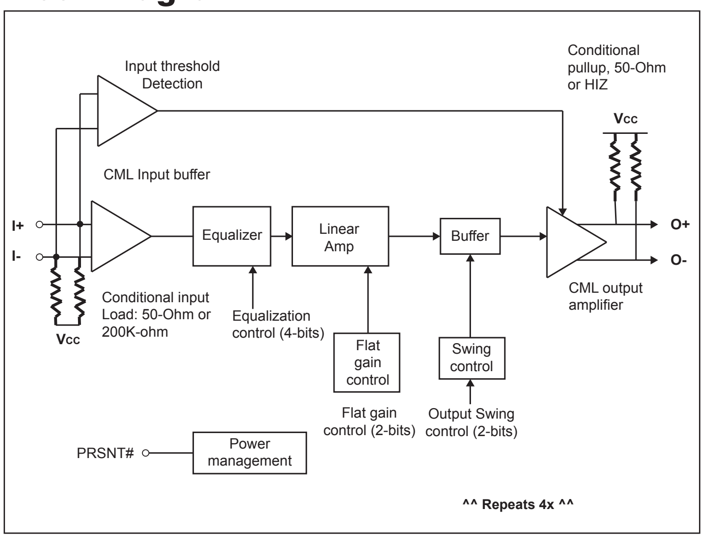
Description

The PI3EQX1204-C is a 4-differential-channel ReDriver™. The device reduces Inter-symbol interference by providing programmable linear equalization in output swing and flat gain. This is achieved by using the pin strapping option or I^2C Control to optimize performance over a variety of physical mediums.

The PI3EQX1204-C supports four 100Ω differential CML data I/O's and extends the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides signal integrity flexibility before the ReDriver, whereas the integrated linear amplifier/buffer circuitry provides signal integrity flexibility after the ReDriver.

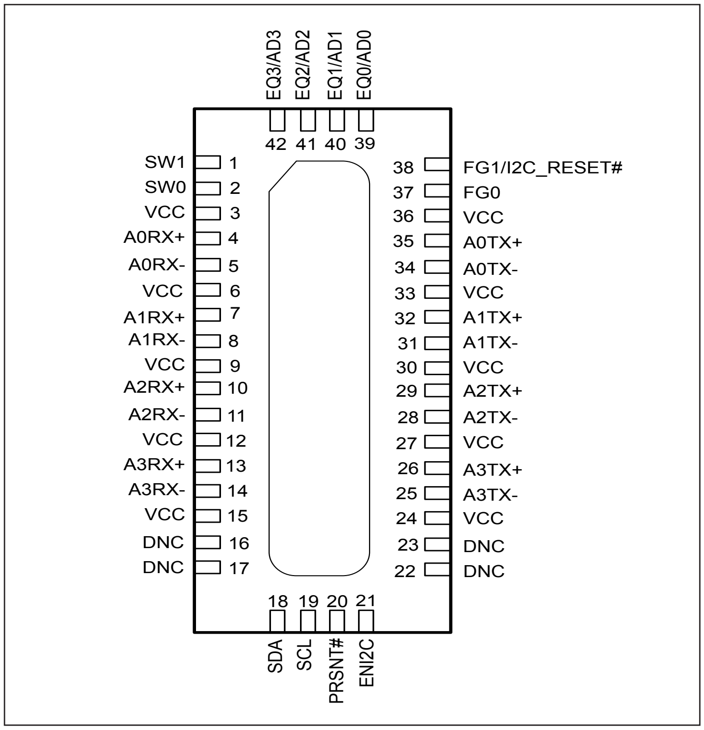
Block Diagram



Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

ReDriver is a trademark of Diodes Incorporated.

Pin Configuration (Top-Side View)



Pin Description

Pin #	Pin Name	Type	Description
Data Signals			
4 5	A0RX+ A0RX-	I I	CML inputs for Channel A0, with internal 50Ω pull-up and ~200KΩ pull-up otherwise.
35 34	A0TX+ A0TX-	O O	CML outputs for Channel A0, with internal 50Ω pull-up and high impedance otherwise.
7 8	A1RX+ A1RX-	I I	CML inputs for Channel A1, with internal 50Ω pull-up and ~200KΩ otherwise.
32 31	A1TX+ A1TX-	O O	CML outputs for Channel A1, with internal 50Ω pull-up and high impedance otherwise.
10 11	A2RX+ A2RX-	I I	CML inputs for Channel A2, with internal 50Ω pull-up and ~200KΩ otherwise.
29 28	A2TX+ A2TX-	O O	CML outputs for Channel A2, with internal 50Ω pull-up and high impedance otherwise.
13 14	A3RX+ A3RX-	I I	CML inputs for Channel A3, with internal 50Ω pull-up and ~200KΩ otherwise.
26 25	A3TX+ A3TX-	O O	CML outputs for Channel A3, with internal 50Ω pull-up and high impedance otherwise.

Pin Description Cont.

Pin #	Pin Name	Type	Description
Control Signals			
19	SCL	I	I^2C SCL clock input.
18	SDA	I	I^2C SDA data input.
42, 41, 40, 39	AD[3:0]	I	I^2C programmable address bits, with internal 100kΩ pull-up.
20	PRSNT#	I	This pin is active in both PIN mode(ENI2C=LOW) and I^2C mode (ENI2C=HIGH). Cable present detect input. This pin has internal 100KΩ pull-up. When High, a cable is not present, and the device is put in lower power mode. When LOW, the device is enabled and in normal operation.
21	ENI2C	I	When LOW, each channel is programmed by the external pin voltage. When HIGH, each channel is programmed by the data stored in the I2C bus.
42, 41, 40, 39	EQ[3:0]	I	Inputs with internal 100kΩ pull-up. This pins set the amount of Equalizer Boost in all channel when ENI2C is LOW.
1, 2	SW[1:0]	I	Inputs with internal 100kΩ pull-up. This pin sets the output Voltage Level in all channel when ENI2C is LOW.
38, 37	FG[1:0]	I	Inputs with internal 100KΩ pull up resistor. Sets the output flat gain level on all channels when ENI2C is low.
38	I^2C_RESET#	I	Inputs with internal 100KΩ pull up resistor. Reset pin for I^2C. When set low will reset the registers to default state.
16, 17, 22, 23	DNC		Do Not Connect
Power Pins			
3, 6, 9, 12, 15, 24, 27, 30, 33, 36	VCC	PWR	3.3V Supply Voltage
EP	GND	PWR	Exposed pad. Supply Ground

Description of Operation

Power Enable function:

One pin control or I^2C control, when PRSNT# is set to HIGH, the IC goes into power down mode, both input and output termination set to 200K and High impedance respectively. Individual Channel Enabling is done through the I^2C register programming.

Equalization Setting:

EQ[3:0] are the selection pins for the equalization selection for each channel.

Table 1. Equalization Setting

Equalizer setting							
EQ3	**EQ2**	**EQ1**	**EQ0**	**@ 3GHz**	**@ 4GHz**	**@ 5GHz**	**@ 6GHz**
0	0	0	0	3.6	4.5	5.5	6.8
0	0	0	1	4	5.1	6.2	7.6
0	0	1	0	4.4	5.6	6.9	8.4
0	0	1	1	4.7	6.1	7.5	9.1
0	1	0	0	5.1	6.6	8.1	9.8
0	1	0	1	5.5	7.1	8.7	10.4
0	1	1	0	5.9	7.6	9.2	11
0	1	1	1	6.2	8	9.7	11.5
1	0	0	0	6.6	8.5	10.2	12
1	0	0	1	6.9	8.9	10.7	12.5
1	0	1	0	7.3	9.3	11.1	12.9
1	0	1	1	7.6	9.7	11.5	13.3
1	1	0	0	8	10.1	11.9	13.7
1	1	0	1	8.2	10.5	12.3	14.1
1	1	1	0	8.6	10.8	12.7	14.4
1	1	1	1	8.9	11.1	13	14.7

Flat Gain Setting:

FG[1:0] are the selection bits for the DC value.

Table 2. Flat Gain Setting

Flat Gain Setting		
FG1	**FG0**	**dB**
0	0	-3.5
0	1	-1.5
1	0	0.5
1	1	2.5

Swing Setting:

Swing Setting: SW[1:0] are the selection bits for the output swing value.

Table 3. Swing Setting

SW1	SW0	mVp-p
0	0	700
0	1	800
1	0	900
1	1	1000

I²C Programming

Address assignment							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
1	1	1	AD3	AD2	AD1	AD0	1=R, 0=W

BYTE 0 Reserved

BYTE 1 Reserved

BYTE 2

Bit	Type	Power up condition		Control affected	Comment
7	R/W	0		A3 Power down	1 = Power down
6	R/W	0		A2 Power down	
5	R/W	0		A1 Power down	
4	R/W	0		A0 Power down	
3	R/W	0			
2	R/W	0			
1	R/W	0			
0	R/W	0			

BYTE 3

Bit	Type	Power up condition		Control affected	Comment
7	R/W	0	Channel A0 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

BYTE 4

Bit	Type	Power up condition		Control affected	Comment
7	R/W	0	Channel A1 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

I²C Programming cont.

BYTE 5					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel A2 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	
BYTE 6					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel A3 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	
BYTE 7-15 with '0' power up condition Reserved					

Transferring Data

Every byte put on the SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I^2C Data Transfer diagram).

Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, the PI3EQX1204-C will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I^2C Data Transfer diagram. The PI3EQX1204-C will generate an acknowledge after each byte has been received.

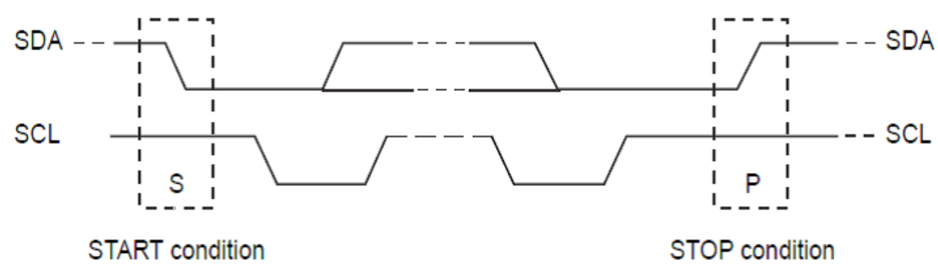
Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, the PI3EQX1204-C will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. For a write cycle, the first data byte following the address byte is an index byte that is used by the PI3EQX1204-C. Data is transferred with the most significant bit (MSB) first.

I2C Data Transfer

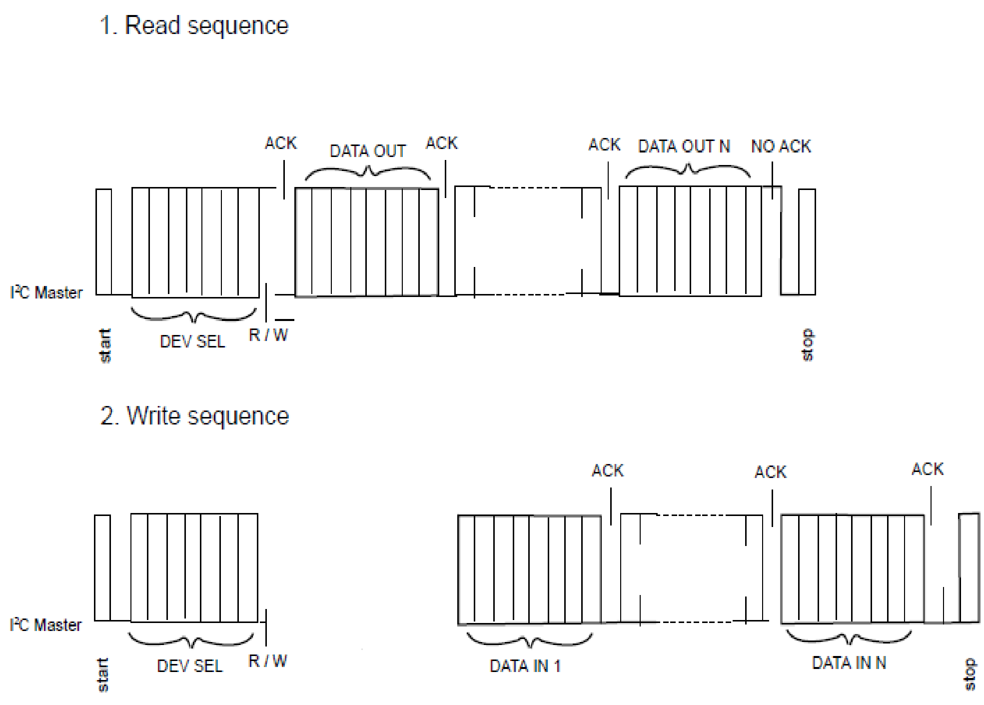
Start & Stop Conditions

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below



I^2C START and STOP conditions.

I²C Data Transfer



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +4.6V
DC SIG Voltage	–0.5V to V_{CC}+0.5V
Output Current	–25mA to +25mA
Power Dissipation Continuous	2.1W
Junction Temperature Tj	125°C
ESD, HBM	–2kV to +2kV

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics:

LVCMOS I/O DC Specifications (V_{CC} = 3.3 ± 0.3V, T_A = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IH}	DC input logic high		V_{CC}/2 + 0.7		V_{CC} + 0.3	V
V_{IL}	DC input logic low		-0.3		V_{CC}/2 - 0.7	V
V_{OH}	At IOH = -200µA		V_{CC} + 0.2			V
V_{OL}	At IOL = -200µA				0.2	V
V_{hys}	Hysteresis of Schmitt trigger input		0.8			V

SDA and SCL I/O for I2C-bus (V_{CC} = 3.3 ± 0.3V, T_A = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC input logic high		V_{CC}/2 + 0.7		V_{CC} + 0.3	V
V_{IL}	DC input logic low		-0.3		V_{CC}/2 - 0.7	V
V_{OL}	DC output logic low	I_{OL} = 3mA			0.4	V
V_{hys}	Hysteresis of Schmitt trigger input		0.8			V
t_{of}	Output fall time from VIHmin to VILmax with bus cap. 10-400pF				250	ns
f_{SCLK}	SCLK clock frequency				100	kHz

High Speed I/O AC/DC Specifications (V_{CC} = 3.3 ± 0.3V, T_A = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{RX}	RX AC coupling capacitance			220		nF
S_{11}	Input return loss	10MHz to 6GHz differential		11.0		dB
		1GHz to 6GHz common mode		5.0		
S_{22}	Output return loss	10MHz to 6GHz differential		11.5		dB
		1GHz to 6GHz common mode		4.8		
R_{IN}	DC single-ended input impedance			50		Ω
	DC Differential Input Impedance			100		

High Speed I/O AC/DC Specifications Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{OUT}	DC single-ended output impedance			50		Ω
	DC Differential output Impedance			100		
Z_{RX-HIZ}	DC input CM input impedance during reset or power down			200		kΩ
$V_{RX-DIFF-PP}$	Differential Input Peak-to-peak Voltage	Operational			1.2	Vppd
	Input source common-mode noise	DC – 200MHz			150	mVpp
$T_{TX-IDLE-SET-TO-IDLE}$	Max time to electrical idle after sending an EIOS			4	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Max time to valid diff signal after leaving electrical idle			4	8	ns
Vcc	Power supply voltage		3	3.3	3.6	V
P_{max}	Max Supply power	PRSNT#=0			1.3	W
I_{max}	Max Supply current				360	mA
P_{idle}	Supply power	PRSNT#=1			14.4	mW
t_{pd}	Latency	From input to output		0.5		ns
G_P	Peaking gain (Compensation at 6GHz, relative to 100MHz, 100mVp-p sine wave input)	EQ<3:0> = 1111		15.4		dB
		EQ<3:0> = 1000		12.5		
		EQ<3:0> = 0000		7.1		
		Variation around typical	-3		+3	dB
G_F	Flat gain (100MHz, EQ<3:0> = 1000, SW<1:0> = 10)	FG<1:0> = 11		2		dB
		FG<1:0> = 10		0		
		FG<1:0> = 01		-2		
		FG<1:0> = 00		-4		
		Variation around typical	-3		+3	dB
V_{1dB_100M}	-1dB compression point of output swing (at 100MHz)	SW<1:0> = 11		1370		mVppd
		SW<1:0> = 10		1280		
		SW<1:0> = 01		1040		
		SW<1:0> = 00		920		
V_{1dB_6G}	-1dB compression point of output swing (at 6GHz)	SW<1:0> = 11		1000		mVppd
		SW<1:0> = 10		940		
		SW<1:0> = 01		700		
		SW<1:0> = 00		600		
V_{Coup}	Channel isolation	100MHz to 6GHz[1], Figure 1		25		dB

High Speed I/O AC/DC Specifications Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Vnoise_input	Input-referred noise	100MHz to 6GHz, FG<1:0> = 11, EQ<3:0> = 0000, Figure 2		0.5		mV_{RMS}
		100MHz to 6GHz, FG<1:0> = 11, EQ<3:0> = 1010, Figure 2		0.4		
Vnoise_output	Output-referred noise(2)	100MHz to 6GHz, FG<1:0> = 11, EQ<3:0> = 0000, Figure 2		0.7		mV_{RMS}
		100MHz to 6GHz, FG<1:0> = 11, EQ<3:0> = 1010, Figure 2		0.8	1.6	

Note: (1) Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.

(2) Guaranteed by design and characterization.

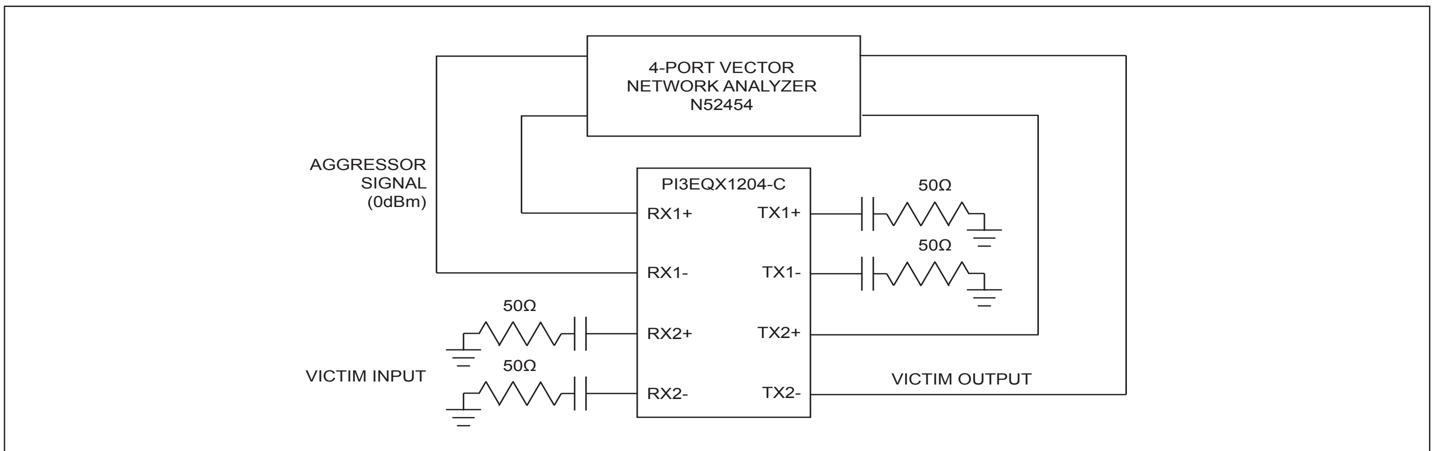


Figure 1. Channel-Isolation Test Configuration

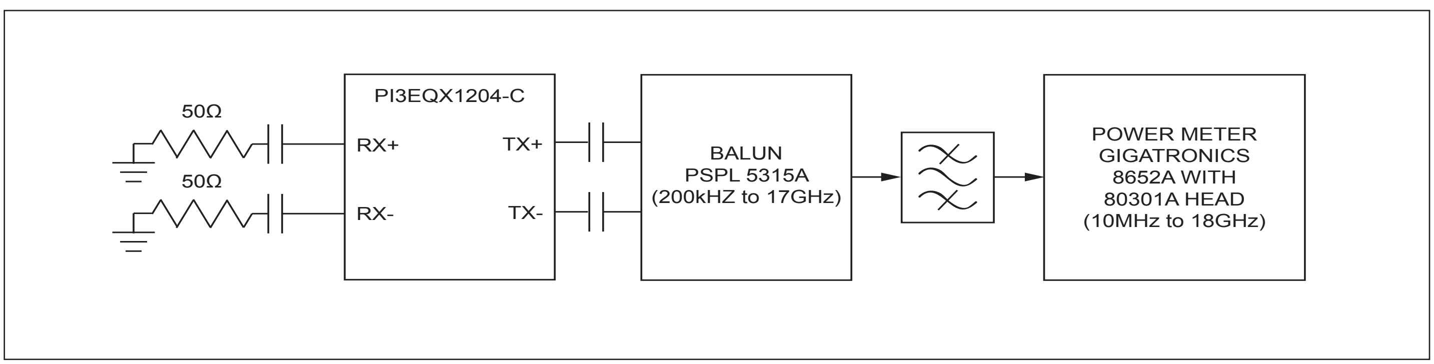
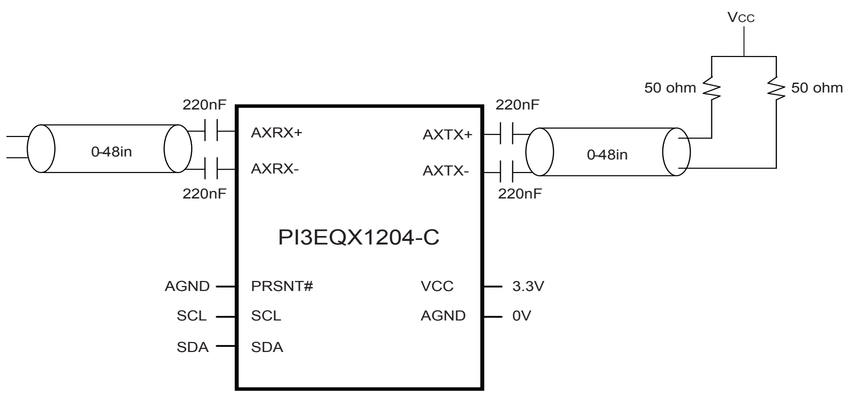


Figure 2. Noise Test Configuration

ESD Specification

- 2000V HBM
- 500V CDM

Application Diagram



AC/DC Specifications - SCL/SDA for I²C BUS

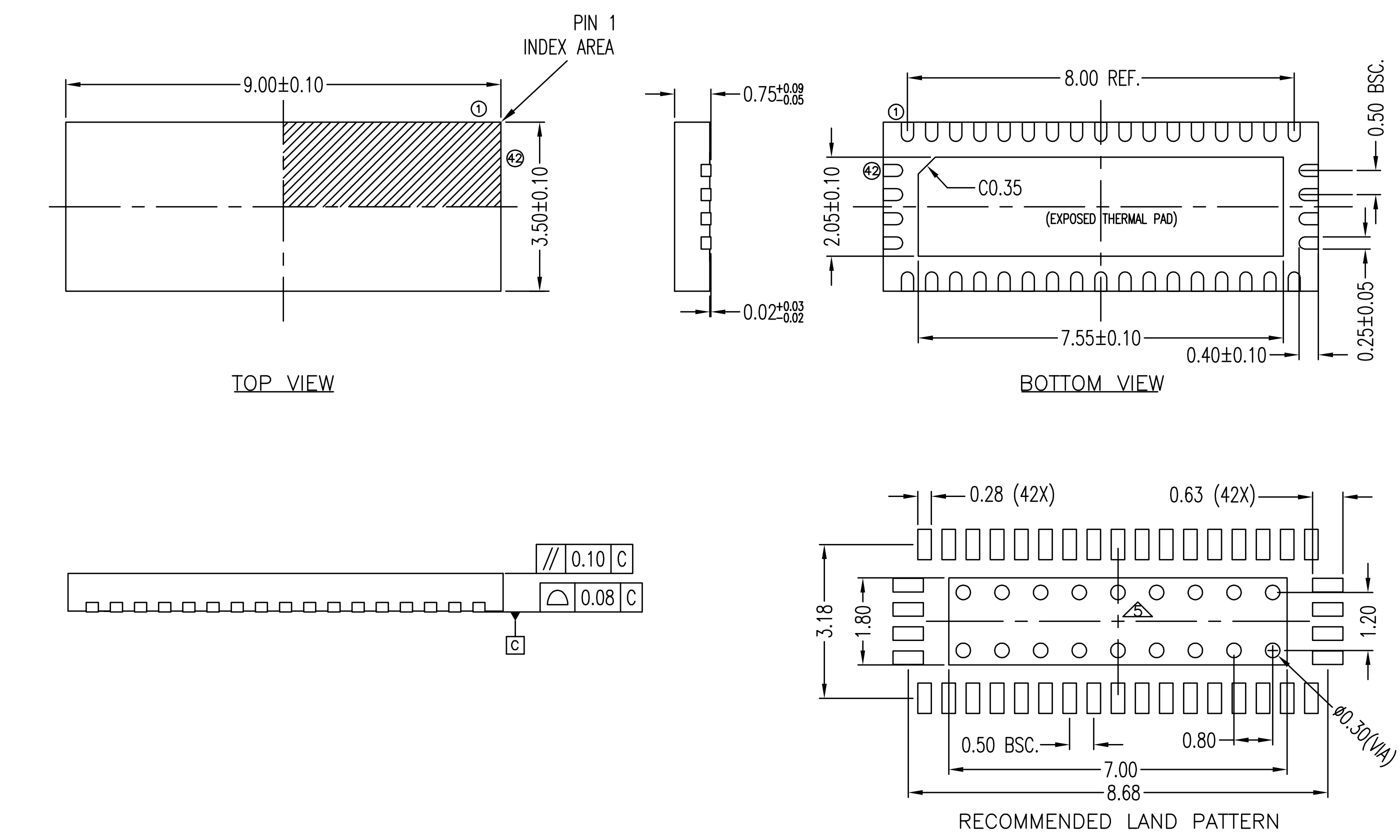
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IH}	DC input logic high		$V_{CC}/2 + 0.7$		$V_{CC} + 0.3$	V
V_{IL}	DC input logic low		-0.3		$V_{CC}/2 - 0.7$	V
V_{OL}	DC output logic low	I_{OL} = 3mA			0.4	V
Ipullup	Current Through Pull-Up Resistor or Current Source	High Power specification	3.0		3.6	mA
VDD	Nominal Bus Voltage		3.0		3.6	V
Ileak-bus	Input leakage per bus segment		-200		200	uA
Ileak-pin	Input leakage per device pin			-15		uA
CI	Capacitance for SDA/SCL				10	pF
Freq	Bus Operation Frequency				100k	Hz
TBUF	"Bus Free Time Between Stop and Start condition"		1.3			us
THD:STA	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At Ipull-up, Max	0.6			us
TSU:STA	Repeated start condition setup time		0.6			us
TSU:STO	Stop condition setup time		0.6			us
THD:DAT	Data hold time		0			ns
TSU:DAT	Data setup time		100			ns
Tlow	Clock low period		1.3			us
Thigh	Clock high period		0.6		50	us
tF	Clock/Data fall time				300	ns
tR	Clock/Data rise time				300	ns
tpor	"Time in which a device must be operation after power-on reset"				500	ms

Note: (1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Compliant to I²C physical layer specification.
(4) Ensured by Design. Parameter not tested in production.

Part Marking

Z: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Package Mechanical: 42-TQFN (ZH)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL IS RECOMMENDED).

DATE: 04/25/17

DESCRIPTION: 42-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH (ZH42)

DOCUMENT CONTROL #: PD-2035 REVISION: G

17-0266

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX1204-CZHEX	ZH	42-Contact, Very Thin Quad Flat No-Lead (TQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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