Description

The APR349 is a secondary-side MOSFET driver for synchronous rectification, which can effectively reduce the secondary-side rectifier power dissipation and provide a high-performance solution.

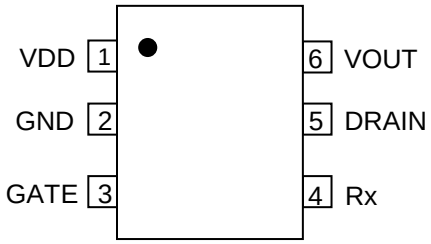
The APR349 supports continuous or discontinuous conduction mode (CCM and DCM) and quasi-resonant flyback operation. It utilizes an intelligent control method to realize on-time control, which not only provides a short turn-on and turn-off delay to reduce power loss, but also eliminate the false trigger of resonant ring and keep safe operation without adding any external components or circuitry.

The APR349 can be charged by internal PLR (Pulse Linear Regulator) at low system output voltage, and provide a wide output operation voltage from 3.3V to 24V.

The APR349 is available in SOT26 (Type CJ) package.

Pin Assignments

(Top View)



SOT26 (Type CJ)

Features

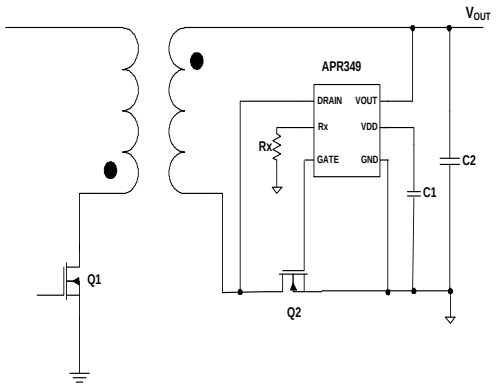
- Support Flyback Synchronous Rectification with CCM/DCM/QR Operation Mode
- Intelligent Control to Minimize Turn-On and Turn-Off Delay
- Smart-Blanking Control to Prevent Shoot-Through
- Supports Both High-Side and Low-Side Application
- Built-in PLR Power Supply for Low System Output Voltage
- Internal UVLO Protection
- Fewest External Components
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

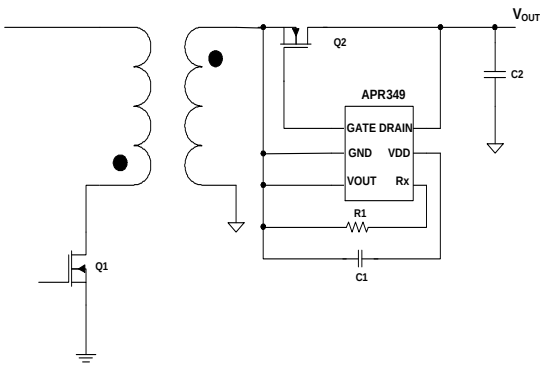
- Adaptive Chargers for Cellular Phones, Digital Cameras, and Power Tools
- AC/DC Adapters
- Battery-Powered Systems
- All SMPS with High-Efficiency Requirements

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



Low-Side Application

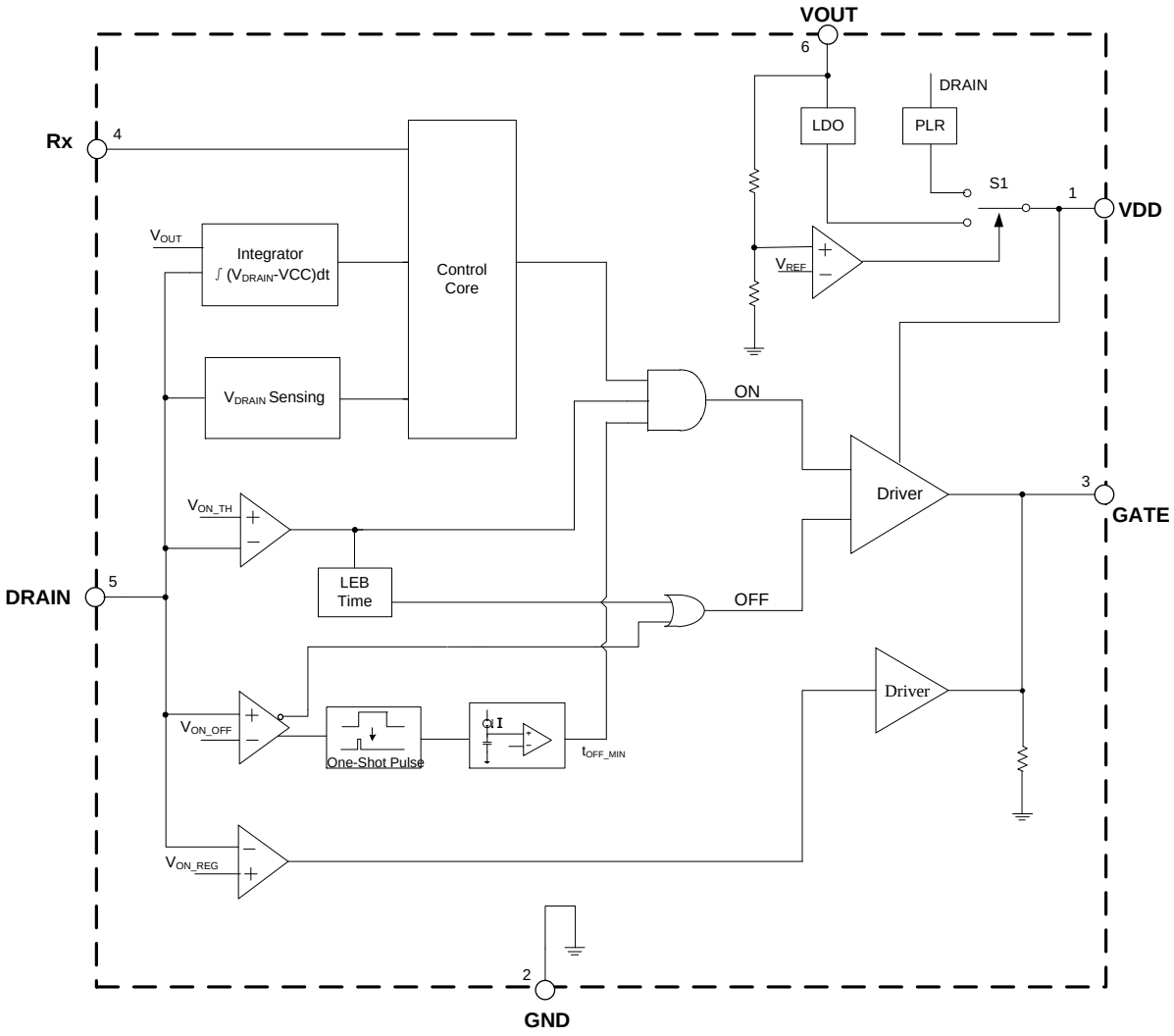


High-Side Application

Pin Descriptions

Pin Number	Pin Name	Function
1	VDD	Supply input. It provides bias voltage for the internal logic circuit and the MOSFET driver.
2	GND	Ground, also used as FET source sense reference for DRAIN
3	GATE	Synchronous Rectification MOSFET Gate Drive
4	Rx	Program a voltage reference with a resistor from Rx to GND, to enable synchronous rectification MOSFET drive signal
5	DRAIN	Synchronous Rectification MOSFET Drain Voltage Sense Input
6	VOUT	Internal Linear Regulator Input

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{OUT}	Supply Voltage	-0.3 to 28	V
V_{DRAIN}	Voltage at DRAIN Pin (Note 5)	-0.7 to 120	V
V_{GATE}	Voltage at GATE Pin	-0.3 to 7	V
V_{RX}	Voltage at Rx Pin	-0.3 to 7	V
P_D	Power Dissipation at T_A = +25°C	0.6	W
T_J	Operating Junction Temperature	+150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 6)	200	°C/W
ESD	Human Body Model	5000	V
	Charged Device Model	1500	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

5. If -0.7V to -2V negative voltage is applied to DRAIN pin, the period of negative pulse is lower than 0.1μs.

6. Test condition: Device mounted on FR-4 substrate PC board, 1mm width,20mm length, 2oz power lead.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{OUT}	Supply Voltage	0	24	V
T_A	Ambient Temperature	-40	+85	°C

Electrical Characteristics (@ V_{OUT} = 5V, T_A = -40°C < T_A < +85°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Output Voltage (VOUT Pin)						
V_{OUT_ON}	LDO Enable Threshold When VOUT Rising	—	4.1	4.4	4.7	V
V_{OUT_OFF}	LDO Disable Threshold When VOUT Falling	—	4.0	4.3	4.6	V
Internal Supply Section (VDD Pin)						
V_{DD_ON}	V_{DD} Startup Voltage	—	3.55	3.75	3.95	V
V_{DD_OFF}	V_{DD} UVLO Voltage	—	3.35	3.55	3.75	V
V_{DD_REG}	VDD Regulation Voltage（Include $V_{VDD\_REG\_OUT}$, $V_{VDD\_REG\_DRAIN}$）	$V_{VDD\_REG\_OUT}$, V_{OUT} = 12V, V_{DRAIN} = 12V	5	5.5	6	V
		$V_{VDD\_REG\_DRAIN}$, V_{OUT} = 3V, V_{DRAIN} = 12V	5.3	5.7	6.5	V
$I_{STARTUP}$	V_{DD} Startup Current	V_{OUT} = 0, V_{DD} = V_{DD_ST} - 0.1V	—	140	165	μA
I_{MAX_VDD}	Maximum Charging Current from LDO to VDD	V_{OUT} = 12V	65	90	120	mA
I_{Q_VDD}	Quiescent Current	V_{DD} = 5.0V, V_{OUT} = 0	—	215	255	μA
DRAIN Detection (DRAIN Pin)						
V_{ON_TH}	Gate Turn-On Threshold Voltage	Voltage at DRAIN Pin	-225	-200	-175	mV
V_{ON_REG}	Gate Turn-On Regulation Voltage	Voltage at DRAIN Pin	-50	-40	-30	mV
V_{ON_OFF}	Gate Turn-Off Threshold Voltage	Voltage at DRAIN Pin	-15	-7	0	mV
I_{CHG_VDD}	Maximum Charging Current from DRAIN to VDD	V_{DRAIN} = 12V	55	75	100	mA
Gate Driver (GATE Pin)						
V_{GATE_H}	Gate Output High Voltage	V_{DD} = 5V	4.9	—	5	V
$V_{GATE\_L\_PRE}$	Gate Output Low Voltage before Startup	V_{DD} = 0, V_{DRAIN} = 8V, I_{LOAD} = 100mA	—	200	300	mV
V_{GATE_L}	Gate Output Low Voltage after Startup	V_{DD} ⩾ V_{DD_ON}, I_{LOAD} = 100mA	—	70	140	mV
I_{SOURCE_MAX}	Maximum GATE Sourcing Current	(Note 7)	—	0.6	—	A
I_{SINK_MAX}	Maximum GATE Sinking Current	(Note 7)	—	3.5	—	A
R_{GATE_L}	GATE Pull-Low Resistance	I_{G_LOAD} = 100mA, V_{DD} = 5V	—	0.7	1.4	Ω
Control Section						
t_{ON_MIN}	GATE Minimum On Time	—	0.65	0.9	1.15	μs
t_{OFF_MIN}	GATE Minimum Off Time	—	0.35	0.5	0.71	μs
t_{D_ON}	Turn-On Delay	C_{LOAD} = 2.2nF	—	30	60	ns
t_{D_OFF}	Turn-Off Propagation Delay	—	—	15	45	ns
Kqs	A Fixed Coefficient Correlated with Voltage-Second Area Criteria	—	0.43	0.5	0.57	mA*μs

Note: 7. Guaranteed by design.

Operation Description

V_{DD} Regulator and UVLO Protection

The V_{DD} is supplied by the PLR (Pulse Linear Regulator) from the drain voltage, or LDO from the V_{OUT} voltage. When the APR349 operates at a low voltage output condition, a Pulse Linear Regulator is integrated in the controller to provide voltage to the V_{DD} pin, in which the system output voltage may drop to 2V. Meanwhile, when the system output voltage is higher than 4.75V, the V_{DD} bias voltage generating circuit will change from the PLR to the LDO circuit.

When the V_{DD} provides bias voltage for the controller, a capacitor (typical 3.3μF) should be connected between the V_{DD} pin and GND pin. The APR349 also has UVLO protection. When V_{DD} drops below V_{DD_UVLO}, the IC will stop providing gate drive pulse.

GATE Turn-On Logic

The APR349 determines the synchronous rectification MOSFET turn-on moment by monitoring the MOSFET drain-to-source voltage. When the drain voltage is lower than the turn-on threshold voltage V_{ON_TH}, the IC outputs a positive drive voltage after a turn-on delay time (t_{D_ON}). The MOSFET will turn on and the current will transfer from the body diode into the MOSFET's channel.

Moreover, the device also sets an internally fixed, volt-sec product threshold to prevent false turn-on within ringing voltage cycle. Regarding the sensed voltage of the DRAIN pin, the volt-second product above the V_{CC} voltage at the primary switch on-time is much higher than the volt-second product of ringing voltage above V_{CC}. Therefore, the APR349 can turn on the synchronous rectifier depending on the detected volt-second product of drain voltage above V_{CC}. The APR349 has an internal parameter Kqs, which multiplies Rx resistor value to generate volt-second product threshold. Thus, changing the Rx resistor can adjust the volt-second product threshold.

$$\mathrm{Area2} = \mathrm{Rx} * \mathrm{Kqs}$$

In general, the Area1 and Area3 values depend on system design. Area2 should be set in the middle of Area1 and Area3 to ensure suitable design margins.

$$\mathrm{Area3} < Rx * Kqs < Area1$$

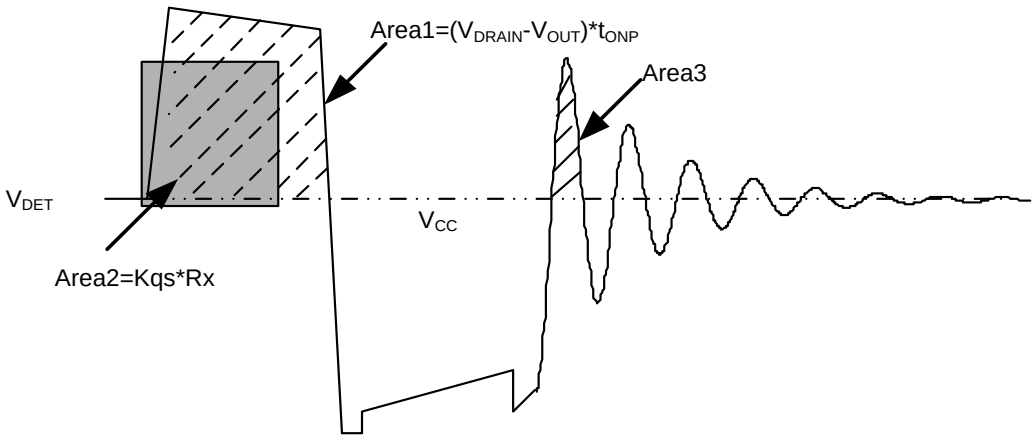


Figure 1. Volt-Second Product Function

Operation Description (continued)

GATE Voltage Regulation/Auto-Tracking

The minimum on-time (t_{ON_MIN}) blanking period aims to prevent an accidental turn-off due to interference of ringing noise voltage. When the controlled MOSFET gate turns on, some ringing noise will be generated. Utilizing the minimum on-time timer to blank the V_{THOFF} comparator, this keeps the SR MOSFET on for at least the minimum on-time. The gate driver can be pulled down quickly to zero when V_{DRAIN} ringing voltage goes over 2V during this period.

Once the synchronous rectification gate outputs a high-level voltage, the secondary-side current goes through the synchronous rectification MOSFET. The voltage drop on the MOSFET is calculated by $R_{DS(ON)}$ × secondary-side current. After minimum turn-on time t_{ON_MIN}, the IC continuously monitors V_{DRAIN} by the DRAIN pin and generates a pull-down current from the MOSFET gate until drain voltage equals -40mV. As shown in Figure 2, the MOSFET drain-to-source voltage would remain around -40mV (V_{ON_REG}) with the secondary-side current decreasing.

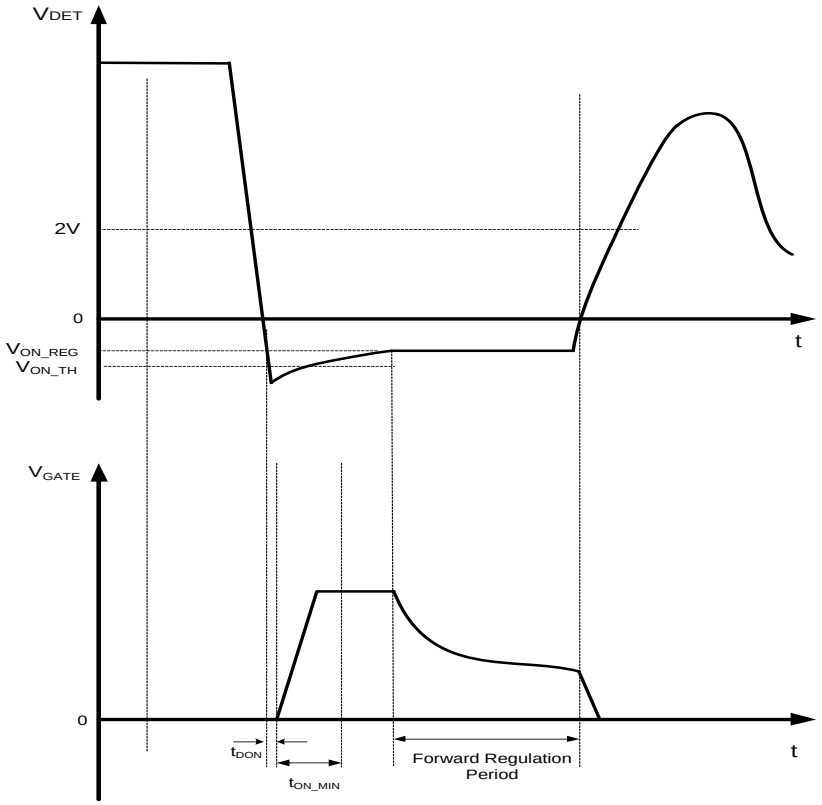


Figure 2. Forward Regulation Operation Principle

Operation Description (continued)

Smart-Blanking Control

Because of the resonance oscillation of the primary inductance and equivalent output capacitance of the switching device, the voltage on the MOSFET drain pin has an under damped voltage ring in DCM operation mode. In some special occasions, such as output transition periods or light-load conditions, the SR MOSFET would turn on falsely during the t_{OFF} period when the ring of the V_{DRAIN} meets the conduction requirement. When the turn–on of the primary MOSFET meets the false turn-on of the SR, the transformer would immediately be shoot through. To avoid such faults, the device has a built-in smart blanking function to prevent continuous false turn-ons. The SR gate driver will blank for a period of 20μs when detecting a false turn-on twice in a period of 4μs in t_{OFF} period. Figure 3 shows a smart-blanking control method.

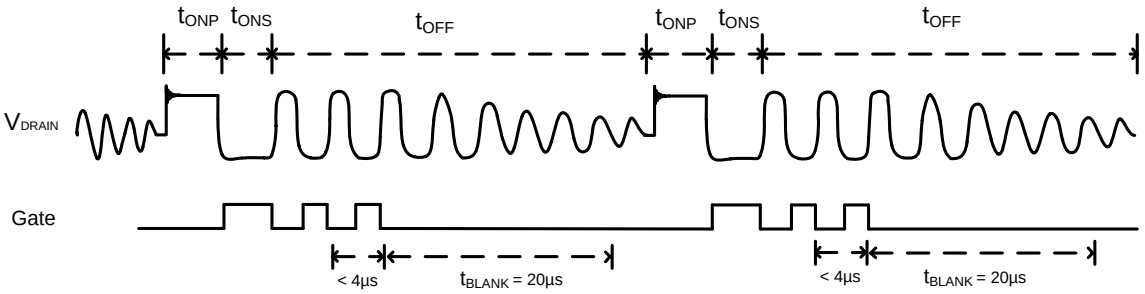
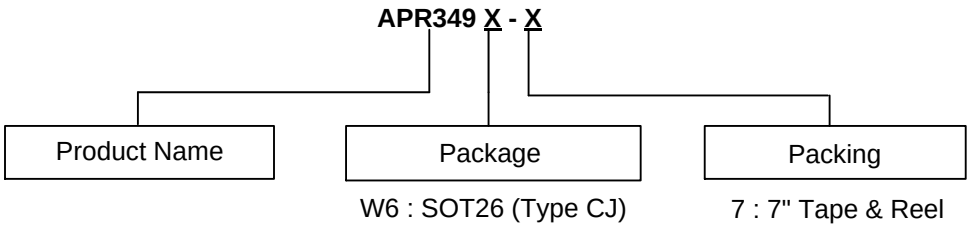


Figure 3. Smart-Blanking Control Method

GATE Turn-Off Logic

When V_{DRAIN} rises to the turn-off threshold (-7mV), the synchronous rectification MOSFET gate voltage will be pulled down quickly from a low voltage to zero after a very short turn-off delay. For CCM mode, the secondary V_{DRAIN} will rise up as the primary MOSFET turns on. Once drain voltage rises to the turn-off threshold, the gate driving signal will immediately shut down.

Ordering Information

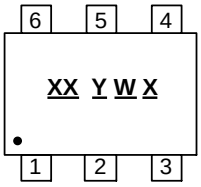


Package	Temperature Range	Part Number	Identification Code	7''Tape and Reel	
				Quantity	Part Number Suffix
SOT26 (Type CJ)	-40°C to +85°C	APR349W6-7	D9	3000/Tape and Reel	-7

Marking Information

SOT26 (Type CJ)

(Top View)

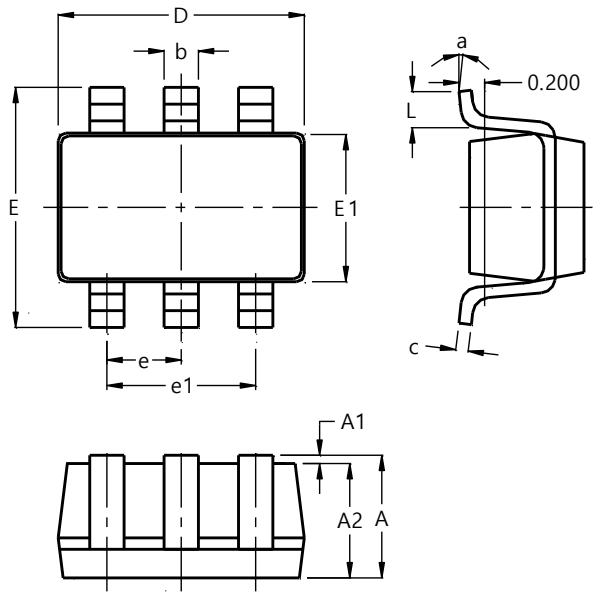


XX : Identification Code
Y : Year 0 to 9
W : Week : A to Z : 1 to 26 Week;
a to z : 27 to 52 Week; z Represents 52 and 53 Week
X : Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26 (Type CJ)

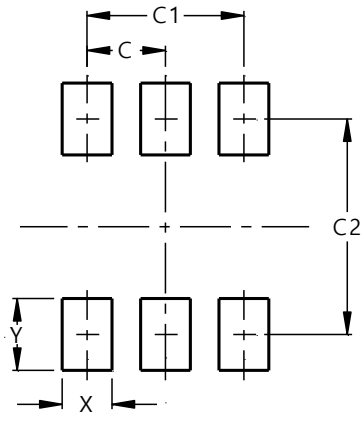


SOT26 (Type CJ)			
Dim	**Min**	**Max**	**Typ**
A	1.050	1.250	--
A1	0.00	0.10	--
A2	1.050	1.150	--
b	0.300	0.500	--
c	0.100	0.200	--
D	2.820	3.020	--
E	2.650	2.950	--
E1	1.500	1.700	--
e	0.950BSC		
e1	1.800	2.000	--
L	0.300	0.600	--
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26 (Type CJ)



Dimensions	Value (in mm)
C	0.95
C1	1.90
C2	2.40
X	0.60
Y	1.00

Mechanical Data

- Moisture Sensitivity: MSL Level 1 per JESD22-A113
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 e3
- Weight: 0.016/0.017 grams (Approximate)

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