

High-Performance Differential Fanout Buffer

Features

- 10 Differential Outputs with Two Banks
- User Configurable Output Signaling Standard for Each Bank:
 - LVDS or LVPECL or HCSL
- LVCMOS Reference Output up to 200MHz
- Up to 1.5GHz Output Frequency for Differential Outputs
- Ultra-Low Additive Phase Jitter:
 - <0.02ps (typ) (Differential 156.25MHz, 12KHz to 20MHz Integration Range)
 - <0.01ps (typ) (Differential 156.25MHz, 10kHz to 1MHz Integration Range)
- Selectable Reference Inputs Support Either Single-Ended or Differential or Xtal
- Low Skew Between Outputs within Banks (<40ps)
- Low Delay from Input to Output (Tpd typ. <0.9ns)
- Separate Input Output Supply Voltage for Level Shifting
- 2.5V/3.3V Power Supply
- Industrial Temperature Support
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.
- Packaging (Pb-free & Green):
 - 48-Pin, TQFN (ZD)

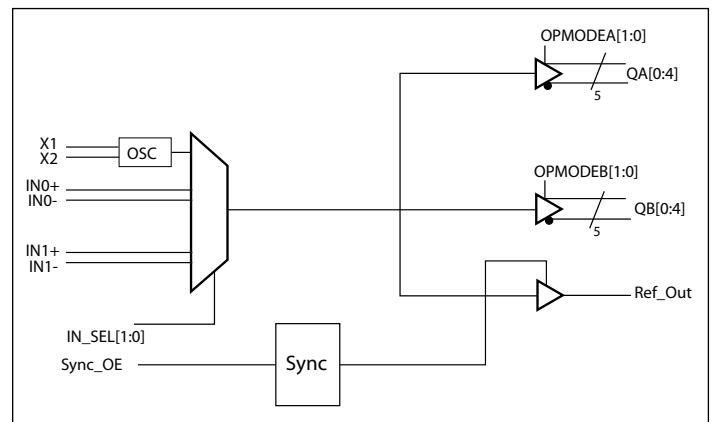
Applications

- Networking Systems Including Switches and Routers
- High-Frequency Backplane Based Computing and Telecom Platforms

Description

The DIODES™ PI6C49S1510B is a high-performance fanout buffer device which supports up to 1.5GHz frequency. It also integrates a unique feature with user-configurable output signaling standards on per bank basis, which provides great flexibility to users. The device also uses Diodes' proprietary input detection technique to make sure illegal input conditions are detected and reflected by output states. This device is ideal for systems that must distribute low jitter clock signals to multiple destinations.

Block Diagram



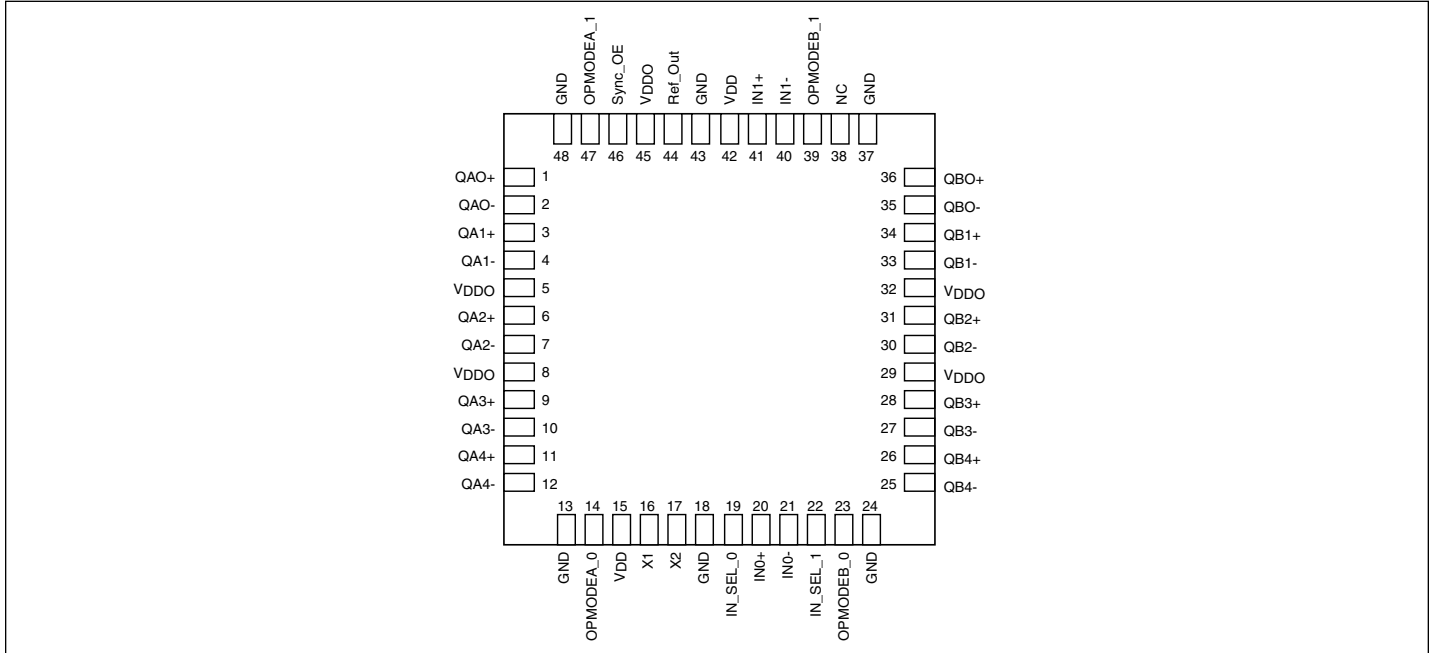
Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Pin Configuration



Pin Description

Pin #	Pin Name	Type	Description
1, 2	QA0+ QA0-	Output	Bank A differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
3, 4	QA1+ QA1-	Output	Bank A differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
5, 8, 29, 32, 45	VDDO	Power	Power supply pins for IO
6, 7	QA2+ QA2-	Output	Bank A differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
9, 10	QA3+ QA3-	Output	Bank A differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
11, 12	QA4+ QA4-	Output	Bank A differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
13, 18, 24, 37, 43, 48	GND	Power	Power supply ground
14, 47	OPMODEA	Input	Pulldown Output mode select for Bank A. See Table 2 for functions, LVCMOS/LVTTL interface levels
15, 42	V _{DD}	Power	Power supply pins
16	X1	Input	XTAL input, can also be used as single ended input pin
17	X2	Output	XTAL output. If X1 is used as a single ended input pin, X2 is to be left open

Pin Description Cont.

Pin #	Pin Name	Type		Description
19, 22	IN_SEL	Input	Pulldown	Input clock select. See Table 1 for function. LVCMOS/LVTTL interface levels.
20	IN0+	Input	Pulldown	Reference input 0, internal bias to $0.33V_{DD}$
21	IN0-	Input	Pullup/ Pulldown	Inverted reference input 0, internal bias to $0.42V_{DD}$
23, 39	OPMODEB	Input	Pulldown	Output mode select for Bank B. See Table 2 for functions, LVCMOS/LVTTL interface levels
26, 25	QB4+	Output		Bank B differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
	QB4-			
28, 27	QB3+	Output		Bank B differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
	QB3-			
31, 30	QB2+	Output		Bank B differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
	QB2-			
34, 33	QB1+	Output		Bank B differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
	QB1-			
36, 35	QB0+	Output		Bank B differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
	QB0-			
38	NC	—		Do not connect
40	IN1-	Input	Pullup/ Pulldown	Inverted reference input, internal bias to $0.42V_{DD}$
41	IN1+	Input	Pulldown	Reference input 1, internal bias to $0.33V_{DD}$
44	Ref_Out	Output		Reference output, CMOS
46	Sync_OE	Input	Pulldown	Synchronous output enable for Ref_Out. See Table 3 for functions.

Function Table

Table 1: Input Select Function

IN_SEL [1]	IN_SEL [0]	Function
0	0	IN0 is the selected reference input
0	1	IN1 is the selected reference input
1	X	XTAL is the selected input

Table 2: Output Mode Select Function

OPMODEA/B [1]	OPMODEA/B [0]	Output Bank A/Bank B Mode
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Hi-Z

Table 3: Reference Output Enable Function

Sync_OE	Ref_Out
0	Hi-Z
1	Output Enabled

Table 4: Illegal Input Level Function

Input Illegal Status	Output Status
Input Open	Logic Low
Input Both High	Logic Low
Input Both Low	Logic Low

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	-55°C to +150°C
Supply Voltage to Ground Potential (V_{DD}, V_{DDO})	-0.5V to +4.6V
Inputs (Referenced to GND)	-0.5V to $V_{DD}+0.5V$
Clock Output (Referenced to GND).....	-0.5V to $V_{DD}+0.5V$
Latch up	200mA
ESD Protection (Input)	2000V min (HBM)
Junction Temperature	150°C max

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage	—	2.375	—	3.465	V
V_{DDO}	Output Supply Voltage	—	2.375	—	3.465	V
I_{DD}	Core Power Supply Current	—	—	90	120	mA
I_{DDO}	Output Power Supply Current	All LVPECL outputs unloaded	—	150	190	
		All LVDS outputs loaded	—	110	130	
		All HCSL outputs unloaded	—	80	140	
T_A	Ambient Operating Temperature ⁽¹⁾	—	-40	—	85	°C
T_B	PCB Operating Temperature ⁽¹⁾	—	-40	—	105	°C

Note 1: Either T_A or T_B used as operating condition.

DC Electrical Specifications - Differential Inputs

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	Input = V_{DD}	—	—	150	μA
I_{IL}	Input Low Current	Input = GND	-150	—	—	μA
C_{IN}	Input Capacitance	—	—	3	—	pF
V_{IH}	Input High Voltage	—	—	—	$V_{DD}+0.3$	V
V_{IL}	Input Low Voltage	—	-0.3	—	—	V
V_{ID}	Input Differential Amplitude PK-PK	—	0.15	—	1.3	V
V_{CM}	Common Mode Input Voltage	—	0.25	—	$V_{DD}-1.2$	V
ISO_{MUX}	MUX Isolation	—	—	-89	—	dBc

DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	Input = V_{DD}	—	—	150	μA
I_{IL}	Input Low Current	Input = GND	-150	—	—	μA
V_{IH}	Input High Voltage	$V_{DD}=3.3V$	2.0	—	$V_{DD}+0.3$	V
V_{IL}	Input Low Voltage	$V_{DD}=3.3V$	-0.3	—	0.8	V
V_{IH}	Input High Voltage	$V_{DD}=2.5V$	1.7	—	$V_{DD}+0.3$	V
V_{IL}	Input Low Voltage	$V_{DD}=2.5V$	-0.3	—	0.7	V

DC Electrical Specifications - LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	—	$V_{DDO}-1.4$	—	$V_{DDO}-0.9$	V
V_{OL}	Output Low Voltage	—	$V_{DDO}-2.2$	—	$V_{DDO}-1.7$	V

DC Electrical Specifications - LVDS Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	—	—	1.43	—	V
V_{OL}	Output Low Voltage	—	—	1.0	—	V
V_{ocm}	Output Commode Voltage	—	—	1.25	—	V
DV_{ocm}	Change in V_{ocm} Between Completely Output States	—	—	—	50	mV
R_o	Output Impedance	—	85	—	140	Ω

DC Electrical Specifications – HCSL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	2.5V	480	—	900	mV
		3.3V	600	850	1050	mV
V_{OL}	Output Low Voltage	—	-150	—	150	mV

DC Electrical Specifications – LVCMOS Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V _{OH}	Output High Voltage	V _{DDO} =3.3V ±5%, I _{OH} = 8mA	2.3	—	—	V
		V _{DDO} =2.5V ±5%, I _{OH} = 8mA	1.5	—	—	V
V _{OL}	Output Low Voltage	V _{DDO} =3.3V ±5%, I _{OL} = -8mA	—	—	0.5	V
		V _{DDO} =2.5V ±5%, I _{OL} = -8mA	—	—	0.4	V
V _{OH}	Output High Voltage	V _{DDO} =3.3V ±5%, I _{OH} = 24mA	2.1	—	—	V
		V _{DDO} =2.5V ±5%, I _{OH} = 16mA	1.5	—	—	V
V _{OL}	Output Low Voltage	V _{DDO} =3.3V ±5%, I _{OL} = -24mA	—	—	1	V
		V _{DDO} =2.5V ±5%, I _{OL} = -16mA	—	—	0.8	V
R _{IUT}	Output Impedance	V _{DDO} = 3.3V ±5%	—	17	—	Ω
		V _{DDO} = 2.5V ±5%	—	22	—	Ω

AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units	
F _{OUT}	Clock Output Frequency	LVPECL, LVDS	—	—	1500	MHz	
		HCSL	—	—	250		
T _r	Output Rise Time	From 20% to 80%	LVPECL	120	150	300	ps
			LVDS	120	150	300	
			HCSL	300	—	700	
T _f	Output Fall Time	From 80% to 20%	LVPECL	120	150	300	ps
			LVDS	120	150	300	
			HCSL	300	—	700	
T _{ODC}	Output Duty Cycle	Frequency <650MHz, V _{ID} ≥ 400mV	LVPECL, HCSL (<250MHz)	48	—	52	%
			LVDS	47	—	53	
		Frequency <1GHz, V _{ID} ≥ 400mV	LVPECL	45	—	55	
			LVDS	45	—	55	
		Frequency <1.5GHz, V _{ID} ≥ 400mV	LVDS	40	—	60	
Frequency <1.5GHz, V _{ID} ≥ 400mV	LVPECL	40	—	60			
V _{PP}	Output Swing Single-Ended	LVPECL Outputs @ <1GHz	500	—	1100	mV	
		LVPECL Outputs @ >1GHz	400	—	1000		
		LVDS Outputs @ <1GHz	250	—	600		
		LVDS Outputs @ >1GHz	250	—	550		

AC Electrical Specifications – Differential Outputs Cont.

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
T _j	Buffer Additive Jitter RMS	156.25MHz, 12kHz to 20MHz	—	0.02	—	ps
		156.25MHz, 10kHz to 1MHz	—	0.01	—	ps
V _{CROSS}	Absolute Crossing Voltage	HCSL	—	460	—	mV
DV _{CROSS}	Total Variation of Crossing Voltage	HCSL	—	—	140	mV
T _{SK}	Output Skew	10 outputs devices, outputs in same bank with same load at DUT	—	15	40	ps
T _{PD}	Propagation Delay	LVPECL, LVDS @ 3.3V, 100MHz	—	570	—	ps
		HCSL @ 3.3V, 100MHz	—	900	—	ps
T _{OD}	Valid to HiZ		—	—	80	ns
T _{OE}	HiZ to valid		—	—	80	ns
T _{P2P Skew}	Part-to-Part Skew ⁽¹⁾		—	80	120	ps

AC Electrical Specifications – CMOS

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F _{OUT}	Ref_Out Frequency	XTAL input	10	—	50	MHz
		Reference input	—	—	200	MHz
T _j	Buffer Additive Jitter RMS	XTAL input	—	0.3	—	ps
		Reference input	—	0.03	—	ps
t _r /t _f	Rise Time, Fall Time	C _L = 10pF	—	1.5	—	ns
T _{ODC}	Output Duty Cycle	C _L = 10pF	45	—	55	%
t _{PD}	Propagation Delay	3.3V, 25MHz	—	2200	—	ps
t _S	Setup Time	—	300	—	—	ps
t _{SOD}	Clock Edge to Output Disable	Ref_Out	2	—	4	cycles
t _{SOE}	Clock Edge to Output Enable	Ref_Out	2	—	4	cycles

Notes:

1. This parameter is guaranteed by design.

Crystal Characteristics

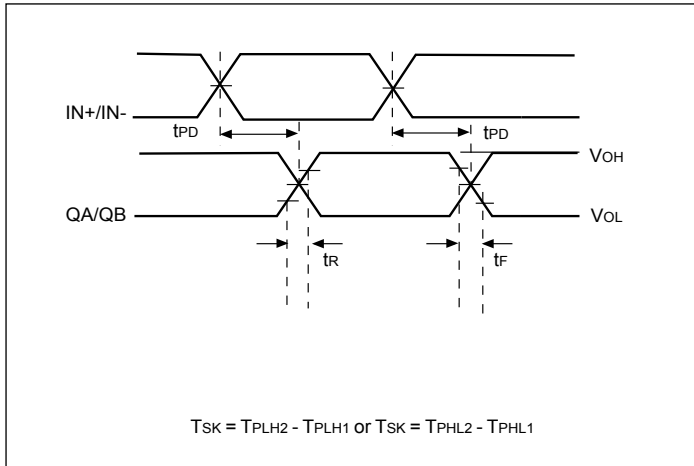
Parameter	Min.	Typ.	Max.	Units
Mode of Oscillation	Fundamental			
Frequency Range	10	—	50	MHz
Equivalent Series Resistance (ESR)	—	—	70	Ω
Shunt Capacitance	—	—	7	pF
Load Capacitance	10	—	18	pF
Drive Level	—	—	500	μ W

Recommended Crystals

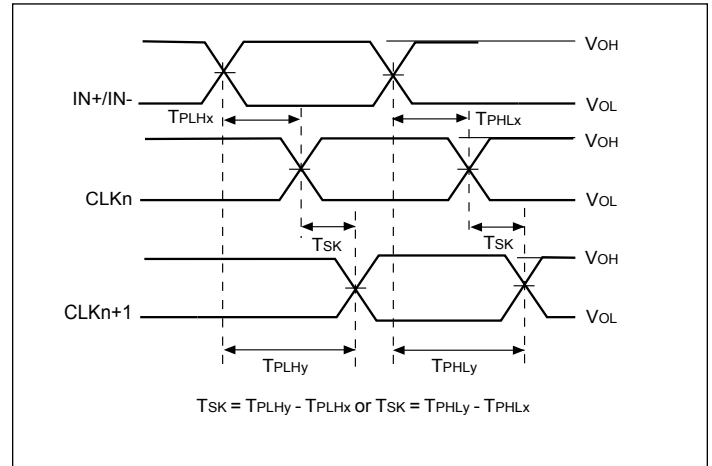
Diodes recommends:

- a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, \pm 30ppm
- b) FY2500091, SMD 5x3.2(4P), 25M, CL=18pF, \pm 30ppm
- c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, \pm 20ppm

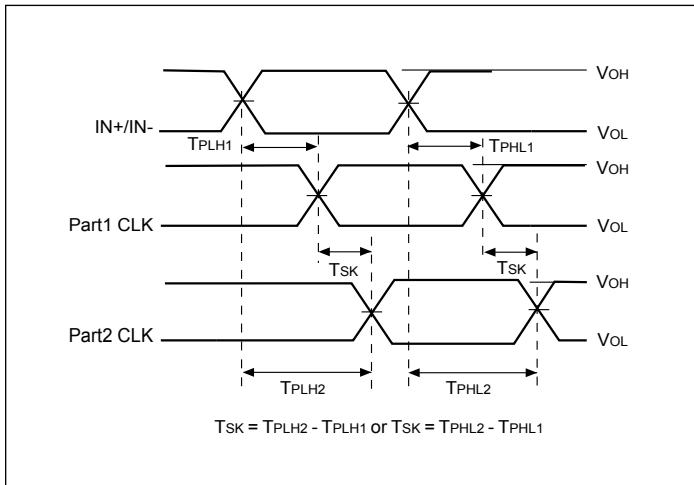
Propagation Delay (T_{PD})



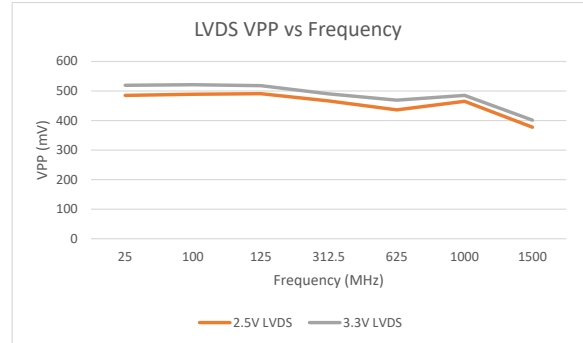
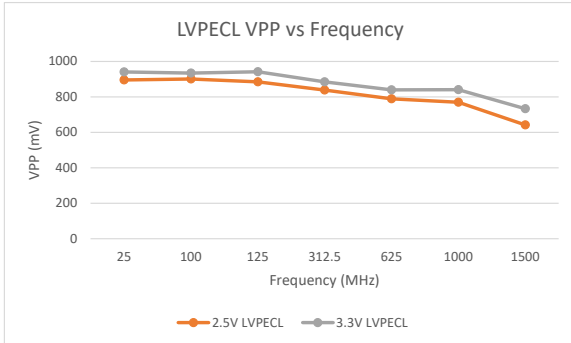
Output Skew (T_{SK})



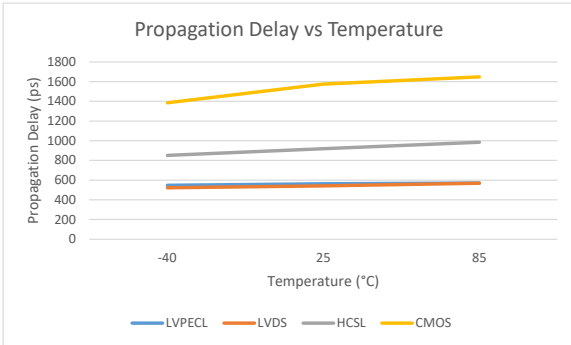
Part-to-Part Skew



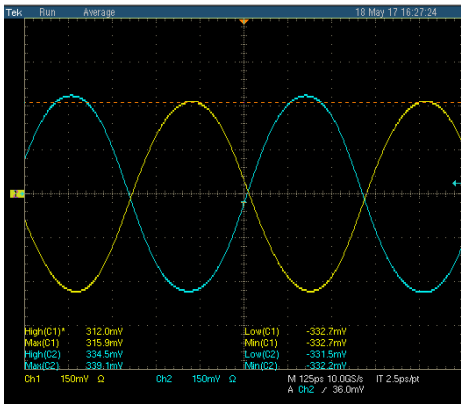
LVPECL/LVDS Output Swing vs Frequency



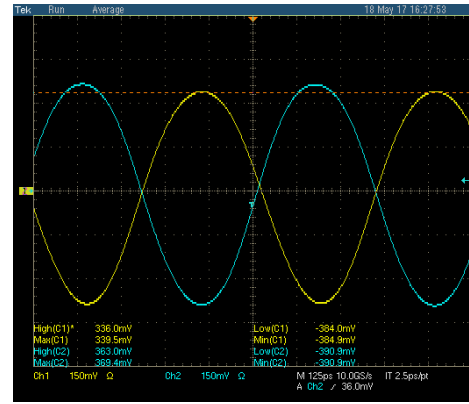
Propagation Delay vs Temperature



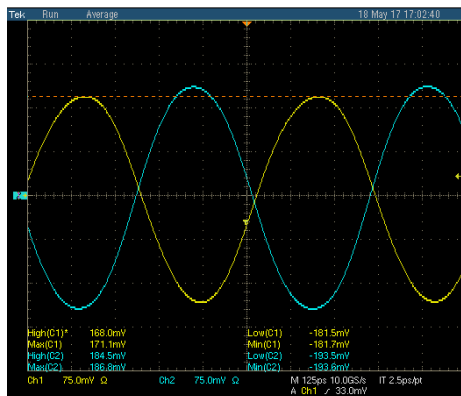
1.5GHz LVPECL/LVDS Waveform



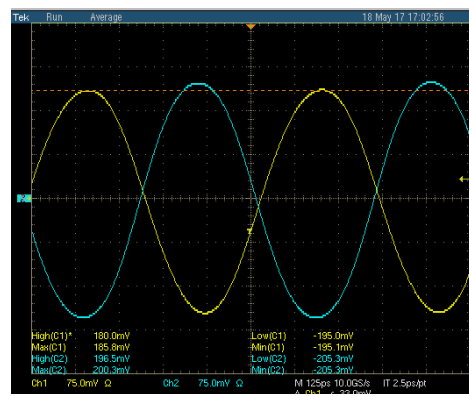
2.5V LVPECL Waveform



3.3V LVPECL Waveform



2.5V LVDS Waveform

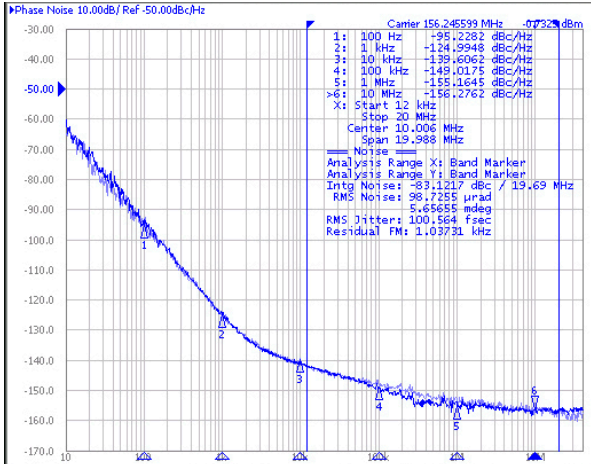


3.3V LVDS Waveform

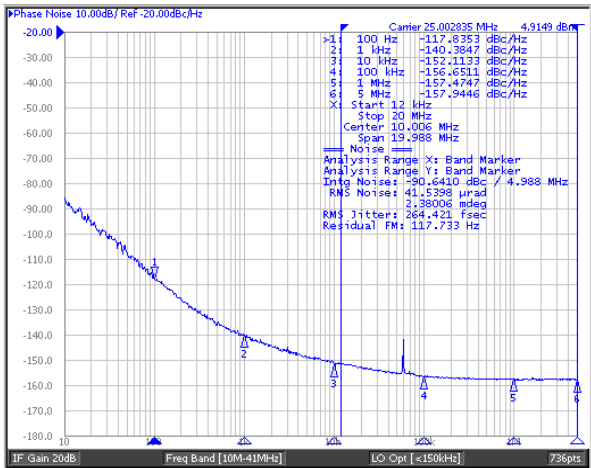
Phase Noise and Additive Jitter

Output Phase Noise (Dark Blue) vs Input Phase Noise (Light Blue)

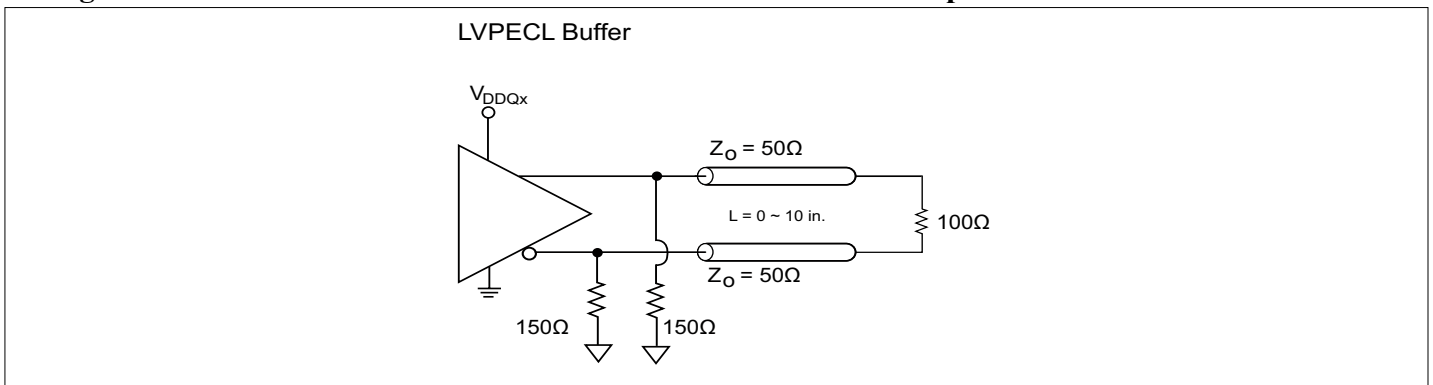
Additive jitter is calculated at 156.25MHz ~ 27fs RMS (12kHz to 20MHz). Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$.



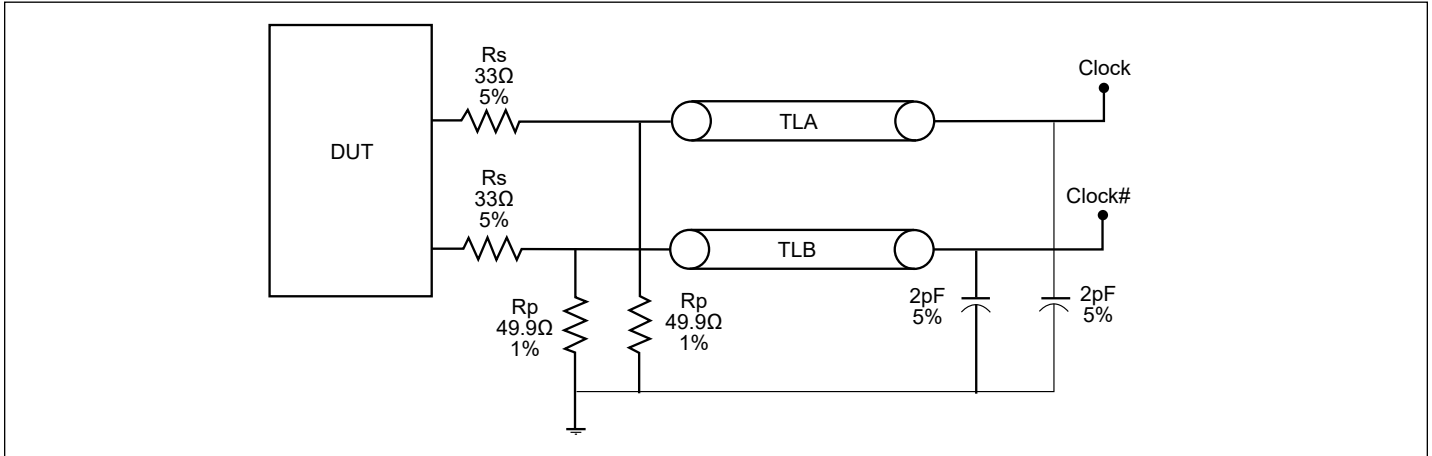
Total Phase Jitter with 25MHz XTAL ~ 264fs RMS (12kHz ~ 20MHz)



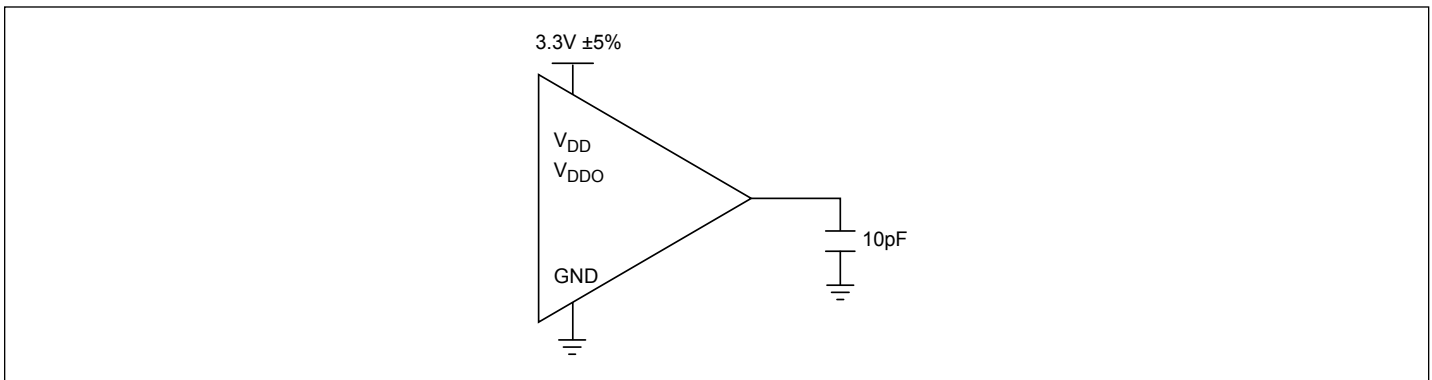
Configuration Test Load Board Termination for LVPECL/LVDS Outputs



Configuration Test Load Board Termination for HCSL Outputs



Configuration Test Load Board Termination for LVCMOS Outputs



Application Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1, R2, and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might require to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V, $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

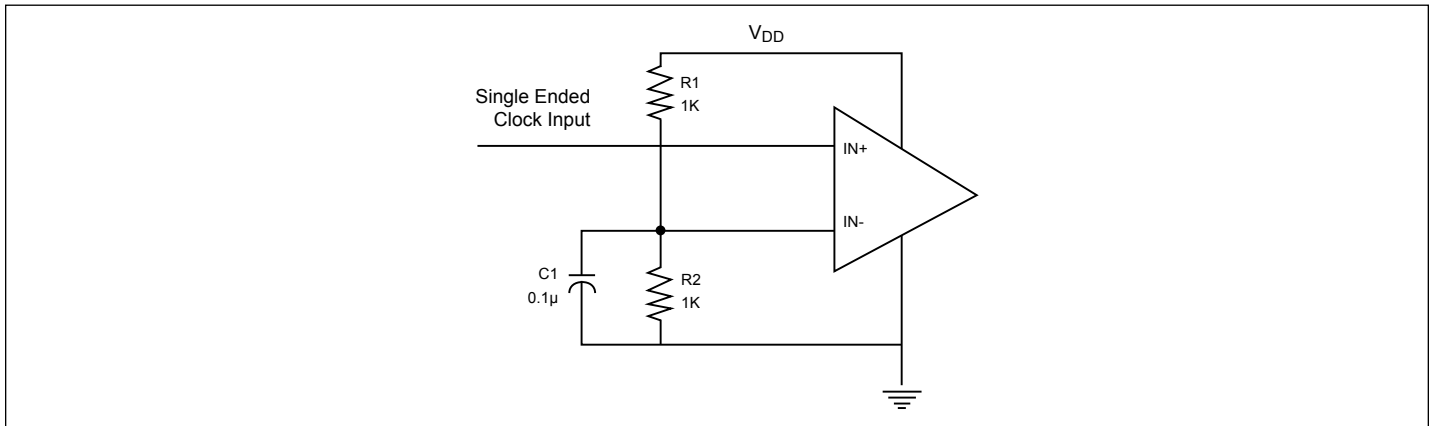
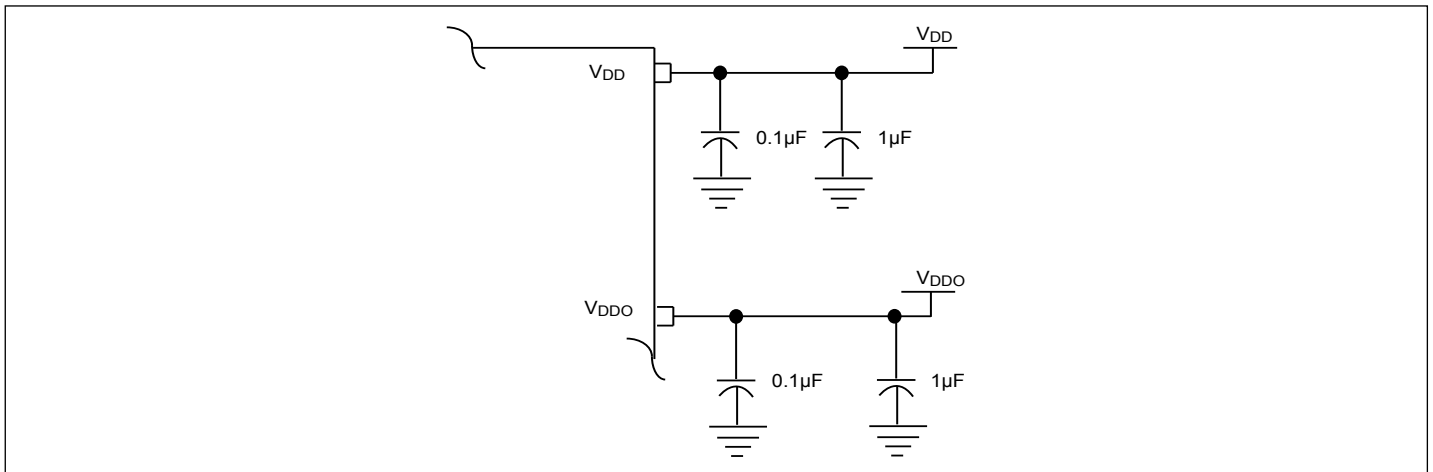


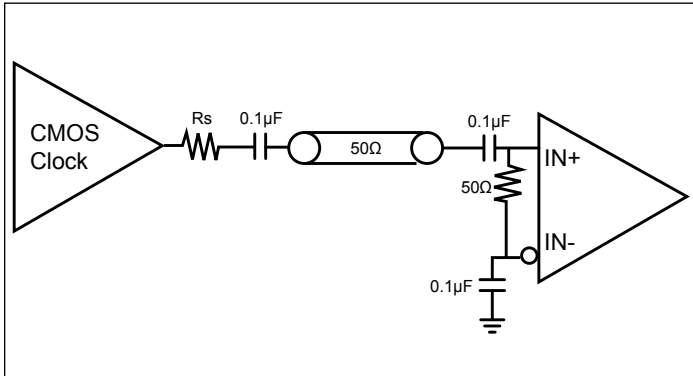
Figure 1. Single-Ended Input to Differential Input Device

Power Supply Filtering Techniques

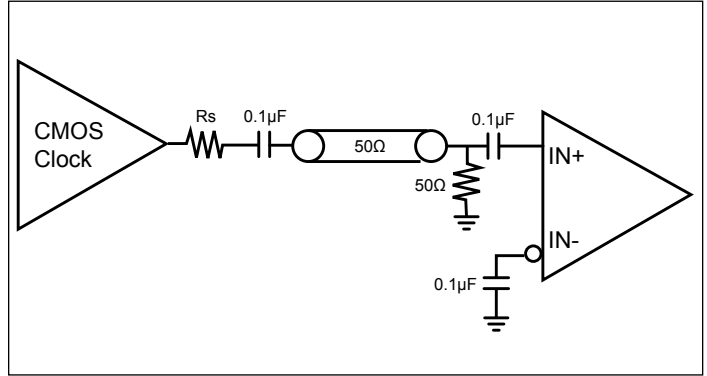
As in any high-speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, and 0.1µF and 1µF bypass capacitors should be used for each pin.



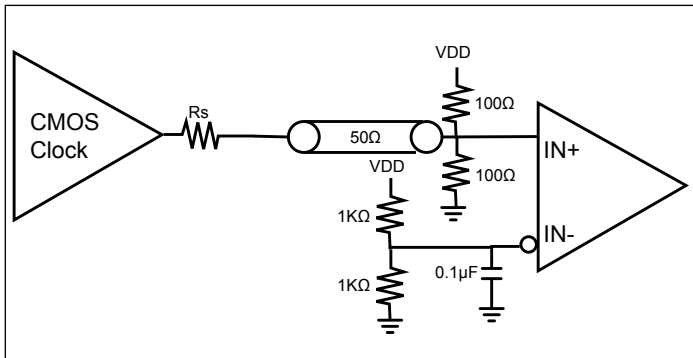
Single-Ended Input, AC Couple



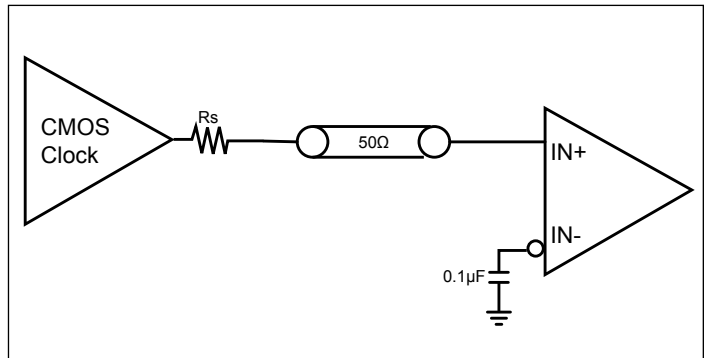
Single-Ended Input, AC Couple



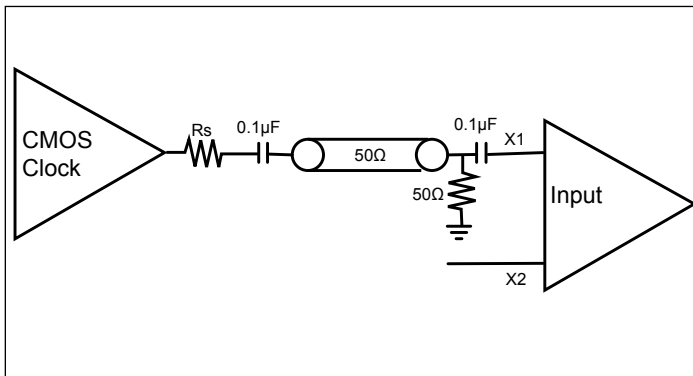
Single-Ended Input, DC Couple



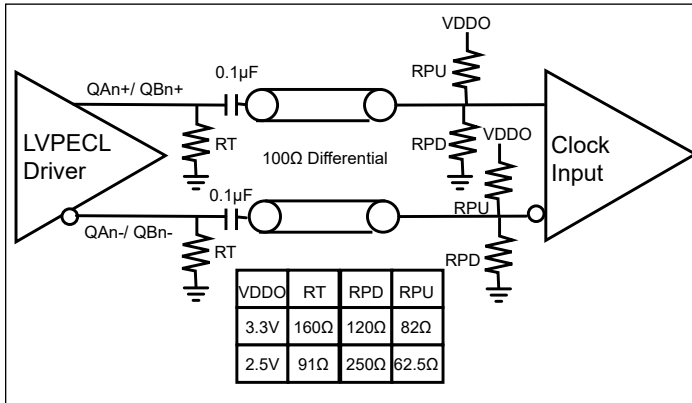
Single-Ended Input, DC Couple



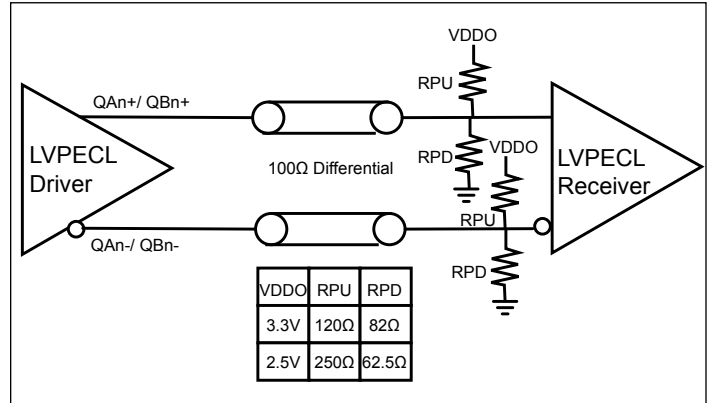
Driving X1 with a Single-Ended Input



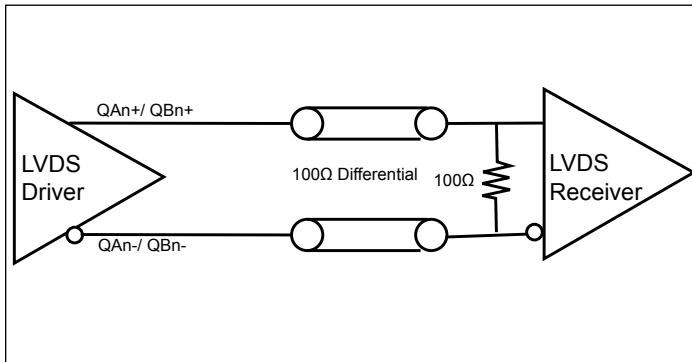
LVPECL, AC Couple, Thevenin Equivalent



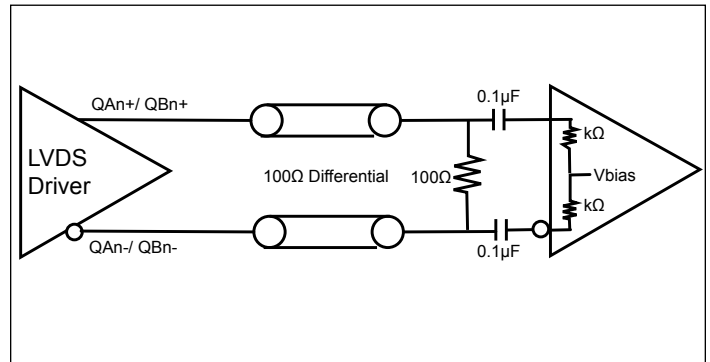
LVPECL, DC Couple, Thevenin Equivalent



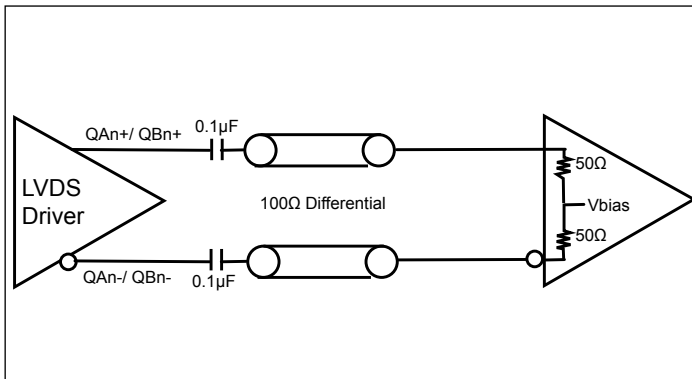
LVDS DC Couple



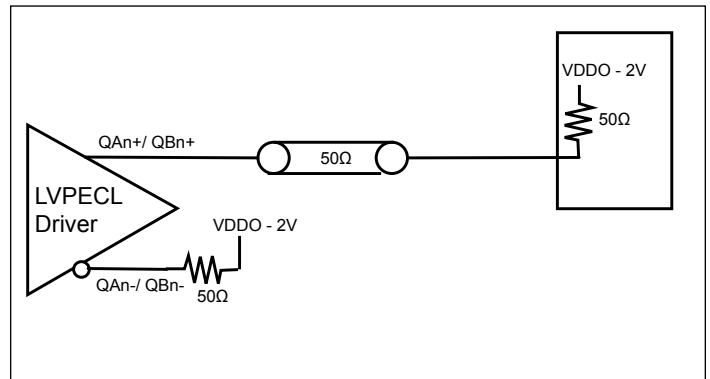
LVDS AC Couple at Load



LVDS AC Couple with Internal Termination

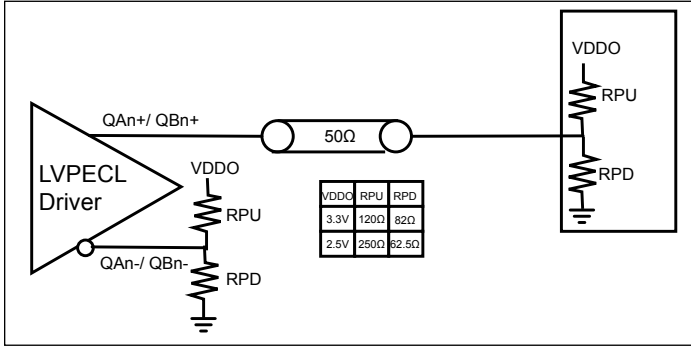


Single-Ended LVPECL, DC Couple

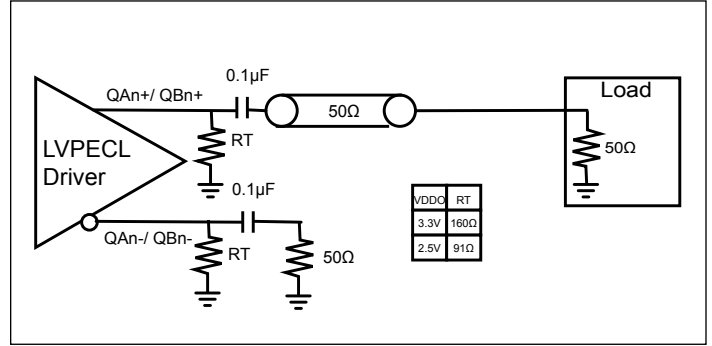


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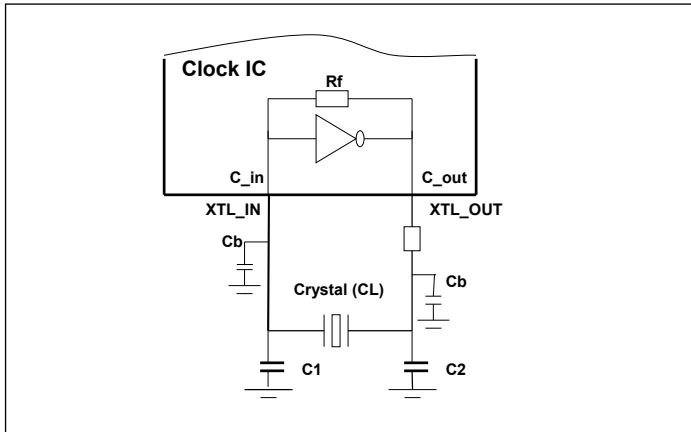
Single-Ended LVPECL, DC Couple, Thevenin Equivalent



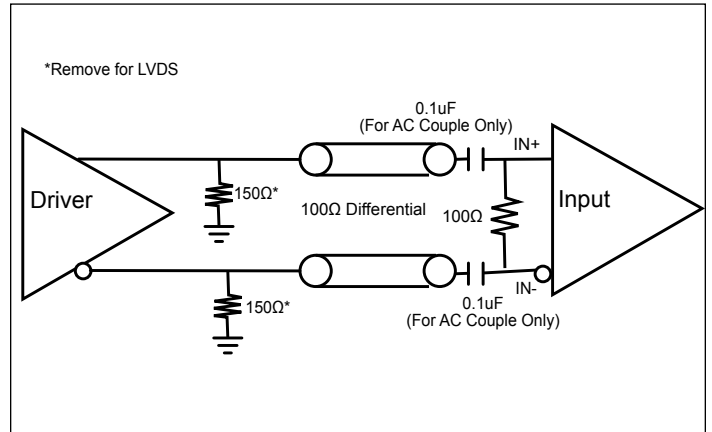
Single-Ended LVPECL, AC Couple, Thevenin Equivalent



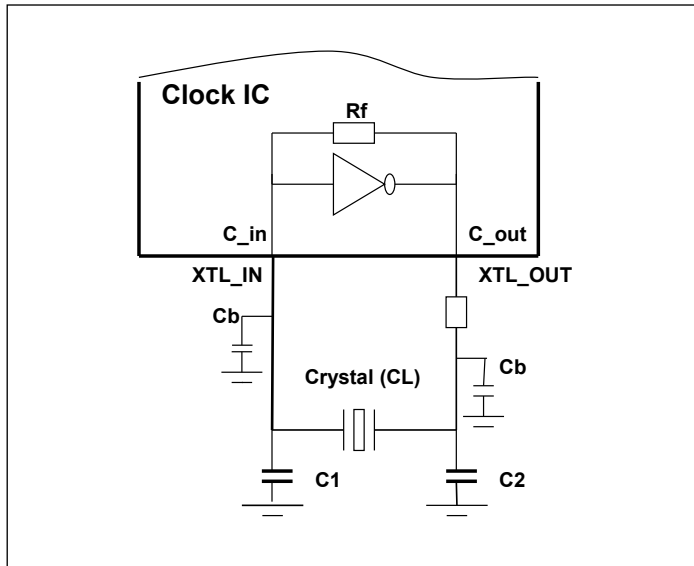
Clock IC Crystal Input Guide



LVPECL/LVDS AC and DC Input



Clock IC Crystal Loading Cap. Design Guide



CL = crystal spec. loading cap.

C_{in/out} = (3pF ~ 5pF) of IC pin cap.

C_b = PCB trace (2pF ~ 4pF)

C_{1,C2} = load cap. of design

R_d = 50Ω to 100Ω drive level limit

Design guide: $C_1 = C_2 = 2 \times CL - (C_b + C_{in/out})$ to meet target $\pm ppm < 20ppm$

Example 1: Select CL = 18pF crystal, $C_1 = C_2 = 2 \times (18pF) - (4pF + 5pF) = 27pF$. Check datasheet.

Example 2: For higher frequency crystal ($>20MHz$), the following formula can be used: $C_1 = C_2 = 2 \times (CL - 6)$. A fine tune of C₁, C₂ can be used for more accurate ppm if necessary.

Thermal Information

Symbol	Description	Condition	—
Θ_{JA}	Junction-to-Ambient Thermal Resistance	Still air	23.65°C/W
Θ_{JC}	Junction-to-Case Thermal Resistance	—	9.1°C/W

Part Marking

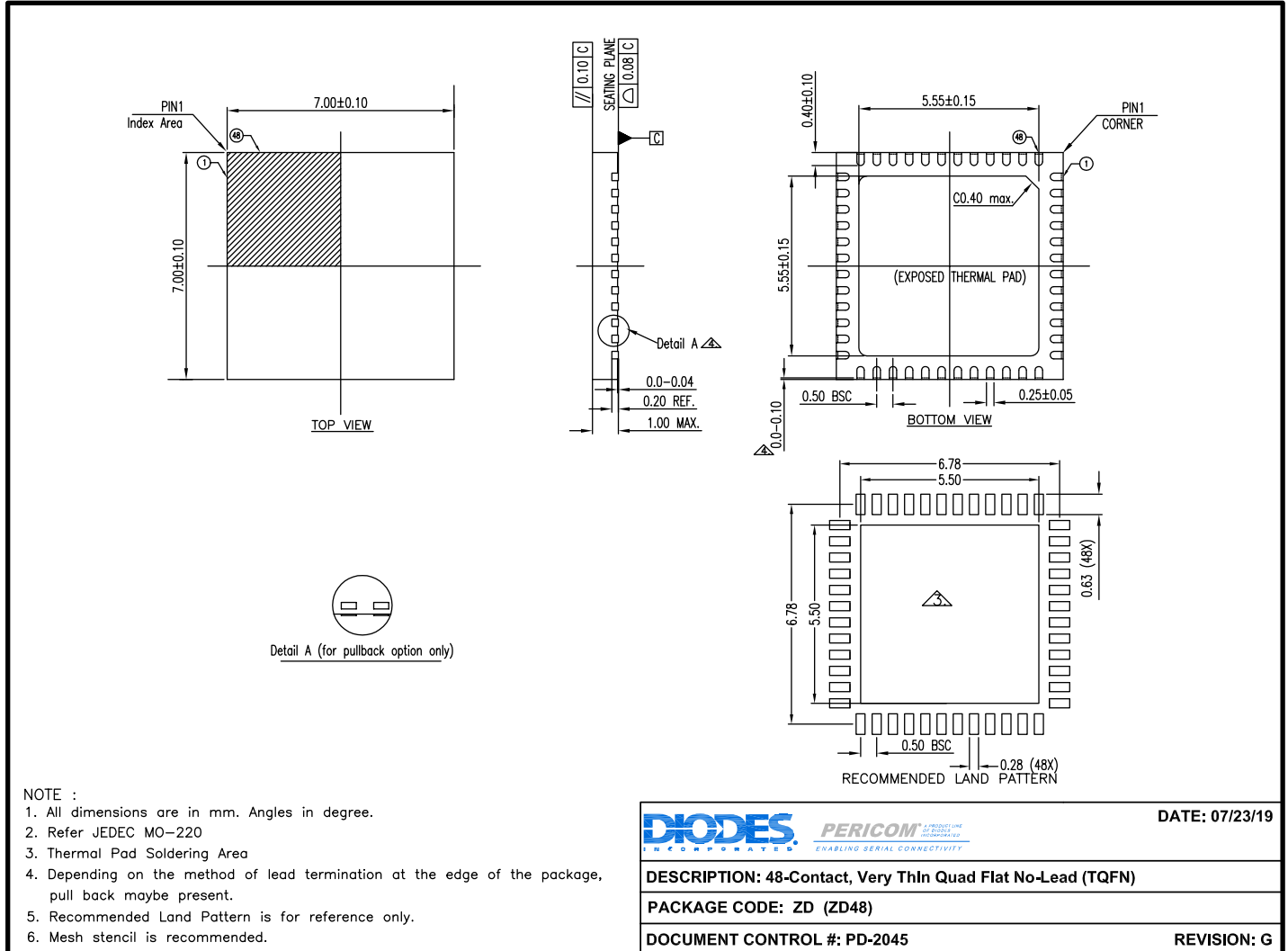
PI6C49S
1510BZDIE
YYWWXX



YY : Year
WW : Workweek
1st X : Assembly Site Code
2nd X : Wafer Site Code

Packaging Mechanical

48-TQFN (ZD)



19-1087

For latest package information:

See <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>.

Ordering Information

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C49S1510BZDIEX	ZD	48-Contact, Very Thin Quad Flat No-Lead (TQFN)	-40°C to 85°C

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- I = Industrial
- E = Pb-free and Green
- X suffix = Tape/Reel

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