A product Line of
Diodes Incorporated

PI3DPX1207B

DP-Alt DP1.4/USB3.1 10Gbps Linear Redriver with Non-Blocking, Latency-Free and built-in Aux Switch

Description

PI3DPX1207B is the DP-Alt 1.4 (Max 10Gbps) Linear Redriver. DP1.4 standard can support 4K2K@120Hz / 25.82 Gbps with 4-channels.

Each of the DP1.4 and USB3.1 Gen2 differential signals can be easily adjustable with equalization, output swing and gain adjustment by either pin or I2C control settings. It can optimize the DP/USB 10Gbps signal performance over a variety of physical mediums by reducing Inter-symbol interference jitters.

Non-blocking linear Redriver can provides 2x better additive jitter performance than the conventional CMOS-based Redriver. Since Linear Redriver does not block the Receiver DFE's adaptive channel controls, it can natively support DisplayPort Transparent LT(Link Training) without any dependency of the DP-Aux channels listener.

Named as "Trace Loss Canceling" technology, and supports the cascading high speed link connections between Host and Device. It means multiple linear Redriver can be placed in the link to work seamlessly to compensate high insertion loss.

The Cascading, Low Jitter and Simplicity of Gain adjustment capabilities to extend signal transmission features are ideal choice for the 8-10Gbps high speed DP Alt signal integrity solutions.

Features

- DP-Alt 4-channel Redriver and DeMux (DP 2-ch and USB 2-ch)
- Latency-free USB Read/Write Transfer rate and DisplayPort Redriver Link Training for variable video frame rate control
- DP1.4 (8.1 Gbps) and USB3.1 Gen 2 (10 Gbps) standard compliant
- Type-C DP/USB mode selection: DP only, USB only, DP/USB split modes
- Natively support Transparent DisplayPort Link training with Non-blocking No-latency Linear ReDriver
- Independently controlled EQ/Gain/Swing signal outputs for DisplayPort and USB modes
- Type-C Plug and Aux Flipping controls through I2C slave pins
- Slave I2C support only. I2C speed up to 1MHz
- Auto power saving circuit
- Single Power Supply: 3.3V

Applications

- Notebook, Desktop and AIO personal computers
- DP-Alt Monitors and Displays
- Active DP-Alt Cables/Adapters

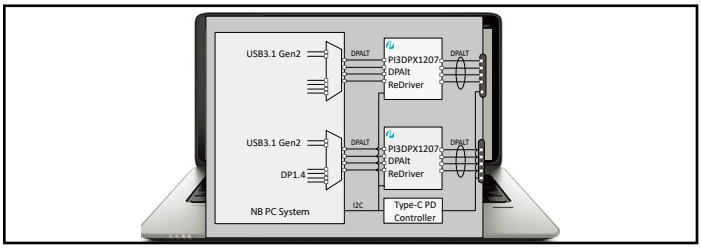


Figure 1-1 Type-C Connector inside PCs

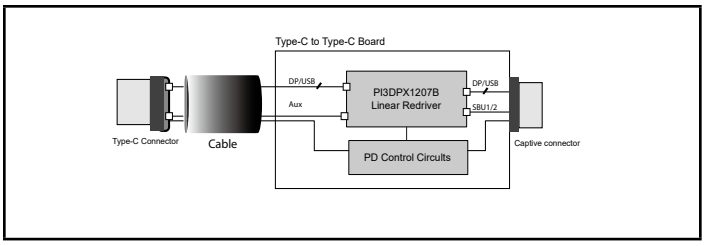


Figure 1-2 DP-Alt to DP Active Cables

Ordering Information

Ordering Number	Package Code	Package Description
PI3DPX1207BZHEX	ZH	42-pin, Very Thin Quad Flat No-Lead (TQFN) (3.5x9mm)

Notes:

1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.

2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/

3. E = Pb-free and Green

4. X suffix = Tape/Reel

2. General Information

2.1 Revision History

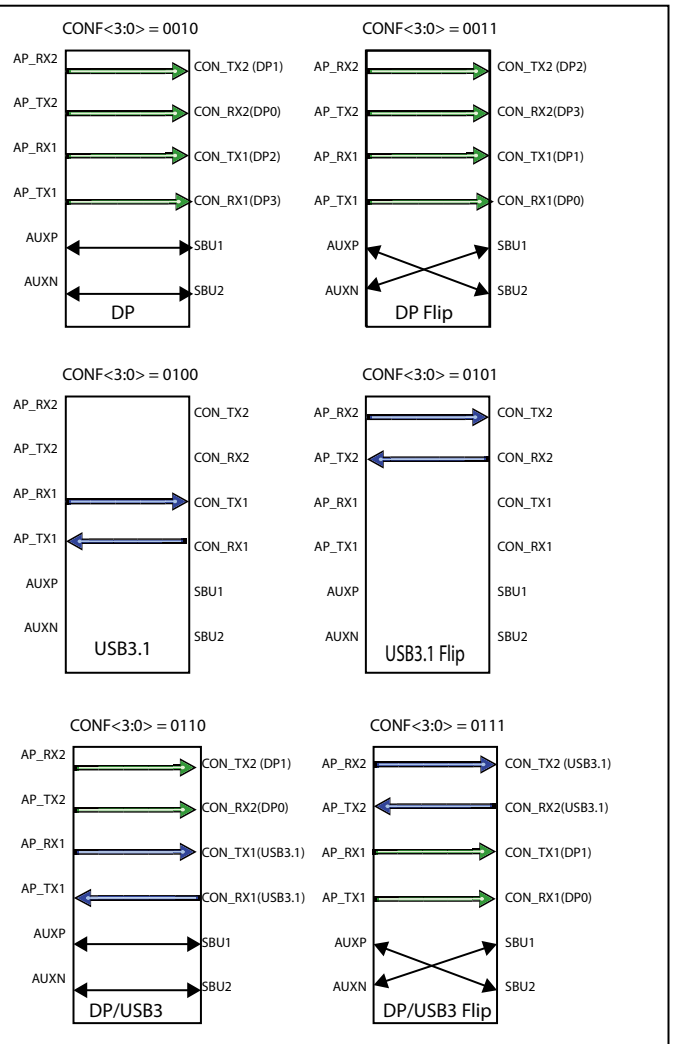
Revision	Description of Changes
Jul 2016	Preliminary Datasheet release.
Aug 2016	Low-power mode, ePad Via, Default register values added.
Oct 2016	Ch 4. $V_{in\text{-}Diff}$ 400mV to Typ changed. Add more clarification in Pin Description and Block Diagram.
Nov 2016	Ch 4. AC/DC electrical parameters and output eye added. Removed Generic mode. Pls contact Diodes for Generic mode application usage.
Dec 2016	Ch 4. Power consumption max added. Ch 5. PCB routing information, CTS report added. Add Sample Errata and disclaimer
Jan 2017	Ch5. DP1.4 CTS test report added.
May 2017	Ch3. 4-bit EQ and FG setting change for high speed Eye signal optimization. Related register spec updated Ch5. USB compliance report added.
Aug 2017	Application reference schematic changed for Aux & SBU1/2 connection. SiGe BiCmos Redriver Jitter performance Benchmark data added in Application session. Power down current max IPD increase 100uA from 66uA. Aux listener features and DP low power D3 mode removed.
Nov 2017	USB3.2, PCIeG3, TMDS modes added for special usage. EC / PD / TCPC programming guide(p51). Due to the Intel's new requirement on the TX impedance when Power-on and Receiver detect phase. All TX 4kOhm impedance changed from 4kOhm to 4.5kOhm (p9, p11,p17)
Mar 2018	AUXSBU2, 18 pin; AUXSBU1, 19 pin Page 46, EN and IN_HPD are reversed.
Apr 2018	Updated 2.3 Diagram
May 2018	Remove Industrial Temp Ordering Information, Remove PI3DPX1207D from Section 2.2; Remove PI3HDX711B and PI3HDX2711B from Section 2.4

2.2 Family Products Comparison

	PI3DPX1207B	PI3DPX1205A
General Features	Type-C DisplayPort Alt Redriver USB / DP Latency-Free	Type-C DisplayPort Alt Active Mux USB / DP Latency-Free
Max Data Rate	10Gbps	10Gbps
Package	42-pin TQFN (3.5x9mm)	40-pin TQFN(4x6mm)
NEXT Crosstalk	Very good, -45dB at 5GHz	Very good, -45dB at 5GHz
Package Pin-out	Place 2 pins space between 10Gbps Data channels TX0/1, RX0/1 to reduce Crosstalk	Place 2 pins space between 10Gbps Data channels TX0/1, RX0/1 to reduce Crosstalk
Control modes	I2C or Pin-mode	I2C mode control
Power supply	3.3V	3.3V

2.3 PI3DPX1207 Redriver Switching Preset modes

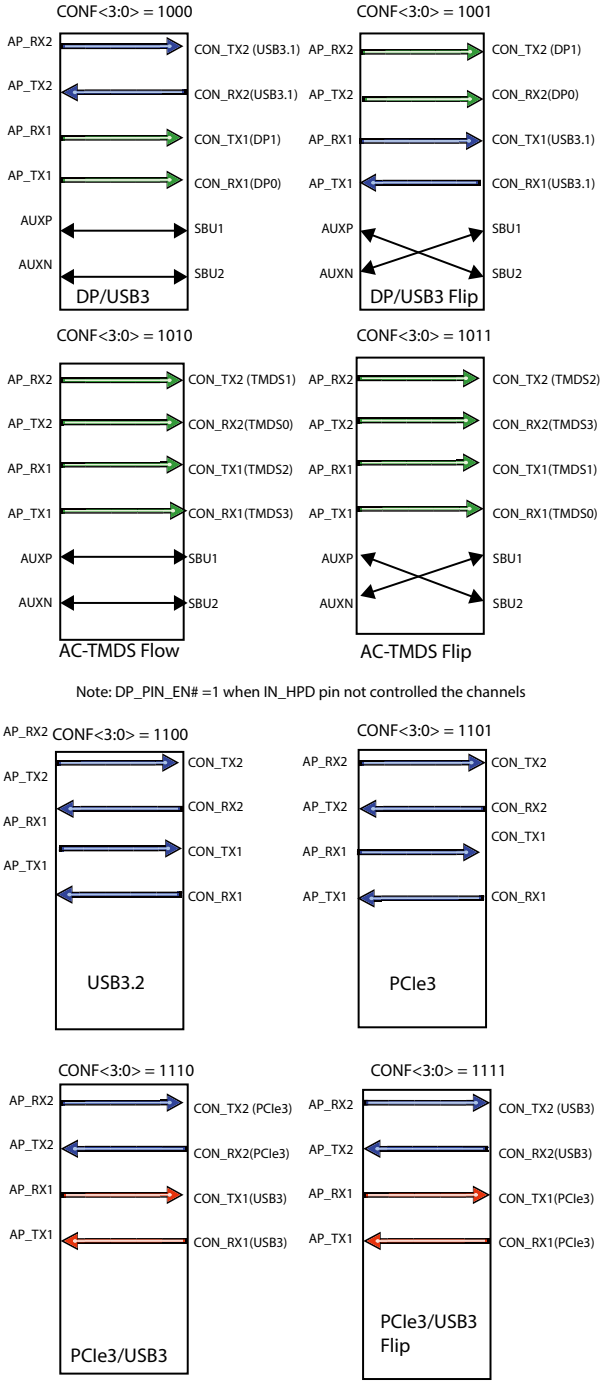
Preset mode with pin-strap (or I2C control)



DP Alt Type-C Redriver

Preset mode supporting with I2C control

CONF<3> bit controlled by I2C. Default CONF<3> = 0



USB3.2 and PCIe3 , AC-TMDS Redriver Modes

2.4 Other Related Products

Part Numbers	Products Description
Redrivers	
PI3DPX1203B	DisplayPort 1.4 Redriver for Source/Sink/Cable Application, Linear-type
PI3HDX1204B1	HDMI 2.0 Redriver (DP++ Level Shifter), High EQ, place near to the source-side, Limiting type
PI3HDX1204E	HDMI 2.0 Linear Redriver (DP++ Level Shifter) , Link transparent, place near to the sink-side
PI3DPX1207B	DisplayPort 1.4 Alt Type-C Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent
PI3DPX1202A	Low Power DisplayPort 1.2 Redriver with built-in AUX Listener, Limiting-type
PI3HDX511F	High EQ HDMI 1.4b Redriver and DP++ Level Shifter for Sink/Source Application, Limiting-type
Active Switches & Splitters	
PI3DPX1205A	DisplayPort 1.4 Alt Type-C Mux Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent
PI3HDX231	HDMI 2.0 3:1 ports Mux Redriver, Linear-type
PI3HDX414	HDMI 1.4b 1:4 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type
PI3HDX412BD	HDMI 1.4b 1:2 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type
PI3HDX621	HDMI 1.4 Redriver 2:1 Active Switch with built-in ARC and Fast Switching support, Limiting-type

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3. Pin Configuration

3.1 Package Pin-out

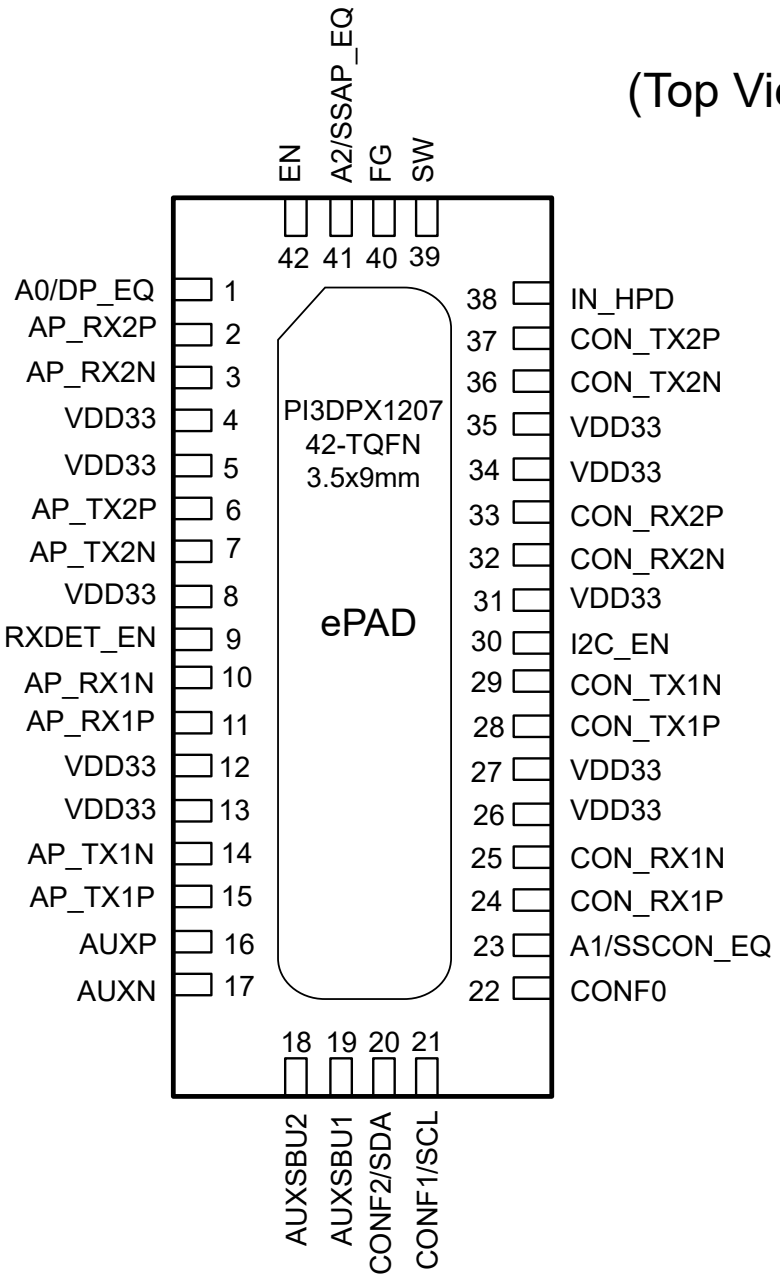


Figure 3-1 42-TQFN package pin-out (PI3DPX1207B)

3.2 Pin Description

Pin Name	Pin #	Type	Description
CON_RX1N/P	25,24	I/O	Type-C receptacle RX/TX Channel CML input/output With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND. With selectable output termination between 50Ω to VbiasTx, 4.5k to VbiasTx or Hi-Z
CON_RX2P/N	33,32	I/O	Type-C receptacle RX/TX Channel CML input/output With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND. With selectable output termination between 50Ω to VbiasTx, 4.5k to VbiasTx or Hi-Z
CON_TX2P/N	37,36	O	CML output terminals. With selectable output termination between 50Ω to VbiasTx, 4.5kΩ to VbiasTx or Hi-Z
CON_TX1N/P	29,28	O	CML output terminals. With selectable output termination between 50Ω to VbiasTx, 4.5kΩ to VbiasTx or Hi-Z
AP_RX2P/N	2,3	I	CML input terminals. With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND.
AP_RX1N/P	10,11	I	CML input terminals. With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND.
AP_TX2P/N	6,7	I/O	Type-C receptacle RX/TX Channel CML input/output terminals. With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND. With selectable output termination between 50Ω to VbiasTx, 4.5k to VbiasTx or Hi-Z
AP_TX1N/P	14,15	I/O	Type-C receptacle RX/TX Channel CML input/output terminals. With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND. With selectable output termination between 50Ω to VbiasTx, 4.5k to VbiasTx or Hi-Z
A0/DP_EQ	1	I	For pin control mode (I2C_EN=Low) DP Application processor side: The equalization selection. 4-level input pins. With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
			For I2C control mode (I2C_EN=High). I2C address select. 2-level input pins. Internal 200kΩ pull-down resistor.
RXDET_EN	9	I	Receiver detect enable mode. With internal 300kΩ pull-up resistor. “Low”: Disabled “High”: Enabled (Default)
AUXP/N	16, 17	I/O	Host AP/UFP-side DisplayPort Aux Channel, connected to Source
AUXSBU2 AUXSBU1	18, 19	I/O	Connector/DFP Low Speed Signal Port. Side band use

Pin Name	Pin #	Type	Description
CONF2/SDA	20	I/O	For Pin control mode with internal 300kΩ pull-down resistor (I2C_EN=Low). CONF2 is the selection pin for the channel mode assignment and flip control
			For I2C control mode (I2C_EN=High). SDA is I2C control bus data. Open drain structure.
CONF1/SCL	21	I	For Pin control mode with internal 300kΩ pull-down resistor (I2C_EN=Low). CONF1 is the selection pin for the channel mode assignment and flip control
			For I2C control mode (I2C_EN=High) SCL is I2C control clock. Open drain structure.
CONF0	22	I	For Pin control mode (I2C_EN=Low) CONF0 is the selection pin for the channel mode assignment and flip control. 300kΩ pull-down resistor.
A1/SSCON_EQ	23	I	For pin control mode (I2C_EN=Low) USB Type-C connector side. The equalization selection. 4-level input pins. With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
			For I2C control mode (I2C_EN=High) The I2C address select. 2-level input pins. With internal 200kΩ pull-down resistor.
I2C_EN	30	I	I2C enable control. With internal 300kΩ pull-up resistor. “Low”: Pin control is selected “High”: I2C control is selected (Default)
IN_HPD	38	I	Hot plug detection from Sink. With internal 300kΩ pull-down resistor.
SW	39	I	For pin control mode (I2C_EN=Low) DP Type-C Connector side: The -1dB linear swing selection. 2-level input pins. With internal 300kΩ pull-up resistor.
FG	40	I	For pin control mode (I2C_EN=Low) The flat selection. 4-level input pins. With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
A2/SSAP_EQ	41	I	For pin control mode (I2C_EN=Low) USB Application Process side: The equalization selection. 4-level input pins. With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
			For I2C control mode (I2C_EN=High) The I2C address select. 2-level input pins. With internal 200kΩ pull-down resistor.
EN	42	I	Chip Enable. With internal 300kΩ pull-up resistor. “Low”: Chip Power Down “High”: Normal Operation (Default)
VDD33	4,5 8, 12 13, 26 27,31 34,35	P	3.3V Power Supply
ePAD	ePAD	G	ePAD for the Ground

4. Functional Description

4.1 Product Feature Details

General Features

- ➔ DP-Alt HBR3 8.1Gbps mode and USB3.1 10Gbps Type-C application
- ➔ Flexible DP-Alt mode switching between USB3.1 Gen2 and DP 8.1Gbps
- ➔ Ultra Low standby power with auto power saving for the DisplayPort and USB mode
- ➔ Selectable adjustment of receiver Equalization, Flat gain, -1dB compression linear output swing
- ➔ Built-in control logic for Type-C plug/unplug normal and flipping orientations
- ➔ Active Linear ReDriving for signal integrity
- ➔ Except the EN pin, I2C_EN, I2C address pins, IN_HPD and I2C I/O pins, all other pin setting will be ignored in the I2C mode.
- ➔ Slave I2C only. I2C speed up to 1MHz
- ➔ The I2C I/O buffer supports the 1.8V/3.3V signal condition
- ➔ IN_HPD could be selected as active high or active low by I2C mode (byte4 [1])
- ➔ Single power supply 3.3±0.3V

DisplayPort 1.4

- ➔ DP LT-transparent through linear Redriver design
- ➔ Hot Plug Detect

USB 3.1 Gen 2

- ➔ Selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND.
- ➔ Selectable output termination between 50Ω to VbiasTx, 4.5kΩ to VbiasTx or Hi-Z with receiver termination detection.
- ➔ Possible operation modes: PD, Unplug, deep slumber mode, slumber mode and active mode.
- ➔ Receives and transmits the signal in unplug, deep slumber mode and active mode.
- ➔ Active mode: The channel is always ready to transmit. No Ton/Toff due to the signal detector in this mode.
- ➔ Slumber mode, Deep slumber mode and Unplug mode: The channel is partially/fully off due to the power saving. Signal detector is monitoring the input signal actively. If the input signal is detected, the channel will switch to the active mode. ON-time is operation mode selection dependent.

4.2 Functional Block Diagram

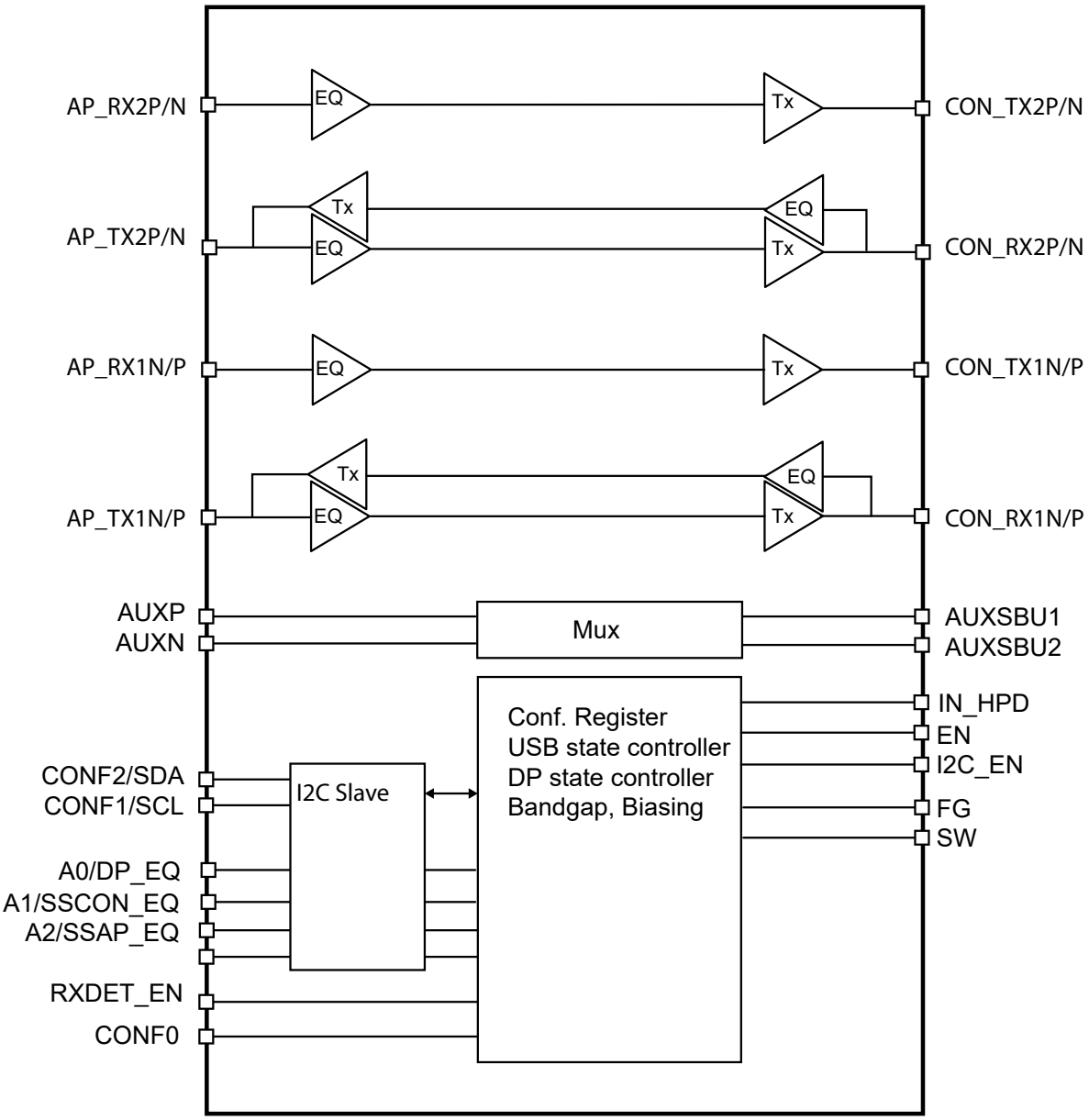


Figure 4-1 PI3DPX1207B DP-Alt ReDriver block diagram

4.3 The Operating mode control

4.3.1 Preset DP-Alt Channel mapping control

CONF	Modes	AP_RX2	AP_TX2	AP_RX1	AP_TX1	AUXP	AUXN	IN HPD/ AUX CMD
with CONF0/1/2 pins or CONF[3:0] I2C register bits control								
0000	Safe State	X	X	X	X	X	X	X
0001	Safe State	X	X	X	X	X	X	X
0010	4 lane DP1.4 + AUX	CON_ TX2 (DP1)	CON_ RX2 (DP0)	CON_ TX1 (DP2)	CON_ RX1 (DP3)	SBU1	SBU2	All CON response
0011	Flip mode: 4 lane DP1.4 + AUX	CON_ TX2 (DP2)	CON_ RX2 (DP3)	CON_ TX1 (DP1)	CON_ RX1 (DP0)	SBU2	SBU1	All CON response
0100	1 lane USB3.x (AP_CH1)	X	X	CON_ TX1	CON_ RX1	X	X	X
0101	Flip mode: 1 lane USB3.x (AP_CH2)	CON_ TX2	CON_ RX2	X	X	X	X	X
0110	USB3 (AP_CH1) + 2 lane DP1.4(AP_CH2) + AUX	CON_ TX2 (DP1)	CON_ RX2 (DP0)	CON_ TX1 (USB3)	CON_ RX1 (USB3)	SBU1	SBU2	CON2 response only
0111	Flip mode: USB3 (AP_CH1) + 2 lane DP1.4 (AP_CH2) + AUX	CON_ TX2 (USB3)	CON_ RX2 (USB3)	CON_ TX1 (DP1)	CON_ RX1 (DP0)	SBU2	SBU1	CON1 response only
with CONF[3:0] i2C register bits control								
1000	USB3 (AP_CH2) + 2 lane DP1.4 (AP_CH1) + AUX	CON_TX-2(USB3)	CON_ RX-2(USB3)	CON_ TX1/DP1	CON_ RX1/ DP0	SBU1	SBU2	CON1 response only
1001	USB3 (AP_CH1) + 2 lane DP1.4 (AP_CH2) +AUX (flipped)	CON_ TX2/ DP1	CON_ RX2/ DP0	CON_ TX-1(USB3)	CON_ RX-1(USB3)	SBU2	SBU1	CON2 response only
1010	4 lane TMDS mode with AUX channel for HDMI DDC	CON_ TX2	CON_ RX2	CON_ TX1	CON_ RX1	SBU1	SBU2	IN_HPD Only[3)]
1011	4 lane TMDS mode flipped with AUX channel for HDMI DDC	CON_ TX2	CON_ RX2	CON_ TX1	CON_ RX1	SBU2	SBU1	IN_HPD Only[3)]
1100	2 lane USB3.x	CON_ TX2	CON_ RX2	CON_ TX1	CON_ RX1	X	X	
1101	2 lane PCIe3	CON_ TX2	CON_ RX2	CON_ TX1	CON_ RX1	X	X	
1110	USB3 (AP_CH1) + PCIe3 (AP_CH2)	CON_TX-2(PCIe3)	CON_ RX2(P-CIe3)	CON_ TX-1(USB3)	CON_ RX-1(USB3)	X	X	X

CONF	Modes	AP_RX2	AP_TX2	AP_RX1	AP_TX1	AUXP	AUXN	IN HPD/ AUX CMD
1111	USB3 (AP_CH2) + PCIe3 (AP_CH1)	CON_ TX2(USB3)	CON_ RX2(USB3)	CON_ TX1(P-CIe3)	CON_ RX1(P-CIe3)	X	X	X

Note:
1) CONF[2:0] pins and CONF[3:0] (I2C 0x3[7:4]) with mode description. Both Pin and I2C mode can access below setting
2) The high speed channels don't do any flip action. Only the AUX channel is flipped.
3) Set the I2C reg byte12 bit2 DP_HPD_PIN_EN#=1 if the target channel is not controlled by the IN_HPD pin.

4.3.2 IN_HPD control

Table 4-1. DP_HPD_PIN_EN# register can enable the IN_HPD control

I2C Byte 0x12[2]: DP_HPD_PIN_EN#	Pin IN_HPD Status (Hot plug detection input from Sink)	DP output status
1	x	Enabled
0	0	Disabled
0	1	Enabled

4.3.3 IN_HPD assert and De-assert De-bounce timer

IN_HPD transition	De-bounce timer timeout	Notes
Assert: Low -> High	~0s	
De-assert: High -> Low	~ 325ms typ	Any Low-> High transition within timeout will reset the timer.

4.4 EQ/FG/SW controls

Table 4-2. Equalization Setting

EQ pin	EQ3	EQ2	EQ1	EQ0	@ 2.5GHz	@ 3GHz	@ 4GHz	@ 5GHz	@ 6GHz	Note
L	0	0	0	0	3.2	3.8	4.9	5.7	6.1	I2C Default
	0	0	0	1	3.5	4.2	5.5	6.4	6.9	
	0	0	1	0	3.8	4.7	6.1	7.1	7.7	
	0	0	1	1	4.2	5.1	6.6	7.7	8.4	
	0	1	0	0	4.7	5.6	7.2	8.3	9	
R	0	1	0	1	5	6	7.7	8.9	9.6	
	0	1	1	0	5.4	6.4	8.2	9.4	10.1	
	0	1	1	1	5.7	6.8	8.6	9.9	10.6	
	1	0	0	0	6.2	7.3	9	10.2	11	
	1	0	0	1	6.5	7.6	9.4	10.7	11.4	
F	1	0	1	0	6.8	7.9	9.8	11.1	11.8	Pin Default
	1	0	1	1	7	8.2	10.1	11.4	12.1	
	1	1	0	0	7.4	8.5	10.4	11.7	12.4	
	1	1	0	1	7.6	8.8	10.7	12	12.7	
	1	1	1	0	7.8	9.1	11	12.3	13	
H	1	1	1	1	8.1	9.3	11.3	12.6	13.3	

4.4.1 Flat Gain Setting

Table 4-3. FG 4-level input selection pins for the DC gain

FG pin	FG[1:0]	Flat Gain Settings V/V
R (Tie Rext to GND)	00	-1.5 dB
F (Leave Open)	01	0 dB (Default)
L (Tie 0Ω to GND)	10	+1 dB
H (Tie 0Ω to VDD)	11	+2.5 dB

4.4.2 Output -1 dB Compression point output swing setting

Table 4-4. SW selection pins for the -1dB compression point output swing setting

SW pin	USB	DP
0	900mVppd	1100mVppd
1	1000mVppd	1200mVppd (Default)

4.4.3 I2C mode: 0x5[1:0] to 0x8[1:0]

CONx_SW[1:0]	Output Linear Swing Settings
00	900mVppd
01	1000mVppd
10	1100mVppd
11	1200mVppd (Default)

4.4.4 Chip Enable Setting:

Table 4-5. Channel EN enable pin

EN	Channel Enable Setting
0	Disabled
1	Enabled (Default)

4.5 USB mode

In the low power mode, the signal detector will still be monitoring the input channel. If a channel is in low power mode and the input signal is detected, the corresponding channel will wake-up immediately. If a channel is in low power mode and the signal detector is idle longer than 6ms, the receiver detection loop will be active again. If load is not detected, then the Channel will move to Device Unplug Mode and monitor the load continuously. If load is detected, it will return to Low Power Mode and receiver detection will be active again per 6ms.

Table 4-6. The I/O termination resistance under different conditions

Symbol	Parameter	Resistance	Units
RX terminal			
Rin-pd	Input resistance at power down mode	67k to GND	Ω
Rin-U0	Input resistance at U0 condition	50 to VDD	Ω
Rin-U1	Input resistance inU1 (1)	50 to VDD	Ω
Rin-U2/U3	Input resistance in U2/U3 (1)	50 to VDD	Ω
Rin-RXDet	Input resistance in RXDET (1)	67k to VbiasRx	Ω
TX terminal			
Rout-pd	Output resistance at power down mode	HIZ	Ω
Rout-U0	Output resistance at U0 condition	50 to VbiasTx1	Ω
Rout-U1	Output resistance in U1 mode (1)	4.5k to VbiadTx1	Ω
Rout-U2/U3	Output resistance in U2/U3 mode (1)	4.5k to VbiasTx2	Ω
Rout-RXDet	Output resistance in RXDET mode (1)	4.5k to VbiasTx2	Ω

Notes: (1) The value of Rin-RxDet will be updated only after the receiver evaluation has been done. Thus, the value can be 50Ω or 67kΩ pull-low.

4.6 DisplayPort mode

By default, all channels will go to active modes if IN_HPD = 1. The ON/OFF of each DP channel is controlled by the Aux lane count.

4.6.1 DisplayPort Main Link

The electrical sub-block of a DP Main-Link consists of up to four differential pairs. The DP TX drives doubly terminated, AC-coupled differential pairs, as shown in Figure 3-34 in a manner compliant with the Main-Link Transmitter electrical specification.

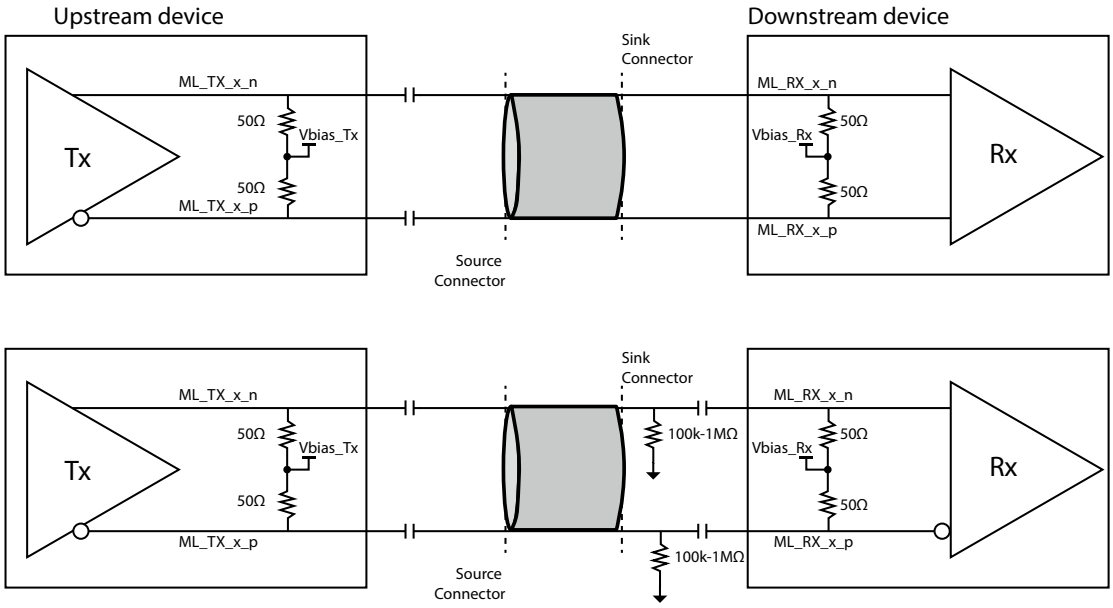


Figure 4-2 DisplayPort Main Link Connection Diagram

Table 4-7. DP Low Power Mode Description

PM_State	Mode	Description
1	Active mode	Data transfer (normal operation); The AUX monitor is actively monitoring for Link Training unless it is disabled through I2C interface. At power-up all Main Link outputs are Enabled by default. AUX Link Training is necessary to overwrite the DPCD registers to Enable/Disable Main Link outputs.
2	Standby mode	Low power consumption (I2C interface is active; AUX monitor is inactive); Main Link outputs are disabled; the Sink device has de-asserted HPD
3	Power down mode(OFF)	Lowest power consumption (EN = 0); all outputs are high-impedance; I2C interface is turned off, all inputs are ignored, I2C register is reset and AUX DPCD is reset:

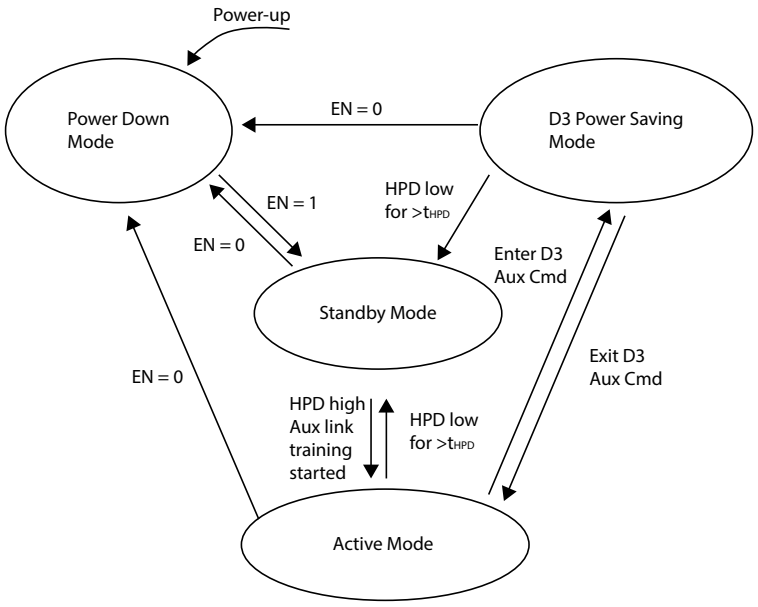


Figure 4-3 DisplayPort Operation mode

4.6.2 DisplayPort Aux Channel

The AUX CH of DP is a half-duplex, bidirectional channel. The DP device with DPTX such as a Source device is the master of the AUX CH (called AUX CH Requester), while the device with DPRX such as a Sink device is the slave (AUX CH Replier). As the master, the Source device must initiate a Request Transaction, to which the Sink device responds with a Reply Transaction.

The system design of a DFP_D on a USB Type-C connector connected to a UFP_D on a USB Type-C connector using a USB Type-C to USB Type-C Cable. The 2MΩ pull-down resistors on SBU1 and SBU2 are representative of the leakage of ESD and EMI/RFI components including termination to ensure no floating nodes, and are intended to show compliance with SBU Termination in USB Type-C r1.1. The plug orientation switch may be replaced by AUX polarity inversion logic in the DisplayPort transmitter or receiver, controlled by the plug orientation detection mechanism associated with the USB Type-C Receptacle. Note: The 3.3V levels in the Adaptors are derived from VCONN because not all DisplayPort UFP_D devices provide DP_PWR.

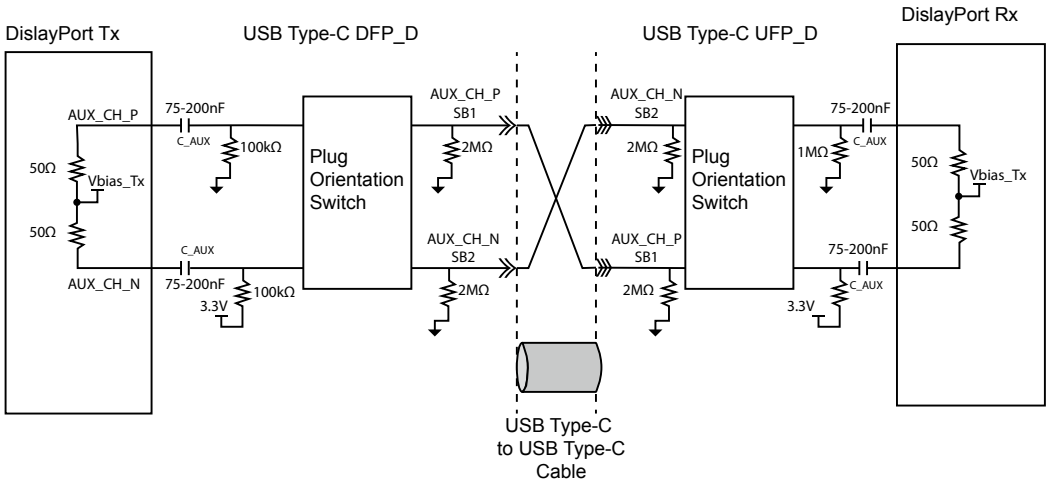


Figure 4-4 AUX Signaling Using USB Type-C to USB Type-C Cables

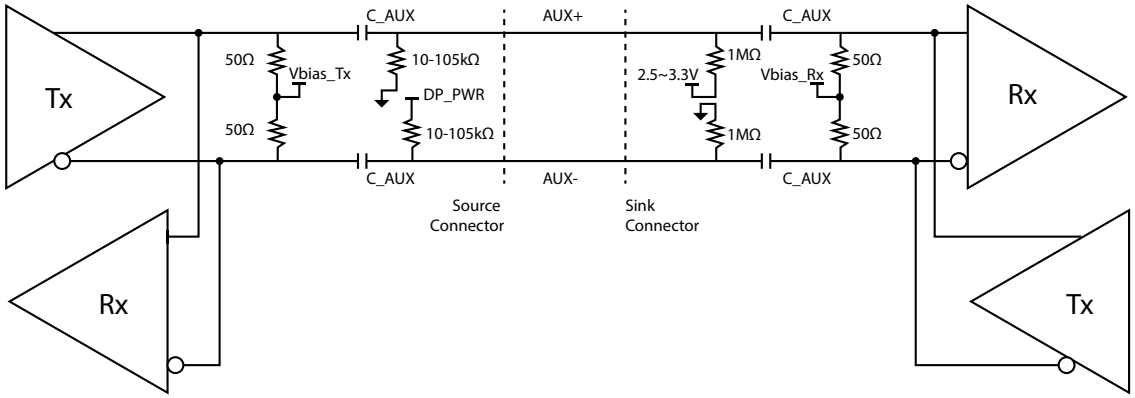


Figure 4-5 DisplayPort Aux Channel Connection

4.7 I2C Programming

4.7.1 I2C Address

Table 4-8. I2C Address bits

	Register Bits							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Slave address (First byte is slave address)	1	0	1	0	A2	A1	A0	0/1 (W/R)

Note: A0, A1, A2 are pin-strapping selectable

4.7.2 I2C Feature Summary

- I2C interface operates as a slave device.
- The device supports Bulk read/write
- Support operating speed up to 1MHz
- Supported 7-bit addressing
- The data byte format is 8-bit bytes with the most significant bit (MSB) first.
- Will never hold the clock line SCL LOW to force the master into a wait state.
- No response when the data on common bus is matched to the device address.
- When I2C_EN=0, all registers become RO byte.
- If I2C master want read/write invalid register, i.e. the I2C slave just write/read from a dummy RO register with FF by default.

4.7.3 Acknowledge

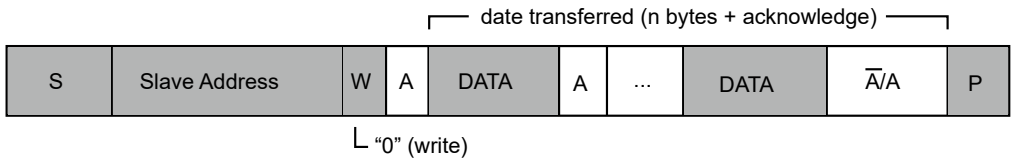
Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, it will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I2C Data Transfer diagram. It will generate an acknowledge after each byte has been received.

4.7.4 Data Transfer

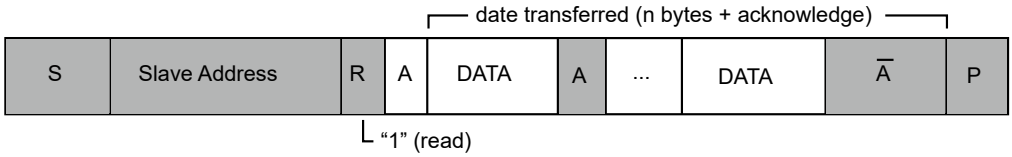
A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, it will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. Data is transferred with the most significant bit (MSB) first. It will never hold the clock line SCL LOW to force the master into a wait state.

4.7.5 Start & Stop Condition

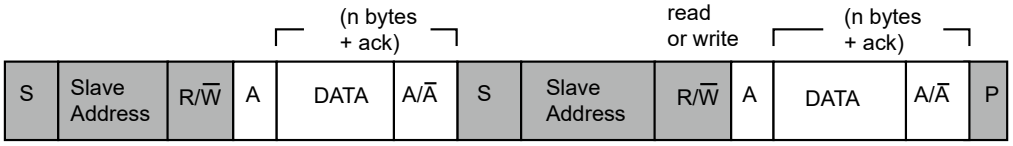
A HIGH to LOW transition on the SDA line, while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below



A master-transmitter addressing a slave receiver with a 7-bit address. The transfer direction is not changed



A master reads a slave immediately after the first byte.



Combined format

Figure 4-6 Block read/write protocol

4.8 Detail Programming Registers

4.8.1 Register Default Summary

Table 4-9. Programming Register Map

Byte	Read after power up	CONF[3:0]															
		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h	03h
1	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h	11h
2	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h	20h
3	00h	00h	10h	20h	30h	40h	50h	60h	70h	80h	90h	A0h	B0h	C0h	D0h	E0h	F0h
4	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh	0Dh
5	03h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h
6	03h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h
7	03h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h
8	03h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h	07h
9	60h	60h	62h	68h	67h	00h	0Eh	48h	27h	21h	4Eh	60h	63h	00h	00h	00h	00h
10	FCh	FCh	FCh	FCh	FCh	42h	42h	FCh	42h	42h	FCh	FEh	Feh	42h	7Fh	7Eh	42h
11	FCh	FCh	FCh	FCh	FCh	42h	42h	42h	FCh	FCh	42H	FEh	Feh	42h	7Fh	42h	7Eh
12	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h	58h
13	00h	00h	00h	FFh	FFh	00h	00h	F0h	0Fh	0Fh	F0h	FFh	FFh	00h	00h	00h	00h
14	FFh	FFh	FFh	00h	00h	33h	CCh	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
15	C8h	C8h	C8h	C8h	C8h	C8h	C8h	59h	C8h	C8h	C8h	C8h	C8h	C8h	C8h	C8h	C8h
16	DCh	DCh	DCh	5Ch	5Ch	D3h	D3h	DCh	56h	56h	59h	5Ch	5Ch	D3h	D3h	D3h	D3h
17	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h	14h
18	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h	04h
19 ~30	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
31	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h

4.8.2 BYTE 0 (Revision and Vendor ID Register)

Bit	Type	Power up condition	Control affected	Comment
7	RO	0	Revision ID	Rev# = 0000
6	RO	0		
5	RO	0		
4	RO	0		
3	RO	0	Vendor ID	Pericom
2	RO	0		
1	RO	1		
0	RO	1		

4.8.3 BYTE 1 (Device Type/Device ID register)

Bit	Type	Power up condition	Control affected	Comment
7	RO	0	Device Type	Device Type Active Mux = 0001
6	RO	0		
5	RO	0		
4	RO	1		
3	RO	0	Device ID	Device ID PI3DPX1207 = 0001
2	RO	0		
1	RO	0		
0	RO	1		

4.8.4 BYTE 2 (Byte count register)

Bit	Type	Power up condition	Control affected	Comment
7	RO	0	Register Byte count	I2C byte count = 32 bytes
6	RO	0		
5	RO	1		
4	RO	0		
3	RO	0		
2	RO	0		
1	RO	0		
0	RO	0		

4.8.5 BYTE 3 (Mode control)

If I2C_EN=0, this byte is Read Only register. If I2C_EN=1, This byte is Read/Write register.

Bit	Type	Power up condition	Default	Control affected	Comment
7	R/W	0	0	CONF<3>	Channel Preset assignment for the Preset Application Mode,
6	R/W	Latch	0	CONF<2>	
5	R/W	Latch	0	CONF<1>	
4	R/W	Latch	0	CONF<0>	
3	R/W	0	0	Reserved	
2	R/W	Latch	0	PIN_RXDET_EN# Inverted version of Pin9 RXDET_EN	Far end Receiver termination detection Enable (Active Low) 0 - Detection is enabled. 1 - Detection is disabled.
1:0	R/W	0	0		Reserved

4.8.6 BYTE 4 (Override the power down control)

If I2C_EN=0, this byte is Read Only register. If I2C_EN=1, this byte is Read/Write register.

Bit	Type	Power up condition	Default	Control affected	Comment
7	R/W	Latch EN pin	0	PD_CON_RX1	CONx power down override 0 – Normal operation 1 – Force the CONx to power down state
6	R/W	Latch EN pin	0	PD_CON_TX1	
5	R/W	Latch EN pin	0	PD_CON_TX2	
4	R/W	Latch EN pin	0	PD_CON_RX2	
3	R/W	1	1	Reserved	
2	R/W	1	1	Reserved	
1	R/W	0	0	IN_HPD_ActiveHigh_EN#	0 - IN_HPD Active High 1 - IN_HPD Active Low
0	R/W	1	1	Reserved	

4.8.7 BYTE 5 (Equalization, Flat gain and -1dB linear Swing setting of CON_RX2)

If I2C_EN=0, this byte is Read Only register. If I2C_EN=1, this byte is Read/Write register.

Bit	Type	Power up condition	Default	Control affected	Comment
7	R/W	Latch EQ	0	CON_RX2_EQ<3>	CON_RX2 setting configuration Equalizer Flat gain Swing
6	R/W	Latch EQ	0	CON_RX2_EQ<2>	
5	R/W	Latch EQ	0	CON_RX2_EQ<1>	
4	R/W	Latch EQ	0	CON_RX2_EQ<0>	
3	R/W	Latch_FG	0	CON_RX2_FG<1>	
2	R/W	Latch_FG	1	CON_RX2_FG<0>	
1	R/W	Latch_SW	1	CON_RX2_SW<1>	
0	R/W	Latch_SW	1	CON_RX2_SW<0>	

4.8.8 BYTE 6 (Equalization, Flat gain and -1dB linear Swing setting of CON_TX2)

If I2C_EN=0, this byte is Read Only register. If I2C_EN=1, this byte is Read/Write register.

Bit	Type	Power up condition	Default	Control affected	Comment
7	R/W	Latch EQ	0	CON_TX2_EQ<3>	CON_TX2 setting configuration Equalizer Flat gain Swing
6	R/W	Latch EQ	0	CON_TX2_EQ<2>	
5	R/W	Latch EQ	0	CON_TX2_EQ<1>	
4	R/W	Latch EQ	0	CON_TX2_EQ<0>	
3	R/W	Latch_FG	0	CON_TX2_FG<1>	
2	R/W	Latch_FG	1	CON_TX2_FG<0>	
1	R/W	Latch_SW	1	CON_TX2_SW<1>	
0	R/W	Latch_SW	1	CON_TX2_SW<0>	

4.8.9 BYTE 7 (Equalization, Flat gain and -1dB linear Swing setting of CON_TX1)

If I2C_EN=0, this byte is Read Only register. If I2C_EN=1, this byte is Read/Write register.

Bit	Type	Power up condition	Default	Control affected	Comment
7	R/W	Latch EQ	0	CON_TX1_EQ<3>	CON_TX1 setting configuration Equalizer Flat gain Swing
6	R/W	Latch EQ	0	CON_TX1_EQ<2>	
5	R/W	Latch EQ	0	CON_TX1_EQ<1>	
4	R/W	Latch EQ	0	CON_TX1_EQ<0>	
3	R/W	Latch_FG	0	CON_TX1_FG<1>	
2	R/W	Latch_FG	1	CON_TX1_FG<0>	
1	R/W	Latch_SW	1	CON_TX1_SW<1>	
0	R/W	Latch_SW	1	CON_TX1_SW<0>	

4.8.10 BYTE 8 (Equalization, Flat gain and -1dB linear Swing setting of CON_RX1)

If I2C_EN=0, this byte is Read Only register. If I2C_EN=1, this byte is Read/Write register.

Bit	Type	Power up condition	Default	Control affected	Comment
7	R/W	Latch EQ	0	CON_RX1_EQ<3>	CON_RX1 setting configuration Equalizer Flat gain Swing
6	R/W	Latch EQ	0	CON_RX1_EQ<2>	
5	R/W	Latch EQ	0	CON_RX1_EQ<1>	
4	R/W	Latch EQ	0	CON_RX1_EQ<0>	
3	R/W	Latch_FG	0	CON_RX1_FG<1>	
2	R/W	Latch_FG	1	CON_RX1_FG<0>	
1	R/W	Latch_SW	1	CON_RX1_SW<1>	
0	R/W	Latch_SW	1	CON_RX1_SW<0>	

4.8.11 BYTE 9 (RESERVED)

4.8.12 BYTE 10 (Feature control of the CON_RX2 and CON_TX2)

- CON2 represents CON_RX2 and CON_TX2

Bit	Type	Power up condition	Control affected	Comment
7	R/W	1	CON2 Feature 0	
6	R/W	1	CON2 Feature 1	
5	R/W	1	CON2 Feature 2	
4	R/W	1	CON2 Feature 3	
3	R/W	1	CON2 Feature 4	
2	R/W	1	CON2 Feature 5	
1	R/W	0	CON2 Feature 6	
0	R/W	0	CON2 Feature 7	

4.8.13 BYTE 11 (Feature control of the CON_RX1 and CON_TX1)

CON1 represents CON_RX1 and CON_TX1

Bit	Type	Power up condition	Control affected	Comment
7	R/W	1	CON1 Feature 0	
6	R/W	1	CON1 Feature 1	
5	R/W	1	CON1 Feature 2	
4	R/W	1	CON1 Feature 3	
3	R/W	1	CON1 Feature 4	
2	R/W	1	CON1 Feature 5	
1	R/W	0	CON1 Feature 6	
0	R/W	0	CON1 Feature 7	

4.8.14 BYTE 12 (Threshold, feature Enable/Disable and timing setting)

Bit	Type	Power up condition	Control affected	Comment
7	R/W	0	IDET_VTH<1>	High Speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default) 10 80mVppd 11 95mVppd
6	R/W	1	IDET_VTH<0>	
5	R/W	0	Reserved	
4	R/W	1	Reserved	
3	R/W	1	Reserved	
2	R/W	0	DP_HPD_PIN_EN#	Enable the IN_HPD Pin, so the redriver will response to this pin. 0 – Enabled 1 – Disabled
1	R/W	0	AUX _EN#	Enable/Disable the AUX Mux 0 – Enabled 1 – Disabled
0	R/W	0	Reserved	

4.8.15 BYTE 13 - 31 : Reserved

5. Electrical Specification

5.1 Absolute Maximum Ratings

Supply Voltage to Ground Potential.....–0.5 V to +3.8 V
DC SIG Voltage..... –0.5 V to V_{DD} + 0.5 V
CML Continuous Output Current.....+30 to +30mA
Storage Temperature .....–65 °C to +150 °C
Junction Temperature .....125°C
ESD HBM.....±2000V
ESD CDM.....±500V

Note:
(1) Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to beyond the absolute maximum rating conditions for extended periods may affect inoperability and degradation of device reliability and performance.

5.2 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max	Units
V_{DD}	VDD Supply Voltage	3.0	3.3	3.6	V
V_{DD_I2C}	VDD I2C Supply Voltage			3.6	V
V_{NOISE}	Supply Noise up to 50 MHz(1)		100		mVpp
T_A	Ambient Temperature, Commercial C-temp range	0		70	°C
	Ambient Temperature, Industrial I-temp range	-40(2)		85	

Notes:
(1) Allowed supply noise (mVpp sign wave) under typical condition
(2) Industrial temperature -40 to +85 °C can be guaranteed by design. Commercial temperature 0 to +70 °C is supported by the production-tested.

5.3 Thermal Information

Symbol	Parameter	42-pin TQFN	Unit
Theta JA	Junction-to-ambient resistance	35.34	°C/W
Theta JC	Junction-to-case (top) thermal resistance	15.17	°C/W

5.5 Power Consumption

Over operating temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
I_{PD}	Typical Pin Power Down current, VDD=3.3V	EN = 0		26	100	µA
I_{DDQ_PD}	I2C Power Down current, VDD=3.3V	EN=1, I2C Byte4<7:4>=1111		112	340	µA
DP1.4 Mode						
I_{DD_DP}	Power supply current in DP mode EN =1, VDD=3.3V	1-lane DP		33	55	mA
		2-lane DP		66	110	mA
		4-lane DP		132	210	mA
1-lane USB 3.1 Gen2 Mode						
I_{U0}	Current in USB U0 mode, VDD=3.3V	EN=1, USB U0 mode		80	112	mA
I_{U1}	Current in USB U1 mode, VDD=3.3V	EN=1, USB U1 mode		16	20	mA
$I_{U2/U3}$	Current in USB U2/U3 modes. VDD=3.3V	EN=1, USB U2/U3 mode		0.5	0.6	mA
I_{RXDET}	Current in USB RXDET mode, VDD=3.3V	EN=1, USB RXDET mode		0.5	0.6	mA

5.6 AC/DC Characteristics

Over operating temperature range (unless otherwise noted)

5.6.1 LVCMOS I/O DC Specifications

Symbol	Parameter	Min.	Typ.	Max	Unit
2-level control pins					
V_{IH}	DC input logic High	V_{DD}*0.65			V
V_{IL}	DC input logic Low			V_{DD}*0.35	V
I_{IH}	Input High current			25	uA
I_{IL}	Input Low current	-25			uA
4-level control pins					
V_{IH}	DC input logic "High"	0.92*V_{DD}	V_{DD}		V
V_{IF}	DC input logic "Float"	0.59*V_{DD}	0.67*V_{DD}	0.75*V_{DD}	V
V_{IR}	DC input logic "With Rext to GND"	0.25*V_{DD}	0.33*V_{DD}	0.41*V_{DD}	V
V_{IL}	DC input logic "Low"		GND	0.08*V_{DD}	V
I_{IH}	Input High current			50	uA
I_{IL}	Input Low current	-50			uA
R_{EXT}	External resistor connects to GND (±5%)		68		kΩ

5.6.2 USB Differential Channel

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB differential Input						
$C_{RXPARASITIC}$	The parasitic capacitor for RX				1.0	pF
$R_{RX-DIFF-DC}$	DC Differential Input Impedance		72		120	Ω
R_{RX-CM_DC}	DC common mode input impedance	DC impedance limits are need to guarantee RxDet. Measured with respect to GND over a voltage of 500mV max	18		30	
$Z_{RX-HIZ-DC-PD}$	DC input CM input impedance for V>0 during reset or power down	(Vcm=0 to 500mV)	25			kΩ
$C_{AC\_COUPLING}$	AC coupling capacitance		75		265	nF
$V_{RX-CM-AC-P}$	Common mode peak voltage	AC up to 5GHz			150	mVpeak
$V_{RX-CM-DC-Active-Idle-Delta-P}$	Common mode peak voltage[1]	Between U0 and U1. AC up to 5GHz			200	mVpeak
USB differential Output						
$V_{TX-DIFF-PP}$	Output differential p-p voltage swing	Differential Swing $\|V_{TX-D+}-V_{TX-D-}\|$			1.2	Vppd
$R_{TX-DIFF-DC}$	DC Differential TX Impedance		72		120	Ω
$V_{TX-RCV-DET}$	The amount of voltage change allowed during RxDet				600	mV
$C_{ac\_coupling}$	AC coupling capacitance		75		265	nF
$T_{TX-EYE(10Gbps)}$	Transmitter eye, Include all jitter	At the silicon pad. 10Gbps	0.646			UI
$T_{TX-EYE(5Gbps)}$	Transmitter eye, Include all jitter	At the silicon pad. 5Gbps	0.625			UI
$T_{TX-DJ-DD(10Gbps)}$	Transmitter deterministic jitter	At the silicon pad. 10Gbps			0.17	UI
$T_{TX-DJ-DD(5Gbps)}$	Transmitter deterministic jitter	At the silicon pad. 5Gbps			0.205	UI
$C_{TXPARASITIC}$	The parasitic capacitor for TX				1.1	pF
R_{TX-CM_DC}	Common mode DC output Impedance		18		30	Ω
$V_{TX-DC-CM}$	The instantaneous allowed DC common mode voltage at the connector side of the AC coupling capacitors	$\|V_{TX-D+}+V_{TX-D-}\|/2$	0		2.2	V
V_{TX-C}	Common-Mode Voltage	$\|V_{TX-D+}+V_{TX-D-}\|/2$	VDD-2V		VDD	V
$V_{TX-CM-AC-PP-Active}$	Active mode TX AC common mode voltage	$V_{TX-D+}+V_{TX-D-}$ for both time and amplitude			100	mVpp
$V_{TX-CM-DC-Active\_Idle-Delta}$	Common mode delta voltage $\|Avg_{uo}(\|V_{TEX-D+} + V_{TX-D-}\|)/2-Avg_{u1}(\|V_{TX-D+} + V_{TX-D-}\|)/2\|$	Between U0 to U1			200	mV-peak

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{TX-Idle-Diff-AC-pp}$	Idle mode AC common mode delta voltage|V_{TX-D+}-V_{TX-D-}|	Between Tx+ and Tx- in idle mode. Use the HPF to remove DC components. =1/LPF. No AC and DC signals are applied to Rx terminals .			10	mVppd
$V_{TX-Idle-Diff-DC}$	Idle mode DC common mode delta voltage|V_{TX-D+}-V_{TX-D-}|	Between Tx+ and Tx- in idle mode. Use the LPF to remove DC components. =1/HPF. No AC and DC signals are applied to Rx terminals.			10	mV
G_P	Peaking gain (Compensation at 5GHz, relative to 100MHz, 100mV_{p-p} sine wave input)	EQx=0 EQx=R EQx=F EQx=1		5.7 8.9 11.1 12.6		dB
		Variation around typical	-3		+3	dB
G_F	Flat gain (100MHz, EQx=F, SWx=F)	FGx=0 FGx=R FGx=F FGx=1		-1.5 0 +1 +2.5		dB
		Variation around typical	-3		+3	dB
V_{SW_100M}	-1dB compression point output swing (at 100MHz)	SWx=0 SWx=1		900 1000		mVppd
V_{SW_5G}	-1dB compression point output swing (at 5GHz)	SWx=0 SWx=1		600 750		mVppd
DD_{NEXT}(2)	Differential near-end crosstalk	100MHz to 5GHz		-45		dB
DD_{FEXT}(2)	Differential far-end crosstalk	100MHz to 5GHz		-45		dB
$V_{NOISE-INPUT}$	Input-referred noise	100MHz to 5GHz, FGx=1, EQx-=R, SW=F		0.6		mV_{RMS}
		100MHz to 5GHz, FGx=1, EQx=1, SW=F		0.5		
$V_{NOISE-OUTPUT}$	Output-referred noise[2]	100MHz to 5GHz, FGx=1, EQx-=R, SW=F		0.8		mV_{RMS}
		100MHz to 5GHz, FGx=1, EQx=1, SW=F		1		
S11	Input return loss	10 MHz to 4.1 GHz differential		-13.0		dB
		1 GHz to 4.1 GHz common mode		-5.0		
S22	Output return loss	10 MHz to 4.1 GHz differential		-15		dB
		1 GHz to 4.1 GHz common mode		-6.0		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Signal and Frequency Detectors						
V_{TH_UPM}	Unplug mode detector threshold	Threshold of LFPS when the input impedance of the redriver is 67kohm to VbiasRx only. Used in the unplug mode.	200		800	mVppd
V_{TH_DSM}	Deep slumber mode detector threshold	LFPS signal threshold in Deep slumber mode	100		600	mVppd
V_{TH_AM}	Active mode detector threshold	Signal threshold in Active and slumber mode	65		175	mVppd
F_{TH}	LFPS frequency detector	Detect the frequency of the input CLK pattern	100		400	MHz
T_{ON_UPM}	Turn on of unplug mode	TX pin to RX pin latency when input signal is LFPS			3	mS
$T_{ON\text{-}DSM}$	Turn on of deep slumber mode				5	µS
T_{ON_SM}	Turn on of slumber mode				20	ns

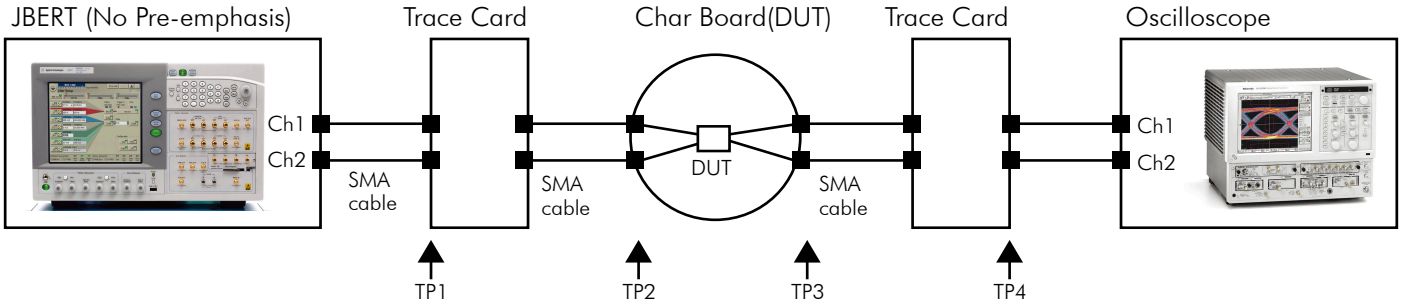
Note:
(1) Measured using a vector-network analyzer (VNA) with -15dbm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
(2) Subtract the Channel Gain from the Total Gain to get the Actual Crosstalk

5.6.3 DisplayPort Differential Channel

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{ID}	Peak to peak differential input voltage			400	1200	mV
V_{ODO}	Differential overshoot voltage				15%*V3P3	V3P3
V_{ODU}	Differential undershoot voltage				25%*V3P3	V3P3
Isc	Output short current				60	mA
Vtx diff-lev1	Differential pk-pk level 1		340	400	460	mV
Vtx diff-lev2	Differential pk-pk level 2		510	600	680	mV
Vtx diff-lev3	Differential pk-pk level 3		690	800	920	mV
Vtx diff-lev4	Differential pk-pk level 4		1020	1200	1380	mV
G_P	Peaking gain: Compensation at 4 GHz, relative to 100 MHz, 100 mVp-p sine wave input	EQx=0 EQx=R EQx=F EQx=1		4.9 7.7 9.8 11.3		dB
		Variation around typical	-3		+3	dB
G_F	Flat gain: 100 MHz, EQ[3:0] = 1000, SW[1:0] = 10	FGx=0 FGx=R FGx=F FGx=1		+1 -1.5 0 2.5		dB
		Variation around typical	-3		+3	dB
V_{1dB_100M}	-1 dB compression point of output swing at 100 MHz	SWx = 0 SWx = 1		1100 1200		mVppd
T_R /T_F	Rise and Fall Time	20% to 80 %		30		ps
$T_{SK(D)}$	Intra-pair differential skew				50	ps
$T_{SK(O)}$	Intra-pair differential skew				50	ps

5.6.4 Hot Plug/Unplug Detect Circuitry

Parameter	Min	Typ	Max	Unit	Notes
HPD Voltage	2.25		3.6	V	
Hot Plug Detection Threshold	2.0			V	
Hot Unplug Detection Threshold			0.8	V	
HPD pin Termination	200			kΩ	To GND
HPD de-assert debounce timer	200		450	ms	Any HPD Low to High edge will reset the debounce timer



1) Trace card between TP1 and TP2 is designed to emulate 6-48" of FR4. Trace width -4 mils,100Ω differnetial impedance
2) All jitter is measured at a BER of 10-9
3) Residual jitter reflects the total jitter measured at TP4 jitter minus TP1 jitter
4) VDD = 3.3V, RT = 50Ω
5) The input signal from JBERT does not have any pre-emphasis.

Figure 5-1 AC Electrical Parameter test setup

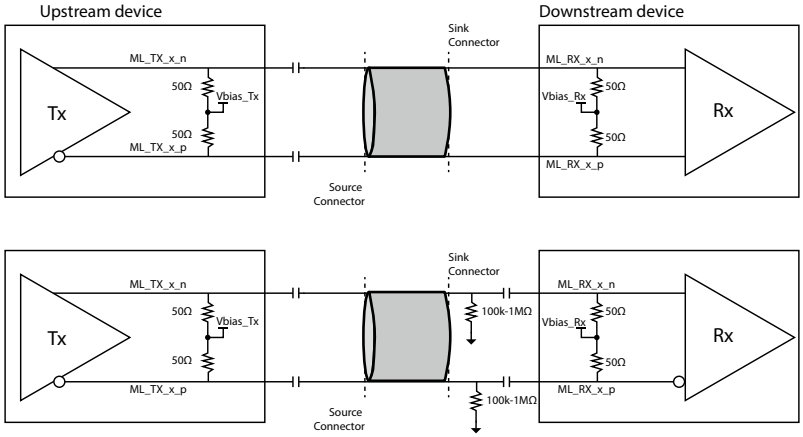


Figure 5-2 High-speed Chanel Test Circuit

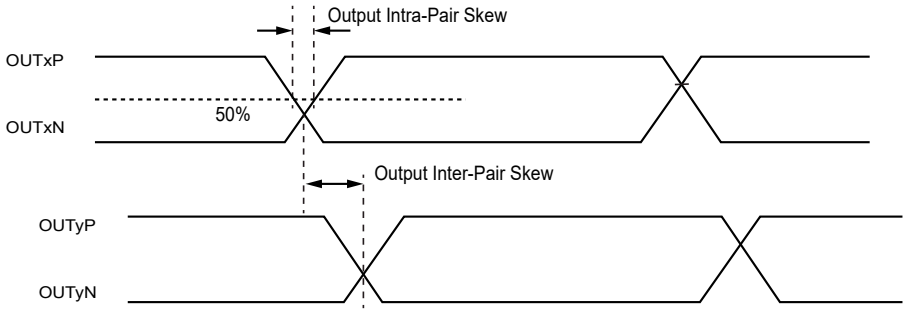


Figure 5-3 Intra and Inter-pair Differential Skew definition

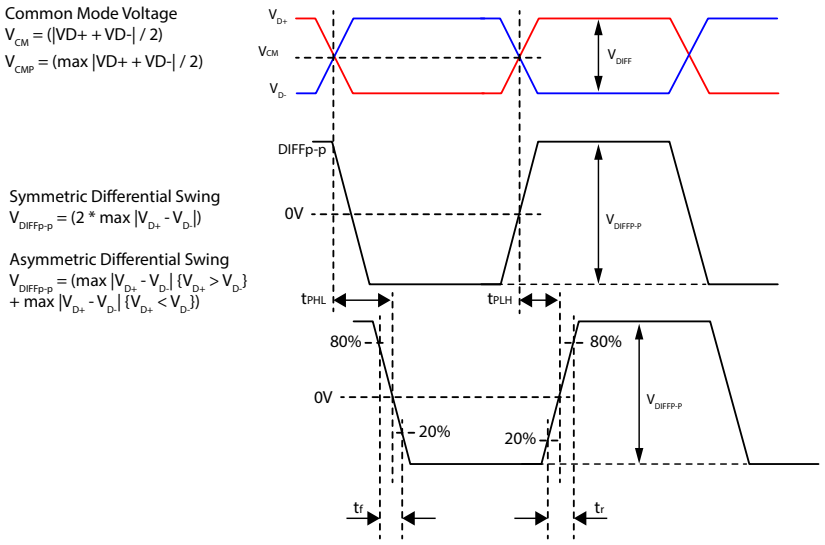


Figure 5-4 Definition of Peak-to-peak Differential voltage

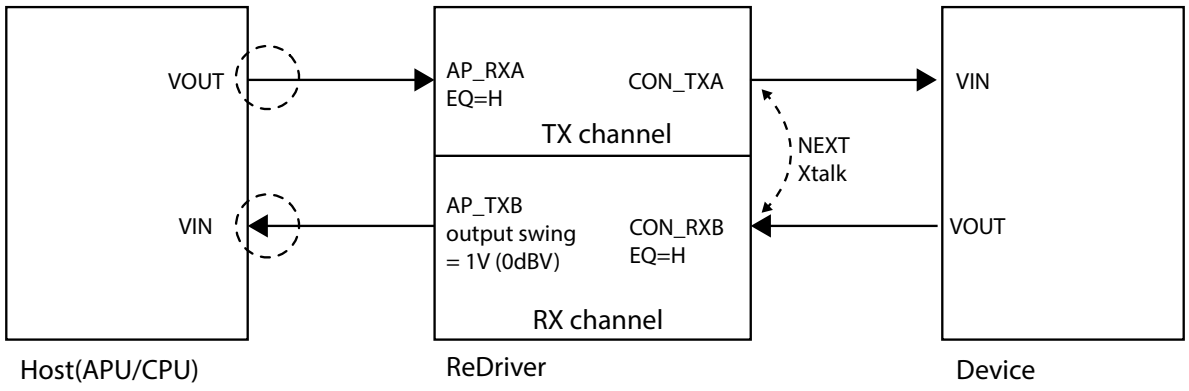


Figure 5-5 NEXT Crosstalk definition

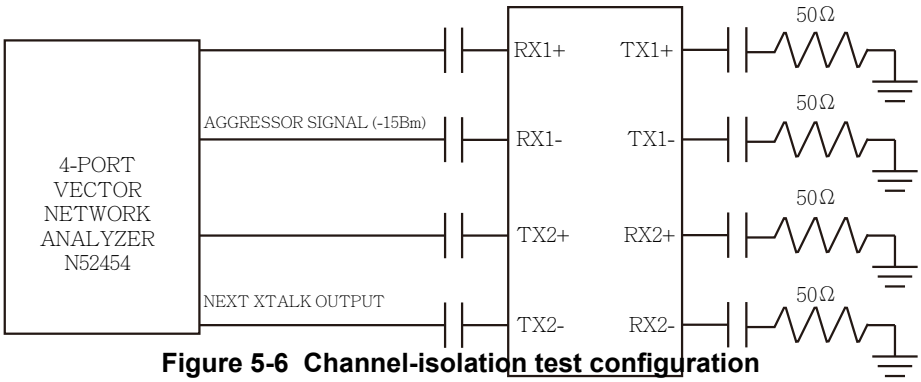


Figure 5-6 Channel-isolation test configuration

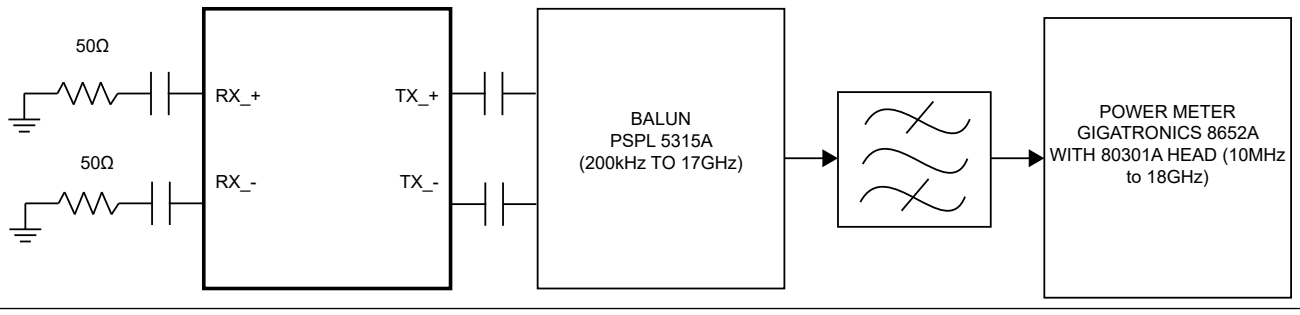


Figure 5-7 Noise test configuration

5.6.5 I2C Bus SCL/SDA Specification

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IL}	DC input logic LOW		-0.5		0.4	V
V_{IH}	DC input logic HIGH		1.2		V_{DD}	V
V_{OL1}	DC output logic LOW voltage	(open-drain or open-collector) at 3 mA sink current;	0		0.4	V
I_{OL}	LOW-level output current	V_{OL} = 0.4V	20			mA
		V_{OL} = 0.6V	6			mA
I_i	Input current each I/O pin		-10		10	uA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	Bus Operation Frequency				1000	KHz
t_{BUF}	Bus Free Time Between Stop and Start condition		1.3			us
$t_{HD:STA}$	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At Ipull-up, Max	0.6			us
$t_{SU:STA}$	Repeated start condition setup time		0.26			us
$t_{SU:STO}$	Stop condition setup time		0.26			us
$t_{HD:DAT}$	Data hold time		0			ns
$t_{SU:DAT}$	Data setup time		50			ns
t_{LOW}	Clock Low period		0.5			us
t_{HIGH}	Clock High period		0.26		50	us
t_F	Clock/Data fall time				120	ns
t_R	Clock/Data rise time				120	ns

Notes:
(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Compliant to I2C physical layer specification.
(4) VIL = 0.4V and VIH = 1.2V because the silicon needs to support both SCL/SDA with 1.8V/3.3V signaling level.

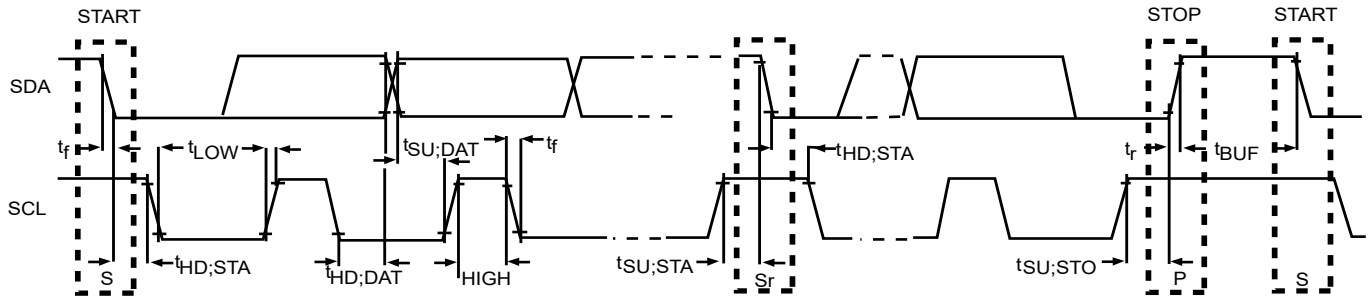


Figure 5-8 Definition of timing for F/S-mode on the I2C-bus

6. Applications

Note:
Information in the following applications sections is not part of the component specification, and does not warrant its accuracy or completeness. Customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Channel connection diagram

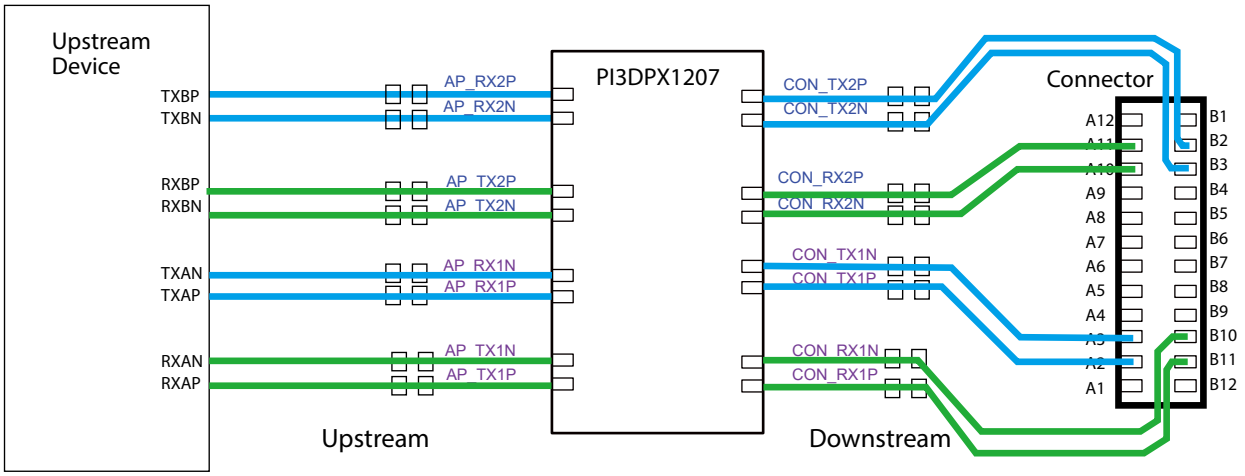
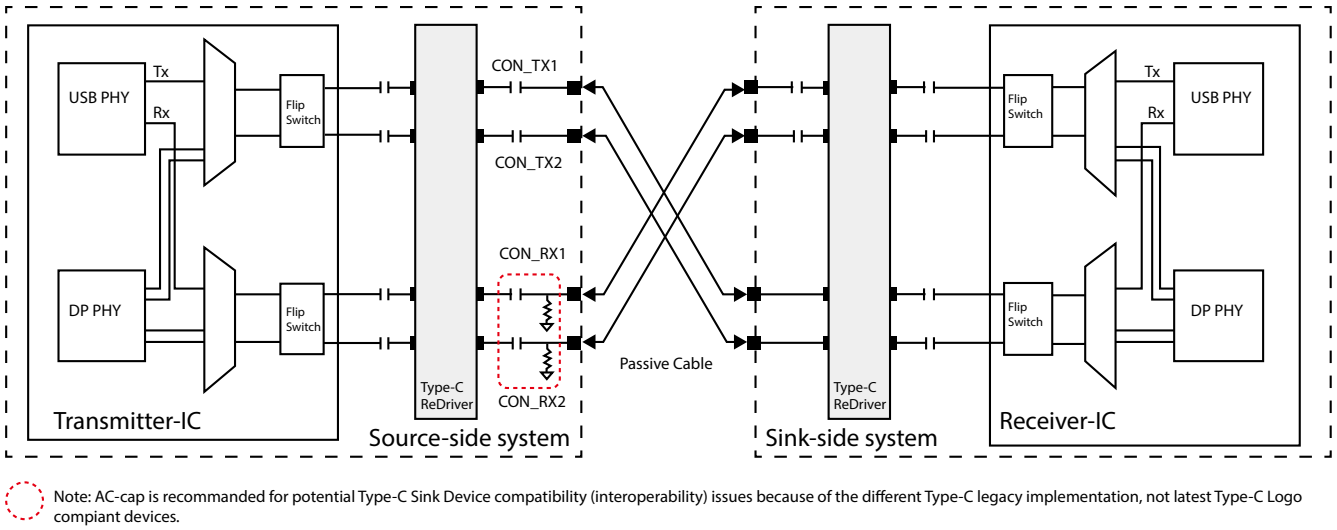


Figure 6-1 Source-side Host to USB Type-C Connector connection diagram

6.2 Type-C AC-cap connection diagram



Note: AC-cap is recommanded for potential Type-C Sink Device compatibility (interoperability) issues because of the different Type-C legacy implementation, not latest Type-C Logo compiant devices.

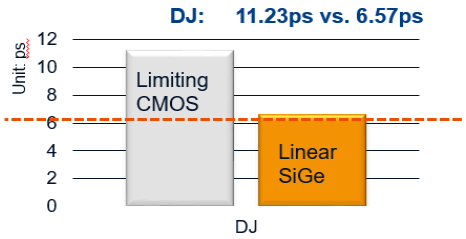
Figure 6-2 AC-capacitor circuits in the high speed channel for Type-C and DP-captive cable

6.3 SiGe BiCMOS vs. CMOS Redrivers Jitter performance

Linear SiGe Redriver jitter test result was shown below. As known, SiGe Redriver can cover most of the Notebook PC routing trace length.

6Gbps(3GHz) CMOS Limiting ReDriver Jitter Measurement Data

	Input Jitter (TP1)	Output Jitter (TP2)	Output - Input	SQRT (Output²-input²)	Units
Random Jitter	0.765	0.954		0.57	RMS ps
Deterministic Jitter	9.632	20.86	11.23		ps



6Gbps(3GHz) BiCmos Linear ReDriver Jitter Measurement Data

	Input Jitter (TP1)	Output Jitter (TP2)	Output - Input	SQRT (Output²-input²)	Units
Random Jitter	0.740	0.775		0.23	RMS ps
Deterministic Jitter	9.138	15.70	6.57		ps

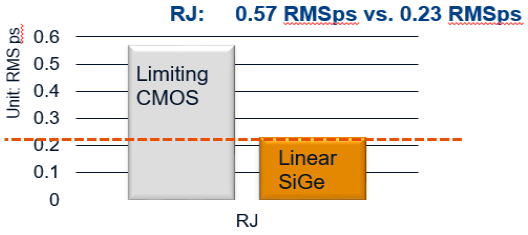


Figure 6-3 SiGe BiCmos vs CMOS Redriver performance comparison

6.4 Redriver Placement Consideration

6.4.1 USB3.1 10Gbps System Design Challenges

- Jitter budget is basis for Tx and Rx compliance specs.
- Loss budget is basis for compliance channels, including pad cap, package, PCB routing

Table 6-1. USB channel Jitter Budget

	DJ (ps)	RJ (ps)	TJ (ps)	Term	Comments
Tx Jitter	17.0	14.1	31.1	Transmitter	Practical route length is <6". Consider a linear SiGe Redriver if design exceeds 8.5db
Channel Jitter	36.0		36.0	Channel	
Rx Jitter	27.1	14.1	41.2	Receiver	
Total	80.1	19.9	100.0	System	

6.4.2 Typical Routing Configuration

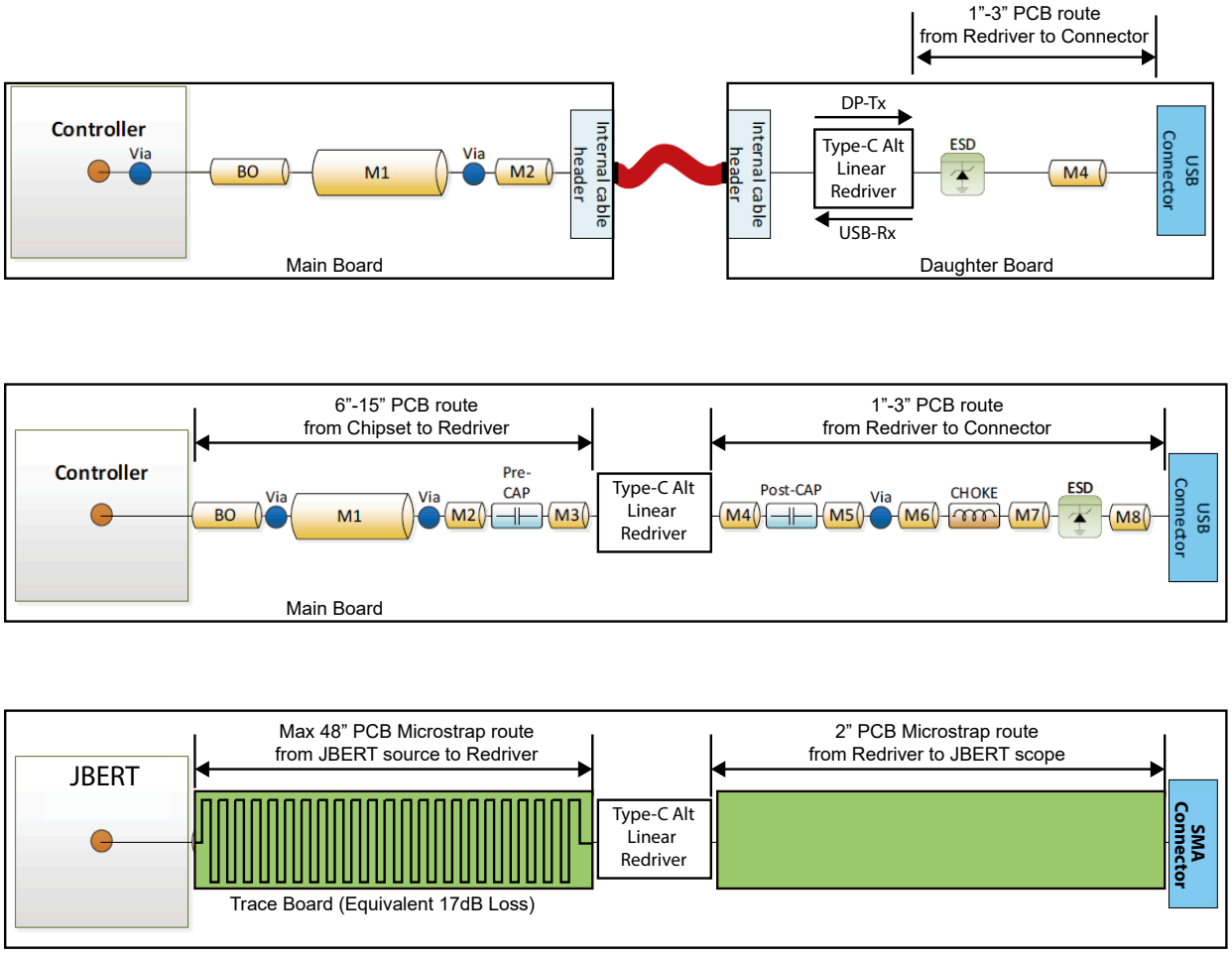


Figure 6-4 Redriver placement in the Source-side application

6.4.3 Type-C 10Gbps PCB routing estimates examples

Table 6-2. USB channel estimated FR-4 Trace Length with discrete Mux and Redriver

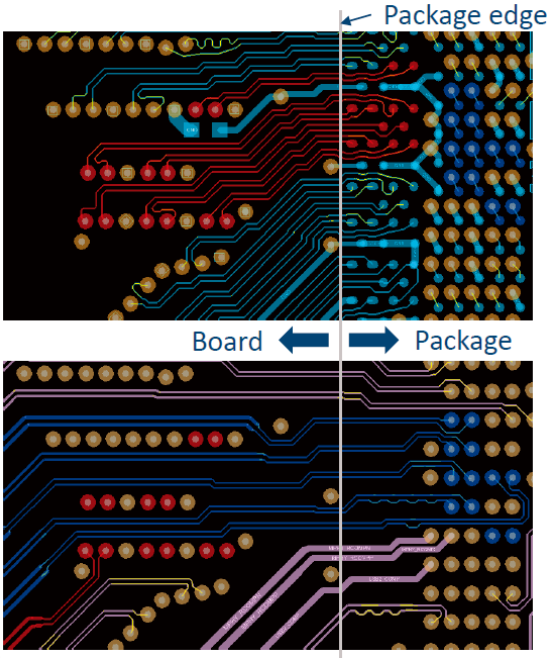
	5Gbps (USB Gen1)	10Gbps (USB Gen2)	Comments
Loss Budget	6.5dB @ 2.5GHz	8.5dB @ 5GHz	Loss budgets are for host/device from silicon to port connector.
USB 3.1 Host only	5.5” –6.5”	5.0” –6.0”	
USB 3.1 Host + Discrete Passive DP-Alt Crossbar mux	4.0” –5.0”	3.0” –4.0”	USB Type-C needs MUX for flipability and switching between USB3.1 and DP-Alt modes. Mux loss is ~1.5dB. It reduces max length by ~1dB/inch.
USB 3.1 + DP-Alt integrated Crossbar mux Host	5.5” –6.5”	5.0” –6.0”	No impact on the Rx-cap & Mux loss

Note:
(1) These are estimates only. Work with your supplier to determine actual supported length.
(2) Estimates assume silicon pad cap, jitter & swing at recommended / allowed by spec, direct route on PCB from package to Type C™ receptacle, integrated mux has no significant impact on silicon pad cap.
(3) Actual lengths also depend upon silicon (swing, jitter, EQ, pad cap), package (loss,impedance, crosstalk) and PCB materials.

6.4.4 PCB Crosstalk Minimization recommendation

Breakout Tx and Rx I/O on different PCB layers.

- Non-interleaved routing. Eliminates a key source of near end crosstalk.
- Places requirements on Tx & Rx I/O placement as shown below.



Board surface layer:
• Tx BGAs at outer region
• Breakout as Microstrip

Board inner layer:
• Rx BGAs at inner region
• Breakout as Stripline

Figure 6-5 Breakout Tx and Rx I/O on different PCB layers

6.5 Channel Output Eye Signal vs. EQ/FG/SW Setting (For ES samples Information Only)

6.5.1 Trace Test Board Insertion Loss Informations

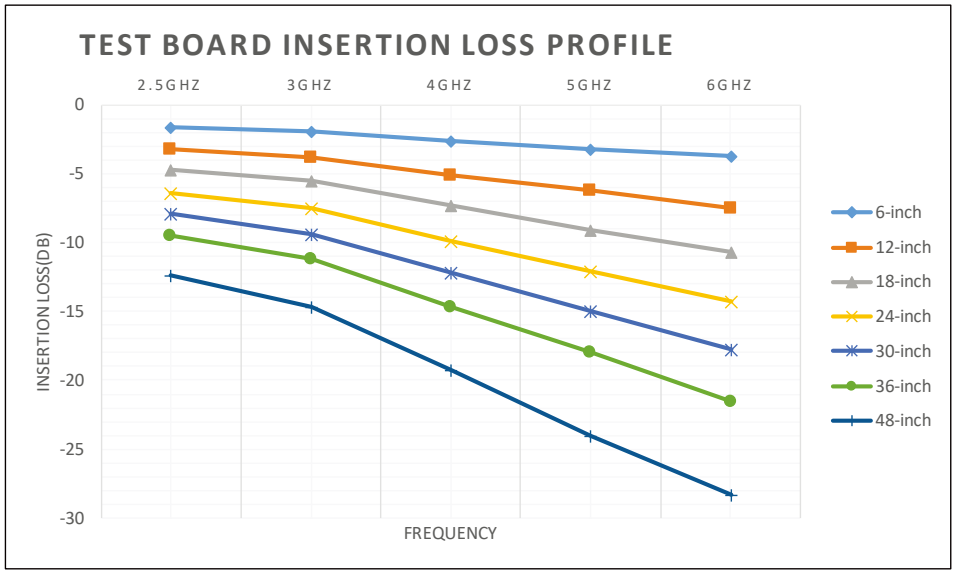


Figure 6-6 Trace Board PCB FR-4 Insertion Loss Profile

6.5.2 Eye Width/Height vs. EQ

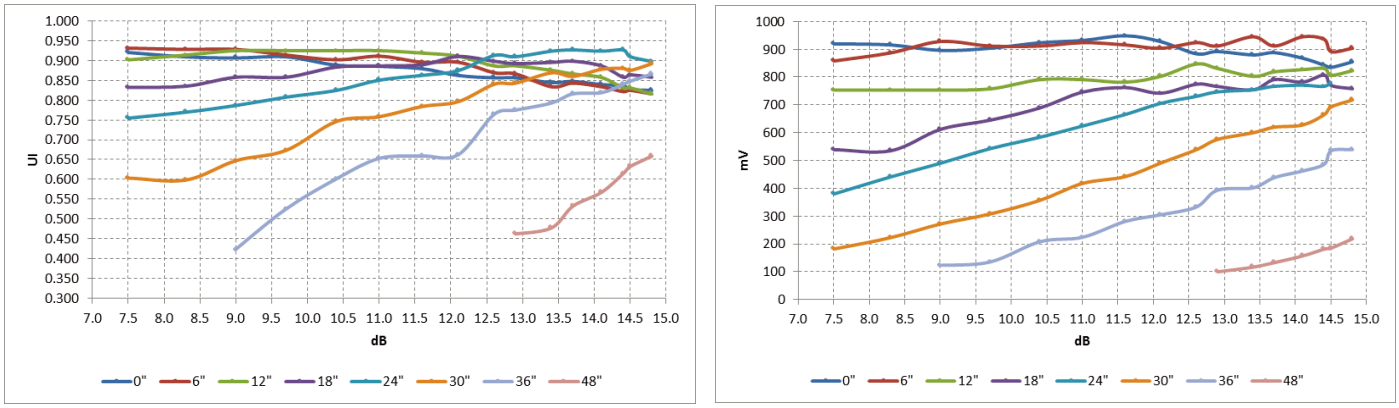
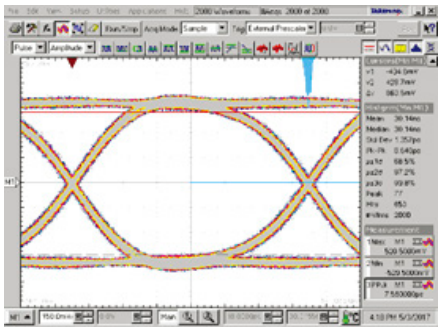


Figure 6-7 Eye Width Height vs. EQ setting curves at 8.1Gbps

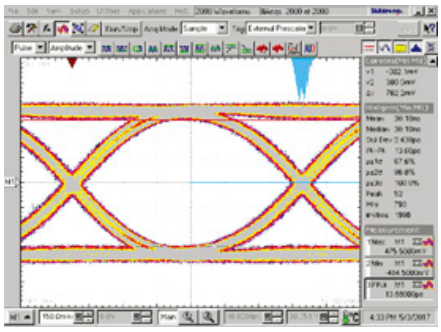
6.5.3 Channel Output waveforms

Test condition: Output Eye Opening with Input Equalization, 8.1Gbps, Vdd=3.0V, Using PRBS 2^23-1 pattern, Input Swing=1000mVd, Output Swing= 1000mV; FG=0dB, Direction: AP_TX2 to CON_RX2, I2C Byte 03 = 0x92h (USB3+2-Lane DP)

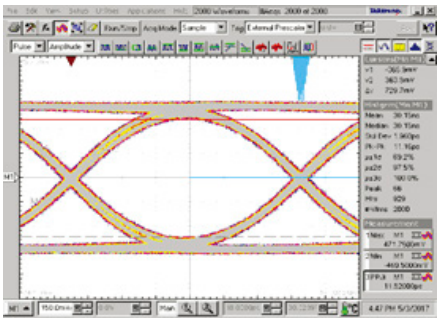
Trace=6-in, EQ=7.5dB



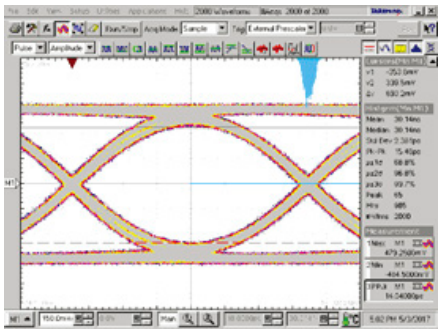
Trace=18-in, EQ=11.6dB



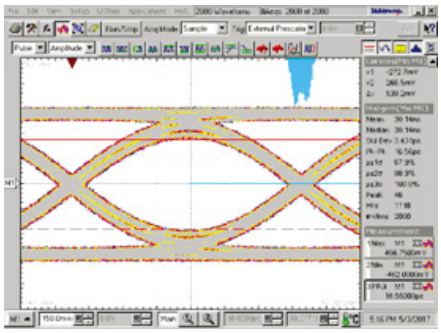
Trace=24-in, EQ=12.9dB



Trace=30-in, EQ=14.5dB



Trace=36-in, EQ=14.8dB



Trace=48-in, EQ=17.1dB

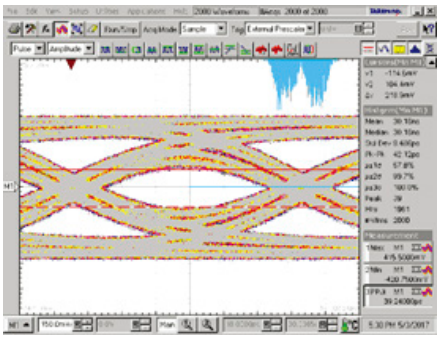
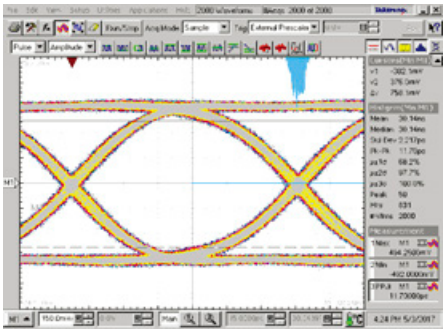


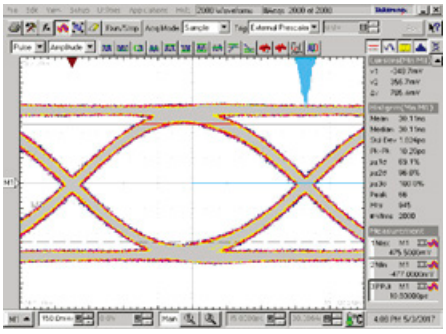
Figure 6-8 Output Eye Opening with EQ setting at DP1.4 8.1 Gbps

Output Eye Opening with Input Equalization, 10Gbps, Using PRBS 2^23-1 pattern, Input Swing=1000mVd, Output Swing= 1000mV; FG=0dB,
Direction: AP_TX2 to CON_RX2, I2C Byte 03 = 0x92h(USB3+2-Lane DP)

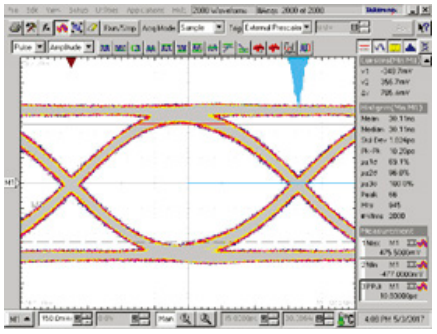
Trace=6-in, EQ=9.2dB



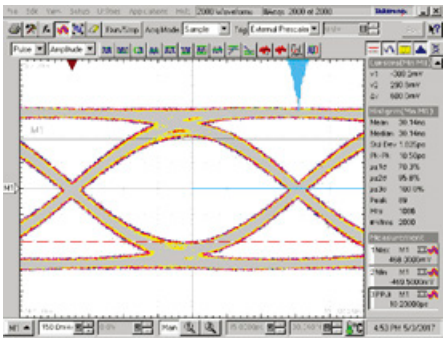
Trace=12-in, EQ=10.2dB



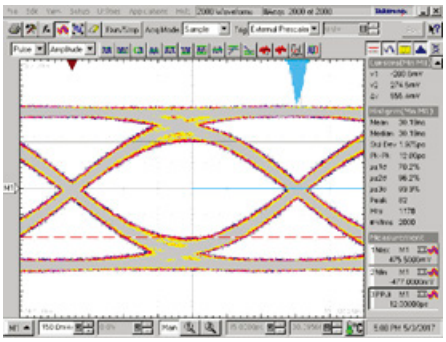
Trace=18-in, EQ=10.2dB



Trace=24-in, EQ=15dB



Trace=30-in, EQ=16.4dB



Trace=36-in, EQ=16.8dB

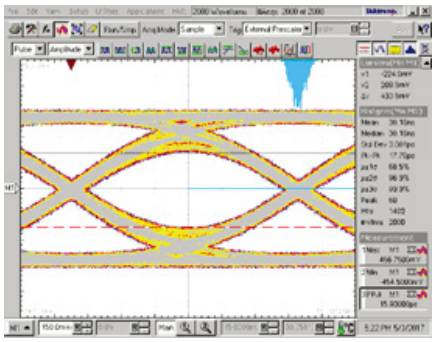


Figure 6-9 Output Eye Opening with EQ setting at USB3.1 Gen2 10Gbps

6.5.4 IDD(mA) changes vs. Gain and Swing

DP Mode, CONF[3:0]=0010 at (25 °C)

Control Setting	Gain (dB)	Swing(mV)	IDD at Vdd=3.0V	Idd at Vdd=3.3V	Idd at Vdd=3.6V
FG/SW=0000	-1.5	900	122	127	128
FG/SW=0001	-1.5	1000	125	131	132
FG/SW=0010	-1.5	1100	127	135	137
FG/SW=0011	-1.5	1200	130	139	141
FG/SW=0100	0	900	122	127	128
FG/SW=0101	0	1000	125	131	132
FG/SW=0110	0	1100	127	135	137
FG/SW=0111	0	1200	130	139	141
FG/SW=1000	+1.0	900	122	127	128
FG/SW=1001	+1.0	1000	125	131	132
FG/SW=1010	+1.0	1100	127	135	137
FG/SW=1011	+1.0	1200	130	139	141
FG/SW=1100	+2.5	900	122	127	128
FG/SW=1101	+2.5	1000	125	131	133
FG/SW=1110	+2.5	1100	127	135	137
FG/SW=1111	+2.5	1200	130	139	141
Average IDD (mA)			126	133	135
Average Power (mW)			378	399	404

6.6 Reference Application Schematics

- Aux CH & SBU1/2 polarity connection between host and PI3DPX1207 is swapped.

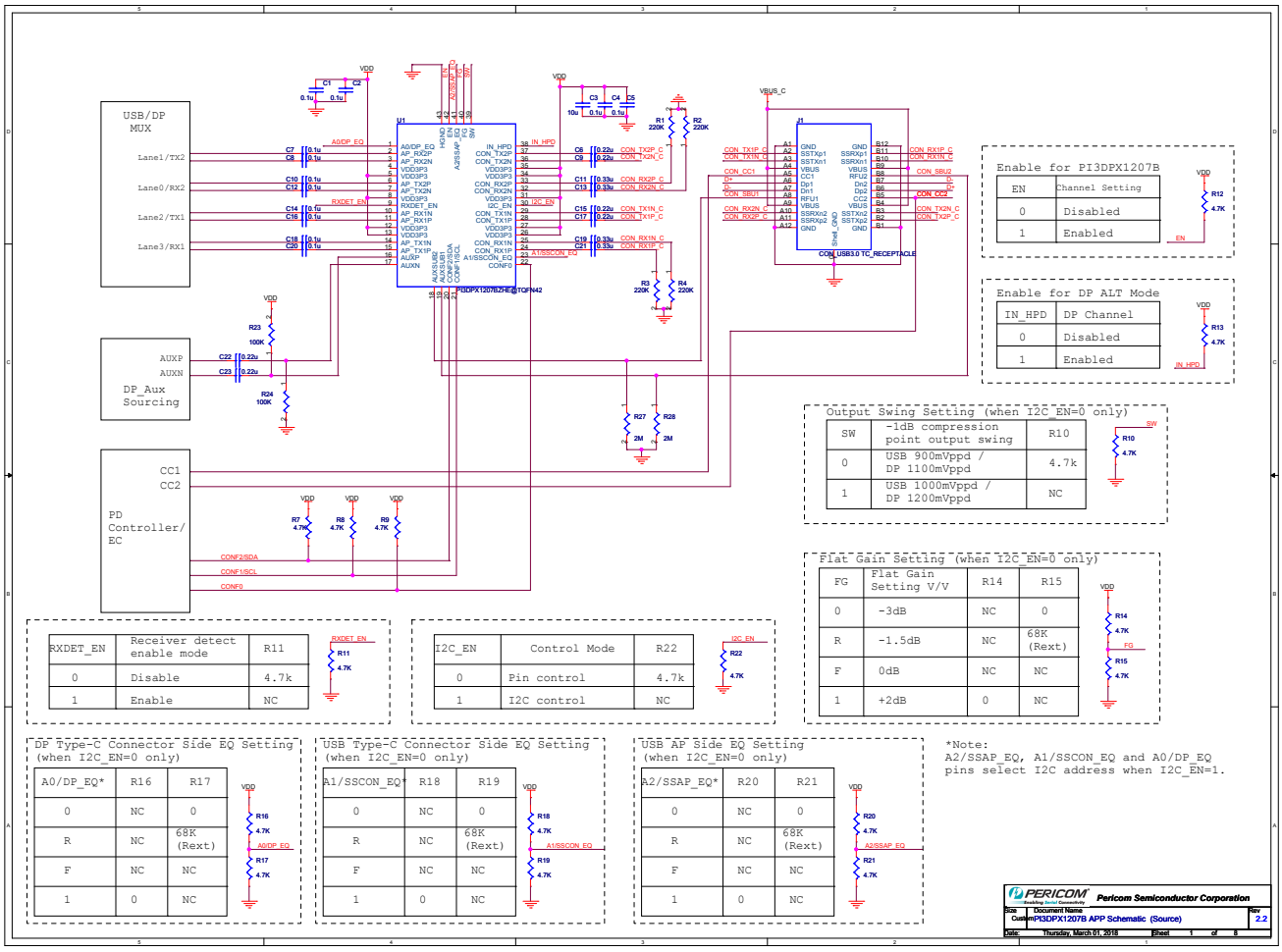


Figure 6-10 Reference EVB demo board application schematic

6.7 Type-C System Block diagram

6.7.1 PD Controller controls Type-C Redriver

In order to allow manufacturer to change EQ setting without modifying PD Controller's firmware,

- PD Controller vendor shall reserve 8x6=48bytes writable registers to store PI3DPX1207 EQ table.
- EC writes the EQ table into PD Controller every time the system is powered up or reset.
- PD Controller writes corresponding EQ/FG/SW settings and features into PI3DPX1207 byte4, 5, 6, 7, 8 and 12 via I2C every time before changing channel mapping setting byte3.
- When DP mode is selected and HPD is low, turn on PI3DPX1207 Aux switch via I2C byte4 and byte12.
- When HPD is high, enable display via I2C byte4 and byte12

This facilitates PI3DPX1207 EQ/FG/SW settings' tuning by manufacturer.

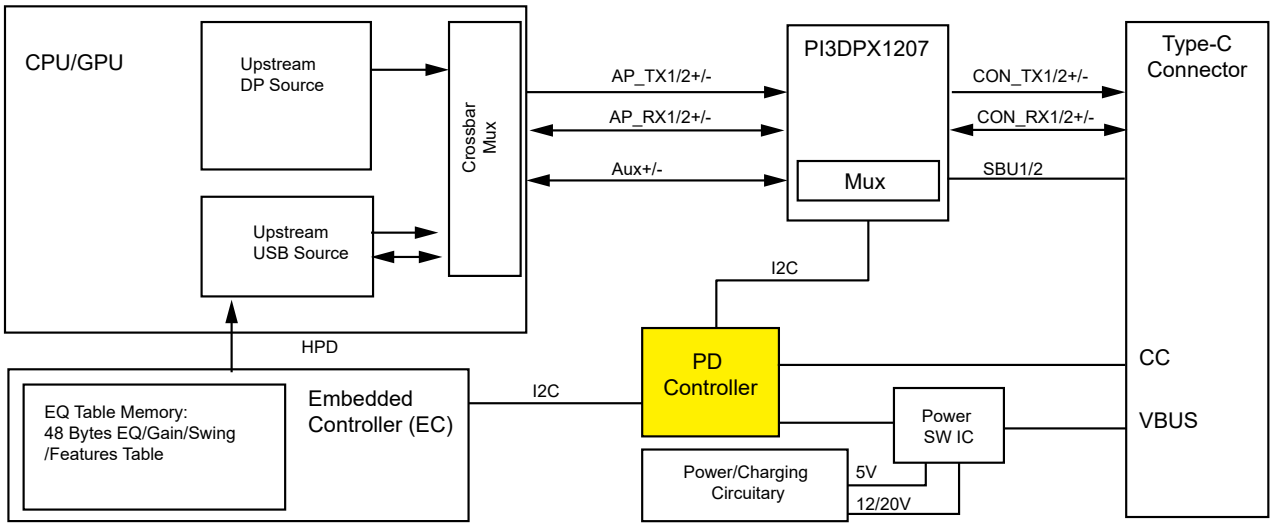


Figure 6-11 Source-side System block diagram with PD controller

Table 6-3. PI3DPX1207 I2C Settings Table

Conf	Byte4 (Power)	Byte 5 (CON_RX2)	Byte 6 (CON_TX2)	Byte 7 (CON_TX1)	Byte 8 (CON_RX1)	Byte12 (Features)	Mode
0000	0Dh	OPEN_EQ	OPEN_EQ	OPEN_EQ	OPEN_EQ	58h	Safe State
0001	0Dh	OPEN_EQ	OPEN_EQ	OPEN_EQ	OPEN_EQ	58h	Safe State
0010	EDh	DP0_EQ	DP1_EQ	DP2_EQ	DP3_EQ	5Ch	4 lane DP1.4 + AUX
0011	7Dh	DP3_FILP_EQ	DP2_FLIP_EQ	DP1_FILP_EQ	DP0_FLIP_EQ	5Ch	4 lane DP1.4 + AUX (flipped)
0100	0Dh	OPEN_EQ	OPEN_EQ	USB3TX1_EQ	USB3RX1_EQ	58h	1 lane USB3.x (AP_CH1)
0101	0Dh	USB3RX2_EQ	USB3TX2_EQ	OPEN_EQ	OPEN_EQ	58h	1 lane USB3.x (AP_CH2) flipped
0110	2Dh	DP0_EQ	DP1_EQ	USB3TX1_EQ	USB3RX1_EQ	5Ch	USB3 (AP_CH1) + 2 lane DP1.4 (AP_CH2) + AUX
0111	4Dh	USB3RX2_EQ	USB3TX2_EQ	DP1_FILP_EQ	DP0_FLIP_EQ	5Ch	USB3 (AP_CH2) + 2 lane DP1.4 (AP_CH1) + AUX (flipped)

6.7.2 Case B: EC controls Type-C Redriver

1) EC vendor shall reserve 8x6=48bytes writable registers to store PI3DPX1207 EQ table.
2) EC initializes PI3DPX1207 every time the system is powered up or reset.
3) EC reads channel mapping setting from PDC and writes corresponding EQ/FG/SW settings and features into PI3DPX1207 byte4, 5, 6, 7, 8 and 12 via I2C first, then change channel mapping setting via I2C byte3.
4) When DP mode is selected and HPD is low, turn on PI3DPX1207 Aux switch via I2C byte4 and byte12.
5) When HPD is high, enable display via I2C byte4 and byte12.

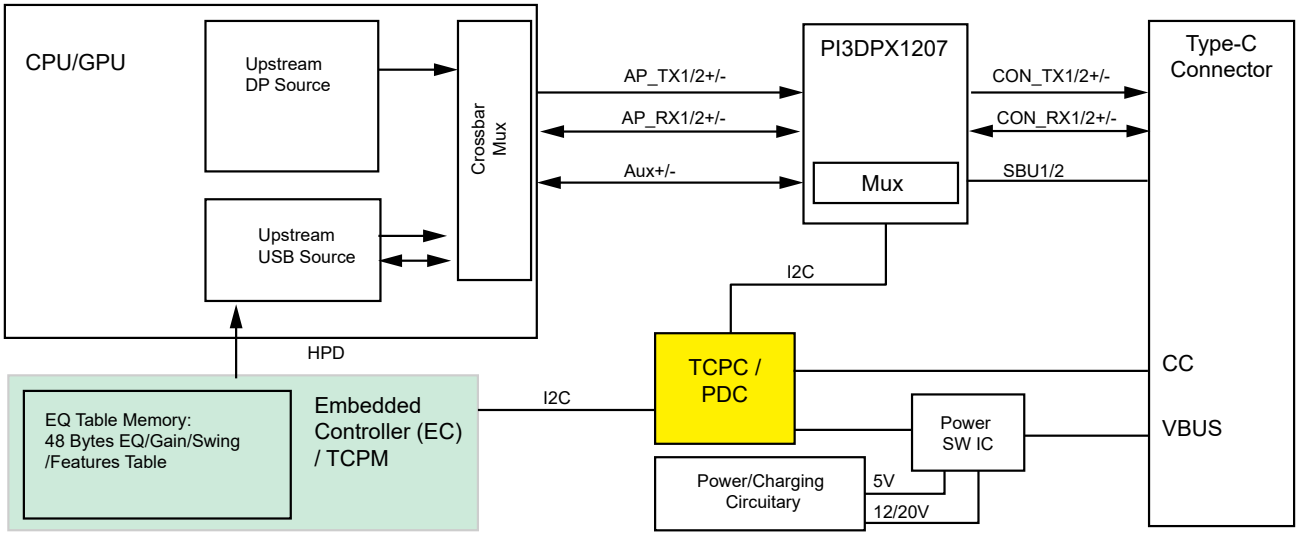
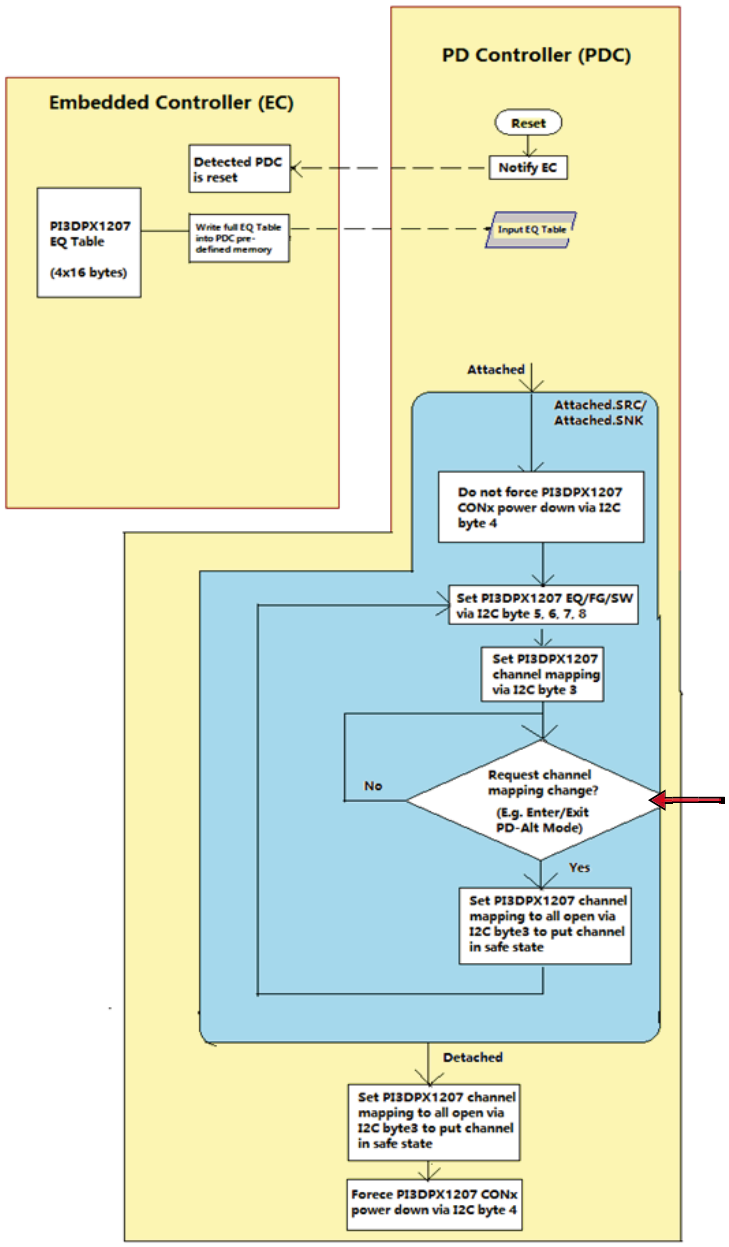


Figure 6-12 Source-side System block diagram with TCPC controller

6.8 Programming Guide

6.8.1 EC and PD Control Flow



HPD Status Update:

if HPD is high,
{
First, PD Controller set IN_HPD pin high.
Then, do below enable display:
{
Enable all DP channels via I2C byte4 bit[7:4]
Enable IN_HPD pin via I2C byte12 bit2
Please refer to pi3dpx1207_hpd() sample code.

}

If HPD is low
{
First, do below to turn-on AUX switch:
{
Keep one DP channel on via I2C byte4 bit[7:4]
Disable IN_HPD pin via I2C byte12 bit2
Please refer to pi3dpx1207_hpd() sample code
}
Then, PD Controller set IN_HPD low.

}

6.8.2 I2C Multi-Byte Read / I2C Block Read using i2c_smbus_read_i2c_block_data()

Example:

```
//Read PI3DPX1207 I2C reg from BYTE0 to BYTE len-1
//return value: no of byte read
int pi3dpx1207_readn( struct i2c_client *client, u8 len, u8 *val)
{

        //Read I2C Byte0 to Byte len-1
        return i2c_smbus_read_i2c_block_data(client, 0, len, val);

}

//Read PI3DPX1207 I2C reg Byte N
//return value: Byte N

int pi3dpx1207_read( struct i2c_client *client, u8 N)
{

        u8 data[N+1];
        int res;

        //Read I2C Byte0 to Byte N
        res = pi3dpx1207_readn(client, N+1, &data);

        if (res >0)
                return data[N];

        return res;
}
```

6.8.3 I2C Multi-Byte Write compared to I2C Block Write using i2c_smbus_write_i2c_block_data()

Example:

```
//Write PI3DPX1207 I2C reg from BYTE0 to BYTE len-1
//return value: no of byte written
int pi3dpx1207_writen( struct i2c_client *client, u8 len, u8 *val)
{

        //Write I2C Byte0 to Byte len-1
        If (len >1)
                return i2c_smbus_write_i2c_block_data(client, *val[0], len, val[1]);
        return i2c_smbus_write_byte(client, *val[0]);
}

//Write PI3DPX1207 I2C reg Byte N
//return value: no of byte written
int pi3dpx1207_write( struct i2c_client *client, u8 N, u8 val)
```

```
{

        u8 data[N+1];
        int res;

        //Read I2C Byte0 to Byte N
        res = pi3dpx1207_readn(client, N+1, &data);

        if (res >0)
        {
                data[N]=val;
                return pi3dpx1207_writen(client, N+1, &data);
        }

        return res;
}
```

6.8.4 Read/Write Byte 3 with OP_MODE 0x03[7:4] to set channel mapping control CONF[3:0]

- 0000 Safe State
- 0001 Safe State
- 0010 4 lane DP1.4 + AUX
- 0011 4 lane DP1.4 + AUX Flipped
- 0100 1 lane USB3.x (AP_CH1)
- 0101 1 lane USB3.x (AP_CH1) Flipped
- 0110 USB3 (AP_CH1) + 2 lane DP1.4 (AP_CH2) + AUX
- 0111 USB3 (AP_CH1) + 2 lane DP1.4 (AP_CH2) + AUX Flipped

Example:

```
//Write PI3DPX1207 Byte 3 to set channel mapping control
//input: confg
//return value: no of byte written
int pi3dpx1207_set_channel_mapping (struct i2c_client *client, u8 confg)
{

        //Read byte 3
        int reg = pi3dpx1207_read(client, 3)

        if (reg < 0)
                return 0;

        reg &= 0x0F;
        reg |= (confg <<4);

        return pi3dpx1207_write(client, 3, reg);
}

/Read PI3DPX1207 Byte 3 to get channel mapping state
//return value: Byte3
```

```
int pi3dpx1207_get_channel_mapping (struct i2c_client *client)
{

        int reg = pi3dpx1207_read(client, 3)

        if (reg > 0)
        {
                reg &= 0xF0;
                return (reg >>4);
        }
        return reg;
}
```

6.8.5 Write Byte 4 with PD_CONx[7:4] and Byte 12 to set HPD state

Example:

```
const u8 eq_fg_sw[8][6] = {"PI3DPX1207 I2C Setting Table"}

//Write PI3DPX1207 Byte 4 to set HPD state
//return value: no of byte written

int pi3dpx1207_hpd(struct i2c_client *client, u8 hpd)
{

u8 data[13];
        //Read byte3
        int confg = pi3dpx1207_get_channel_mapping(client);

        data[0] = 0;
        data[1] = 0;
        data[2] = 0;
        data[3] = confg;

        confg = confg >>4;
        data[4] = eq_fg_sw[conf][0];

        if (hpd)
        {
                if ((confg == 2) || (confg ==3))
                //If HPD is high, power on DP channels by clear bits[7:4] of byte 4.
                        data[4] = eq_fg_sw[conf][0] & 0x0F;
                else if (confg == 6)
                        data[4] = eq_fg_sw[conf][0] & 0xCF;
                else if (confg ==7)
                data[4] = eq_fg_sw[conf][0] & 0x3F;
        }

        data[5] = eq_fg_sw[confg][1];
        data[6] = eq_fg_sw[confg][2];
        data[7] = eq_fg_sw[confg][3];
```

```
	data[8] = eq_fg_sw[confg][4];
	data[9] = 0;
	data[10] = 0;
	data[11] = 0;

	if (hpd)
		//If HPD is high, enable IN_HPD pin by clear bit2 of byte12
		data[12] = eq_fg_sw[confg][5] & 0xFB;
	else
		data[12] = eq_fg_sw[confg][5];

		res = pi3dpx1207_writen(client,13, &data);

	if (res <13)
	return 0; //Fail

	return res;
}
```

6.8.6 Write Byte 4 ~8 and 12 to set EQ/FG/SW and features

Example:

```
const u8 eq_fg_sw[8][6] = {"PI3DPX1207 I2C Setting Table"}

//Write PI3DPX1207 Byte 4 to Byte 8 and Byte 12 to set Equalization, Flat gain, Swing and features.
//return 0 if fail
//input: confg

int pi3dpx1207_set_eq_fg_sw(struct i2c_client *client, u8 confg)
{
	u8 data[13];

	data[0] = 0;
	data[1] = 0;
	data[2] = 0;
	data[3] = 0;
	data[4] = eq_fg_sw[confg][0];
	data[5] = eq_fg_sw[confg][1];
	data[6] = eq_fg_sw[confg][2];
	data[7] = eq_fg_sw[confg][3];
	data[8] = eq_fg_sw[confg][4];
	data[9] = 0;
	data[10] = 0;
	data[11] = 0;
	data[12] = eq_fg_sw[confg][5];

	res = pi3dpx1207_writen(client,13, &data);

	if (res <13)
	return 0; //Fail
```

```
        return res;
}
```

6.8.7 Initialization

const u8 eq_fg_sw[8][6] = {“PI3DPX1207 I2C Setting Table”}

Example:

```
//PI3DPX1207 Init routine
//return 0 if fail
int pi3dpx1207_init(struct i2c_client *client)
{

        return pi3dpx1207_set_eq_fg_sw(struct i2c_client *client, 0)
}
```

6.9 PCB Layout Guideline

6.9.1 General Power and Ground Guideline

To provide a clean power supply for Diodes high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Diodes high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.

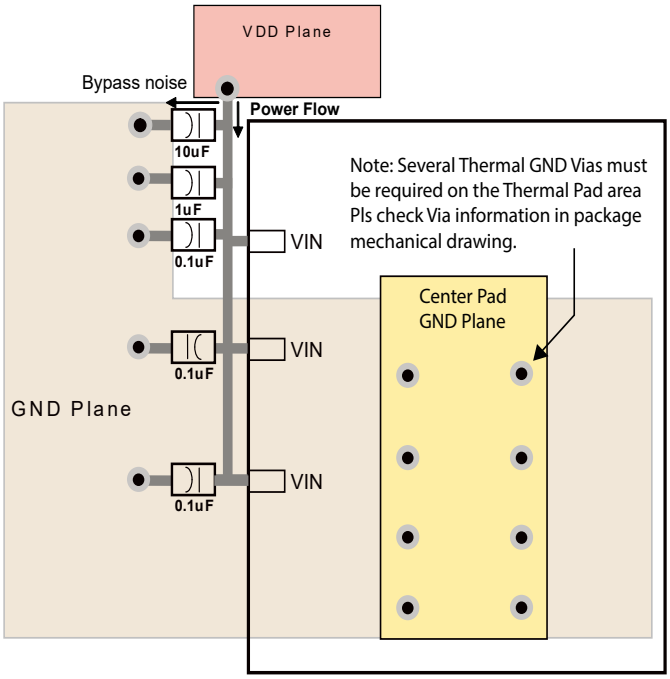


Figure 6-13 Decoupling Capacitor Placement Diagram

6.9.2 High-speed Differential Signal Routing

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.

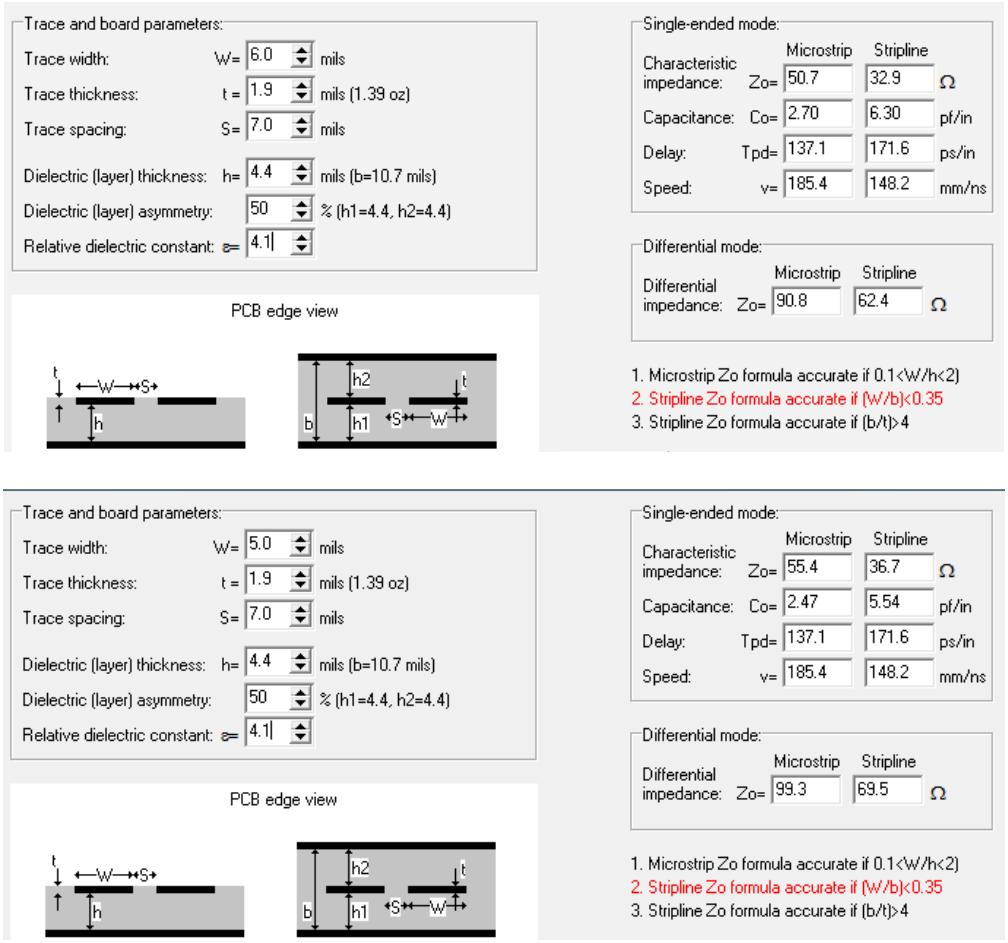


Figure 6-14 Trace Width and Clearance of Micro-strip and Strip-line

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

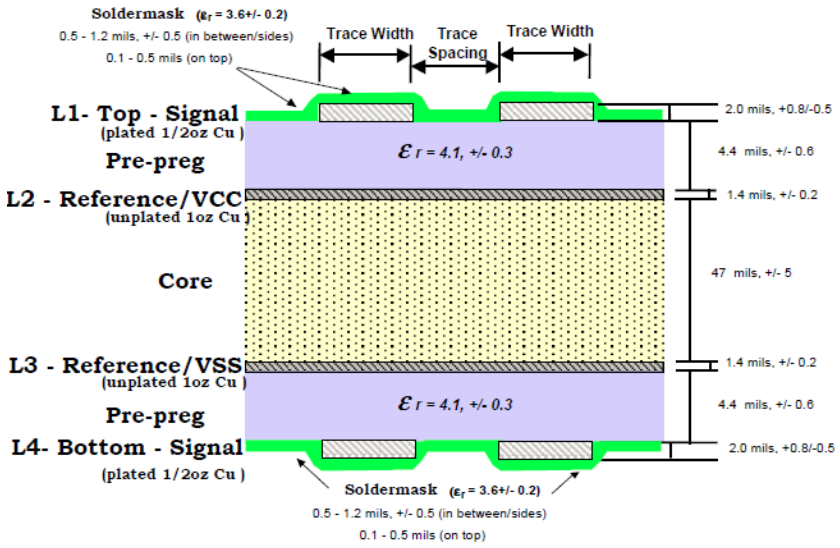


Figure 6-15 4-Layer PCB Stack-up Example

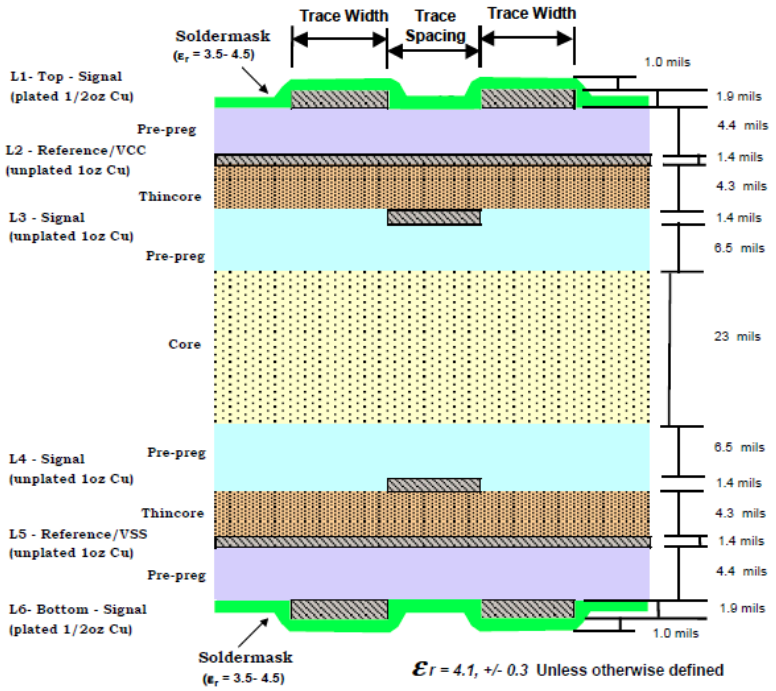


Figure 6-16 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.

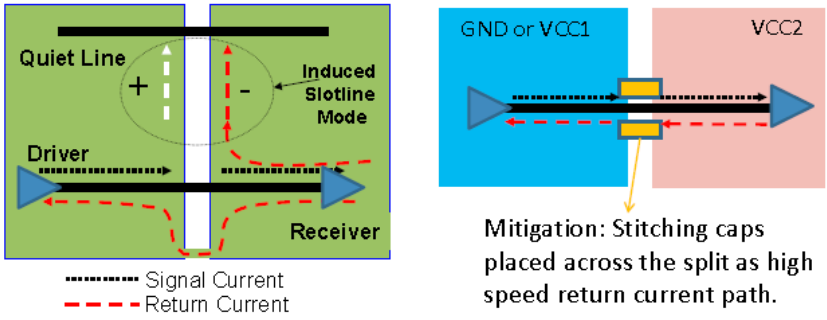


Figure 6-17 Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

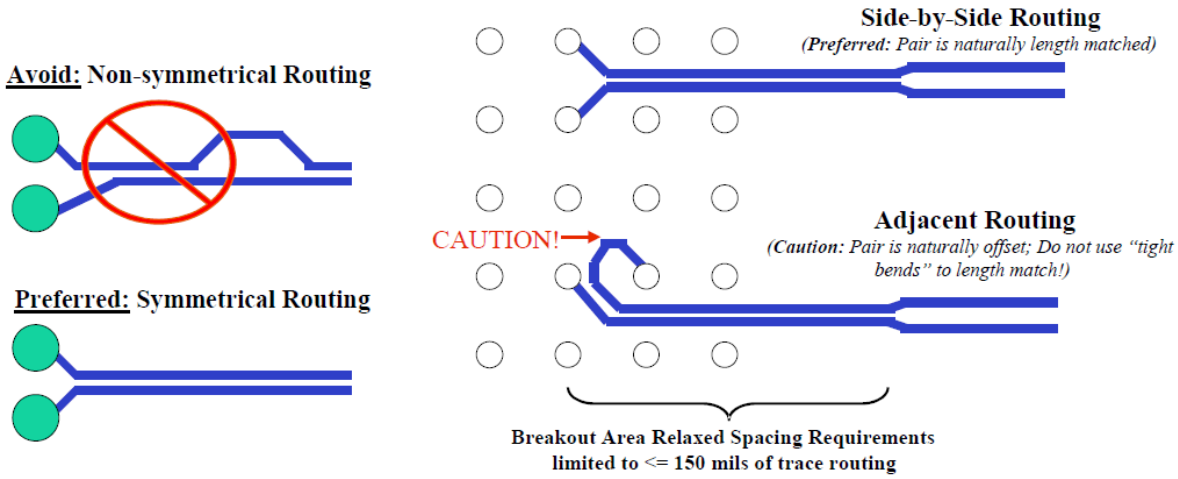


Figure 6-18 Layout Guidance of Matched Differential Pair

- For minimal crosstalk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles α should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.

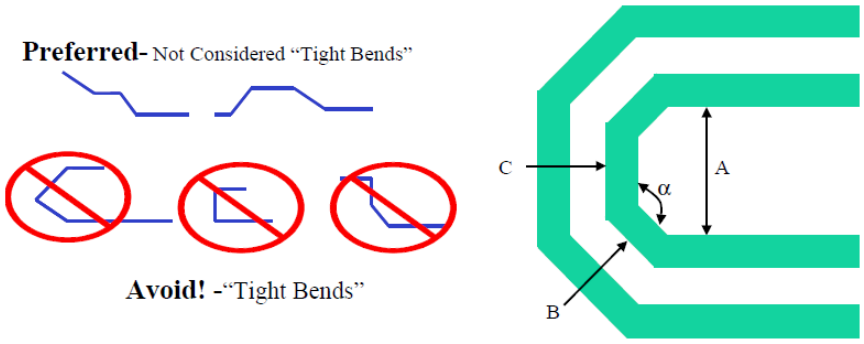


Figure 6-19 Layout Guidance of Bends

- Stub creation should be avoided when placing shunt components on a differential pair.

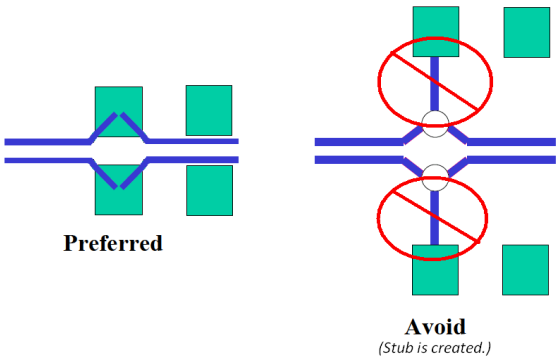


Figure 6-20 Layout Guidance of Shunt Component

- Placement of series components on a differential pair should be symmetrical.

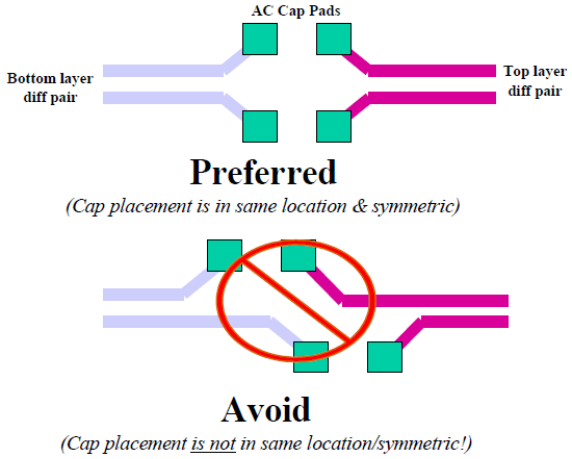


Figure 6-21 Layout Guidance of Series Component

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.

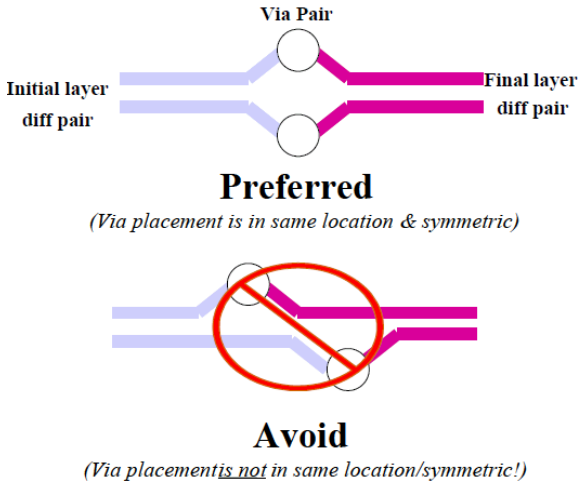


Figure 6-22 Layout Guidance of Stitching Via

6.10 DP/USB Compliance Test

6.10.1 DP1.4 Compliance Test Report

Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Test Specification	1.4
Lane	4 Lanes
SSC	Disabled
Test Session Details	
DisplayPort Test Controller	UnigrafDPTC
Fixture Type	Other
Infiniium SW Version	05.70.00901
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY54410104
Application SW Version	3.52.0001
Debug Mode Used	No
Compliance Limits (official)	DisplayPort Compliance Test Specification Version 1.4 Official Test Limit
Probe (Channel 1)	Model: N2801A Serial: US54094067 Head: N5444A Atten: Calibrated (9 JAN 2017 10:16:47), Using Cal Atten (5.7433E+000) Skew: Calibrated (9 JAN 2017 10:17:05), Using Cal Skew
Probe (Channel 2)	Model: N2801A Serial: US54094054 Head: N5444A Atten: Calibrated (9 JAN 2017 10:18:00), Using Cal Atten (5.5352E+000) Skew: Calibrated (9 JAN 2017 10:18:15), Using Cal Skew
Probe (Channel 3)	Model: N2801A Serial: US54094059 Head: N5444A Atten: Calibrated (9 JAN 2017 10:19:03), Using Cal Atten (5.7151E+000) Skew: Calibrated (9 JAN 2017 10:19:16), Using Cal Skew
Probe (Channel 4)	Model: N2801A Serial: US54094057 Head: N5444A Atten: Calibrated (9 JAN 2017 10:20:00), Using Cal Atten (5.5492E+000) Skew: Calibrated (9 JAN 2017 10:20:11), Using Cal Skew
Last Test Date	2017-01-12 16:19:05 UTC +08:00

Figure 6-23 DisplayPort Compliance Test Report

6.10.2 CTS Testing Trace loss information

DP FR4 trace	0 in	6 in	12 in	18 in	24 in	30 in	36 in
Insertion loss @ 8.1Gbps	-8.15 dB	-11.52 dB	-14.88 dB	-17.60 dB	-19.94 dB	-22.92 dB	-28.62 dB

6.10.3 USB3 Compliance Test Report

Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
10GTransFunc	C:\Users\Public\Documents\Infiniium\Apps\USB3Test\TransferFunctions\SSGen2_TxComp12p2dB_Embedding.tf4
5GTransFunc	C:\Users\Public\Documents\Infiniium\Apps\USB3Test\TransferFunctions\U7242A_Deembed__USB3_TX_Host_Channel.tf
AdcMode	AUTO
DC Gain	0
Reference Clock	SSC
Device	Host
Device ID:	Device 1
Test Session Details	
Infiniium SW Version	06.00.00828
Infiniium Model Number	MSOV334A
Infiniium Serial Number	MY55430101
Application SW Version	3.20
Debug Mode Used	No
Compliance Limits (official)	USB 3.1 Specification version 1.0
Last Test Date	2017-05-09 08:35:14 UTC +08:00

Summary of Results

Test Statistics	
Failed	0
Passed	13
Total	13

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	Deemphasis	-3.449875 dB	32.5 %	-4.100000 dB <= VALUE <= -2.100000 dB
✓	0	1	Preshoot	2.5 dB	35.0 %	1.2 dB <= VALUE <= 3.2 dB
✓	0	1	10G TSSC-Freq-Dev-Min	-4.499636 kppm	50.0 %	-5.300000 kppm <= VALUE <= -3.700000 kppm
✓	0	1	10G TSSC-Freq-Dev-Max	-18.142 ppm	47.0 %	TSSCMin ppm <= VALUE <= TSSCMax ppm
✓	0	1	10G SSC Modulation Rate	30.989320 kHz	33.0 %	30.000000 kHz <= VALUE <= 33.000000 kHz
✓	0	1	10G SSC df/dt	429.5 ppm/us	65.6 %	VALUE <= 1.2500 kppm/us
✓	0	1	10G Random Jitter (CTLE ON)	441 fs	55.9 %	VALUE <= 1.000 ps
✓	0	1	10G Short Channel Template Test	0.000	100.0 %	VALUE = 0.000
✓	0	1	10G Short Channel Extrapolated Eye Height	299.9 mV	328.4 %	VALUE >= 70.0 mV
✓	0	1	10G Short Channel Minimum Eye Width	65.4268 ps	36.3 %	VALUE >= 48.0000 ps
✓	0	1	10G Far End Template Test (CTLE ON)	0.000	100.0 %	VALUE = 0.000
✓	0	1	Extrapolated Eye Height	110.0 mV	57.1 %	VALUE >= 70.0 mV
✓	0	1	Minimum Eye Width	66.3510 ps	38.2 %	VALUE >= 48.0000 ps

Figure 6-24 USB3 Compliance Test Report

7. Mechanical/Packaging Information

7.1 Mechanical Outline

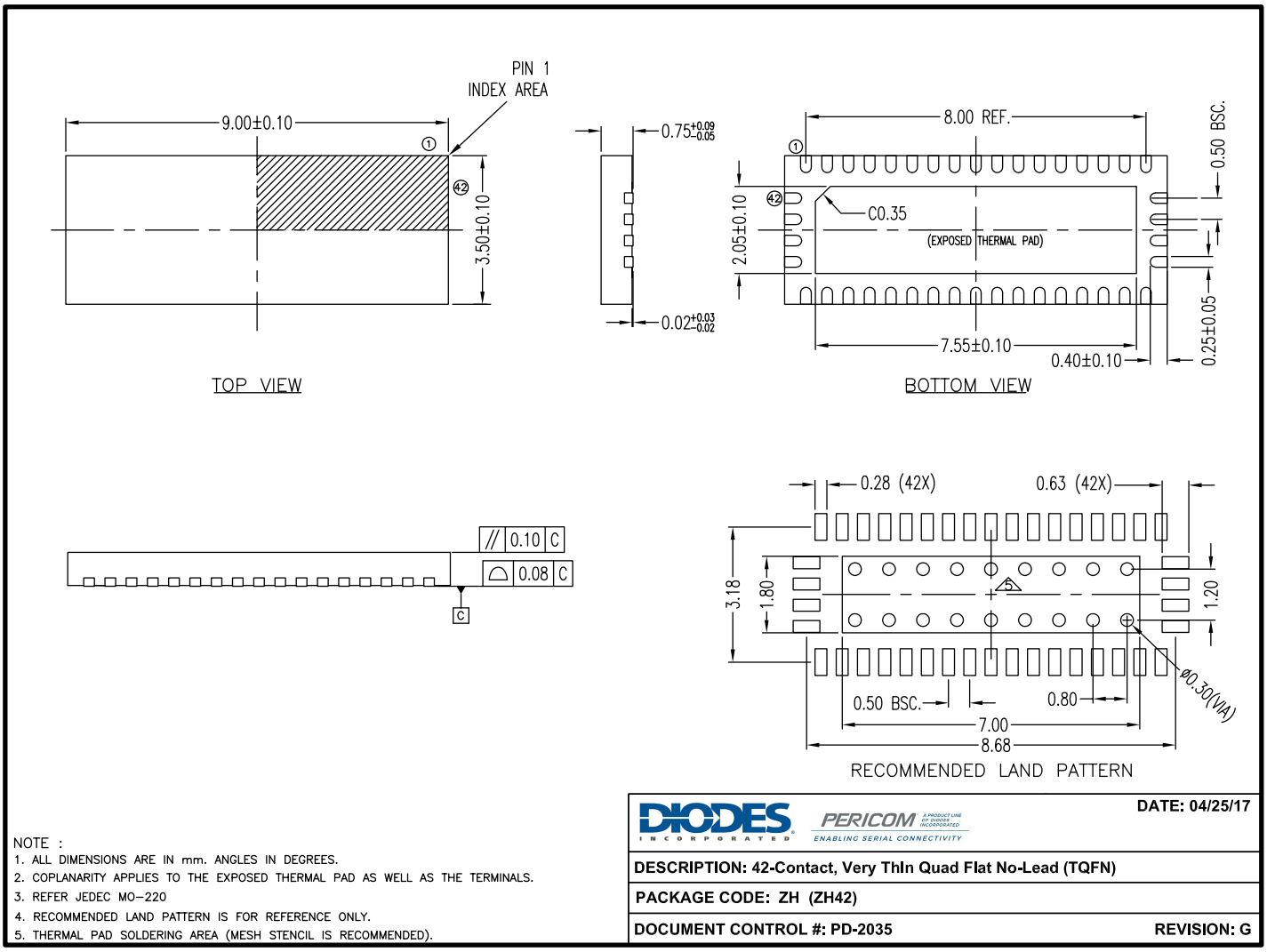


Figure 7-1 PI3DPX1207B (42-pin) Package Mechanical Dimension

7.2 Part Marking Information

Our standard product mark follows our standard part number ordering information, except for those products with a speed letter code. The speed letter code mark is placed after the package code letter, rather than after the device number as it is ordered. After electrical test screening and speed binning has been completed, we then perform an “add mark” operation which places the speed code letter at the end of the complete part number.

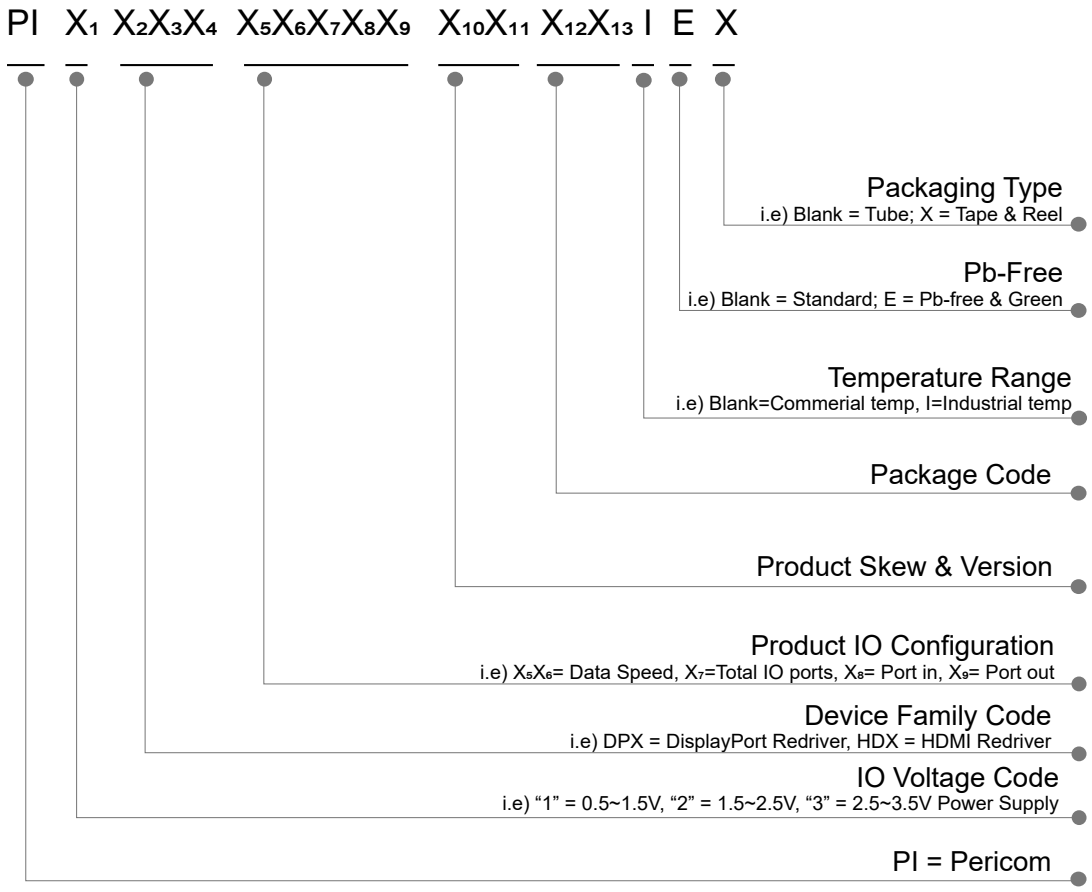


Figure 7-2 Part naming information

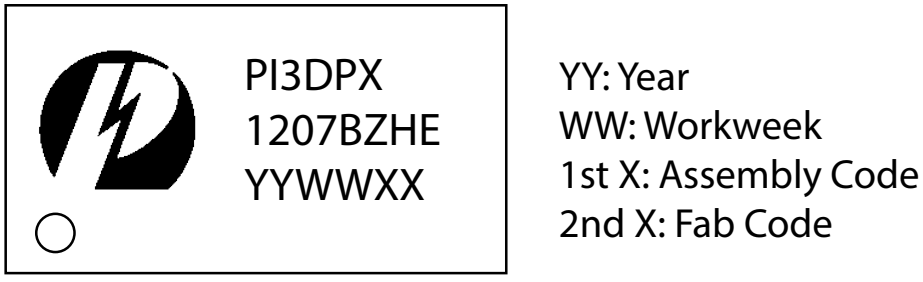


Figure 7-3 Part marking information

7.3 Tape & Reel Materials and Design

Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 10^6Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

Cover Tape

Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is 10^7Ohm/Sq. Minimum to 10^{11}Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

Reel

The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 4) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 10^7Ohm/sq. minimum to 10^{11}Ohm/sq. max.

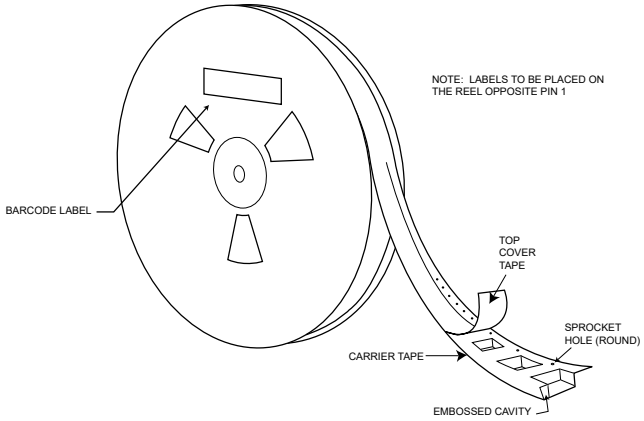


Figure 7-4 Tape & Reel label information

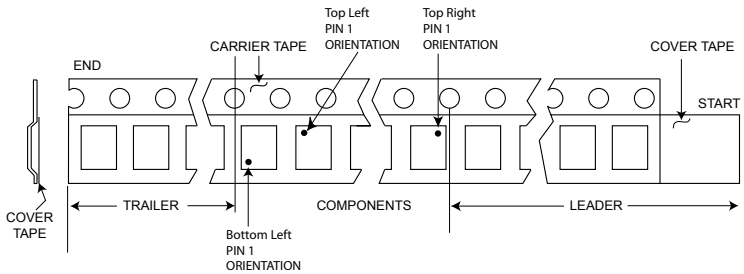


Figure 7-5 Tape leader and trailer pin 1 orientations

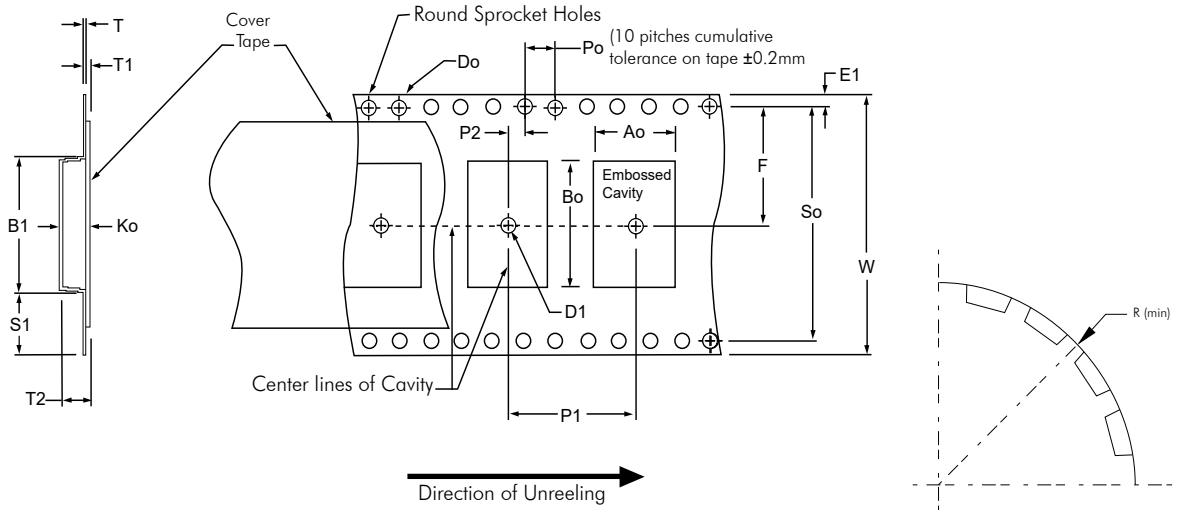


Figure 7-6 Standard embossed carrier tape dimensions

Table 7-1. Constant Dimensions

Tape Size	D_0	D_1 (Min)	E_1	P_0	P_2	R (See Note 2)	S_1 (Min)	T (Max)	T_1 (Max)
8mm	1.5 +0.1 -0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5				30			
16mm					2.0 ± 0.1				
24mm									
32mm		2.0				50	N/A (See Note 3)		
44mm					2.0 ± 0.15				

Table 7-2. Variable Dimensions

Tape Size	P_1	B_1 (Max)	E_2 (Min)	F	So	T_2 (Max.)	W (Max)	A_0, B_0, & K_0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information)	4.35	6.25	3.5 ± 0.05	N/A (see note 4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1		12.0	24.3	
32mm		23.0	N/A	14.2 ± 0.1	28.4± 0.1		32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

NOTES:
1. A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do≥S1.
4. So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

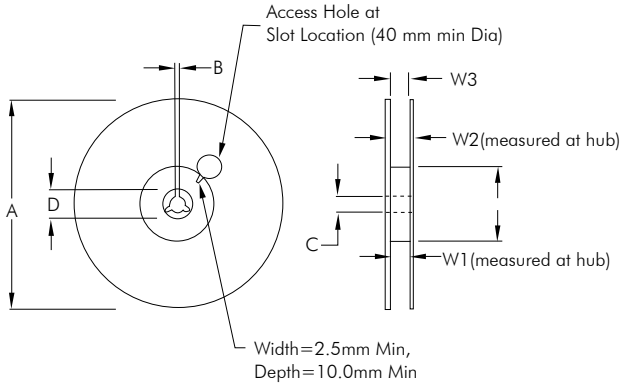


Table 7-3. Reel dimensions by tape size

Tape Size	A	N (Min) See Note A	W_1	W_2(Max)	W_3	B (Min)	C	D (Min)
8mm	178 ±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

NOTE:
A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

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