

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(on)}$ max	I_D $T_A = +25^\circ C$
Q1 N-Channel	60V	40mΩ @ $V_{GS} = 10V$	6.5 A
		55mΩ @ $V_{GS} = 4.5V$	5.6 A
Q2 P-Channel	-60V	110mΩ @ $V_{GS} = -10V$	-3.9 A
		130mΩ @ $V_{GS} = -4.5V$	-3.6 A

Description and Applications

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

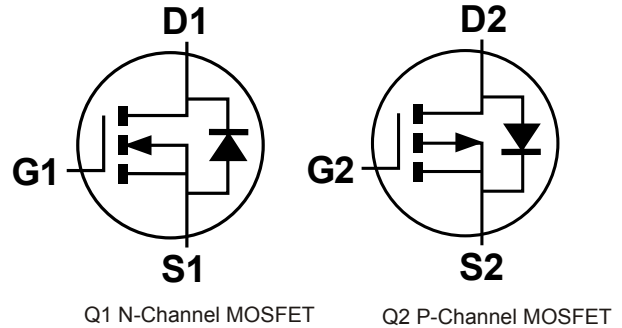
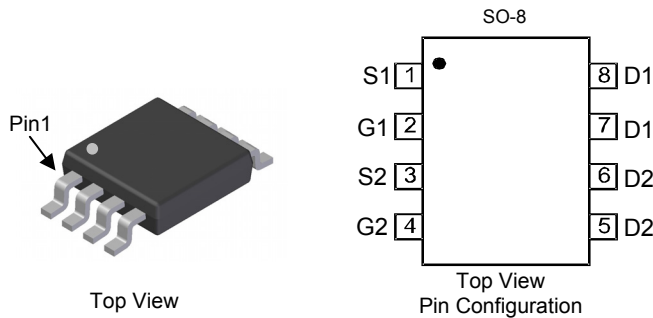
- DC-DC Converters
- Power Management Functions
- Backlighting

Features and Benefits

- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Tin Finish annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.074 grams (approximate)

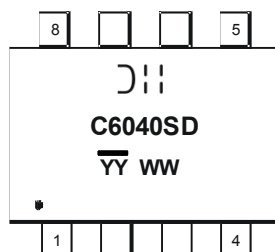
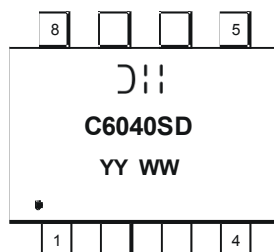


Ordering Information (Note 4)

Part Number	Case	Packaging
DMC6040SSD-13	SO-8	2,500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information


Chengdu A/T Site

Shanghai A/T Site

- DII = Manufacturer's Marking
- C6040SD = Product Type Marking Code
- YYWW = Date Code Marking
- YY or YY = Year (ex: 14= 2014)
- WW = Week (01 - 53)
- YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)
- YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Q1	Q2	Units
Drain-Source Voltage			V_{DSS}	60	-60	V
Gate-Source Voltage			V_{GSS}	± 20	± 20	V
Continuous Drain Current (Note 6) $V_{GS} = -10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	5.1 4.1	-3.1 -2.5	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	6.5 5.2	-3.9 -3.1	A
Maximum Body Diode Forward Current (Note 6)			I_S	2.1	-2.1	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	28	-19	A
Avalanche Current (Note 7) $L = 0.1\text{mH}$			I_{AS}	17.2	-17.6	A
Avalanche Energy (Note 7) $L = 0.1\text{mH}$			E_{AS}	14.7	15.4	mJ

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	P_D	1.24	W
	$T_A = +70^\circ\text{C}$		0.8	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	101	$^\circ\text{C/W}$
	$t < 10\text{s}$		61	
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	P_D	1.56	W
	$T_A = +70^\circ\text{C}$		1.0	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	80	$^\circ\text{C/W}$
	$t < 10\text{s}$		49	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	14.7	$^\circ\text{C}$
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics N-Channel Q1 (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	1	—	3	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	33	40	m Ω	$V_{GS} = 10\text{V}, I_D = 8\text{A}$
		—	37	55		$V_{GS} = 4.5\text{V}, I_D = 5\text{A}$
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	$V_{GS} = 0\text{V}, I_S = 1\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1130	—	pF	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	69	—		
Reverse Transfer Capacitance	C_{rss}	—	42	—		
Gate Resistance	R_G	—	1.7	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	—	20.8	—	nC	$V_{DS} = 30\text{V}, I_D = 4.3\text{A}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	9.4	—		
Gate-Source Charge	Q_{gs}	—	3.3	—		
Gate-Drain Charge	Q_{gd}	—	3.0	—		
Turn-On Delay Time	$t_{D(on)}$	—	3.6	—	nS	$V_{GS} = 10\text{V}, V_{DD} = 30\text{V}, R_G = 6\Omega, I_D = 4.3\text{A}$
Turn-On Rise Time	t_r	—	1.8	—		
Turn-Off Delay Time	$t_{D(off)}$	—	20.1	—		
Turn-Off Fall Time	t_f	—	4.3	—		
Body Diode Reverse Recovery Time	t_{rr}	—	14.2	—	nS	$I_S = 4.3\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Body Diode Reverse Recovery Charge	Q_{rr}	—	7.5	—	nC	$I_S = 4.3\text{A}, di/dt = 100\text{A}/\mu\text{s}$

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 - UIS in production with $L = 0.1\text{mH}$, starting $T_A = +25^\circ\text{C}$.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

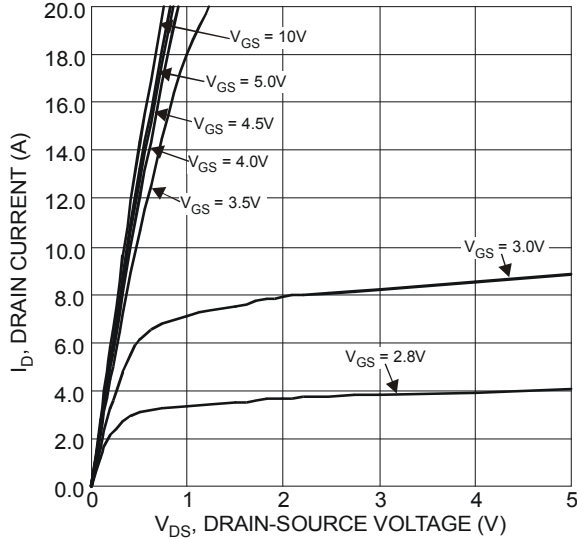


Figure 1 Typical Output Characteristics

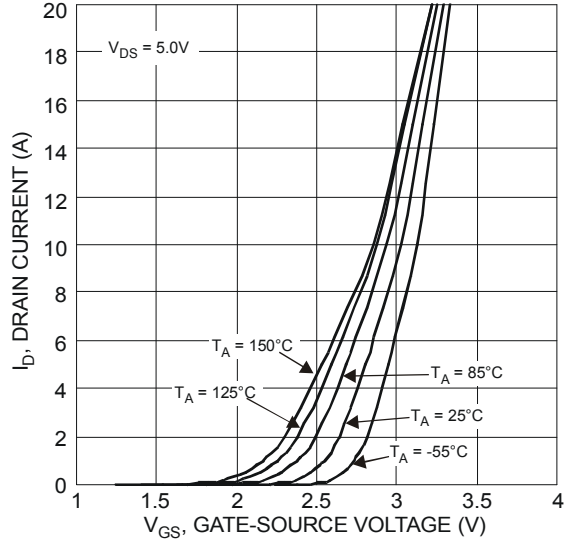


Figure 2 Typical Transfer Characteristics

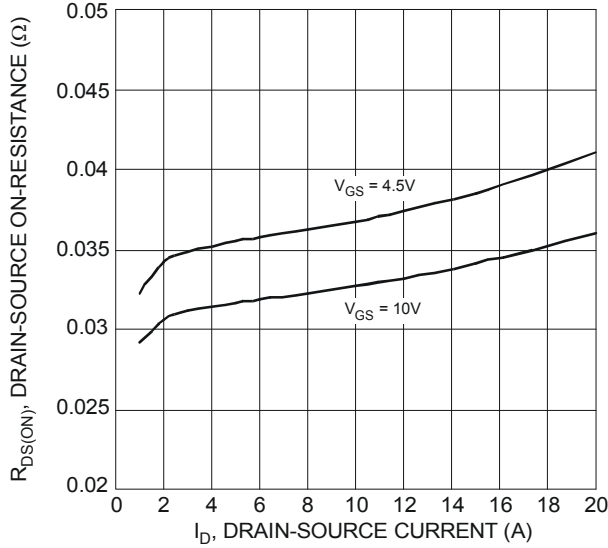


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

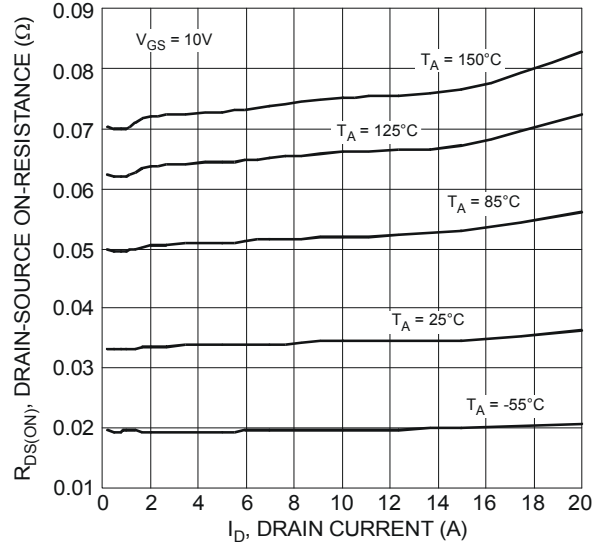


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

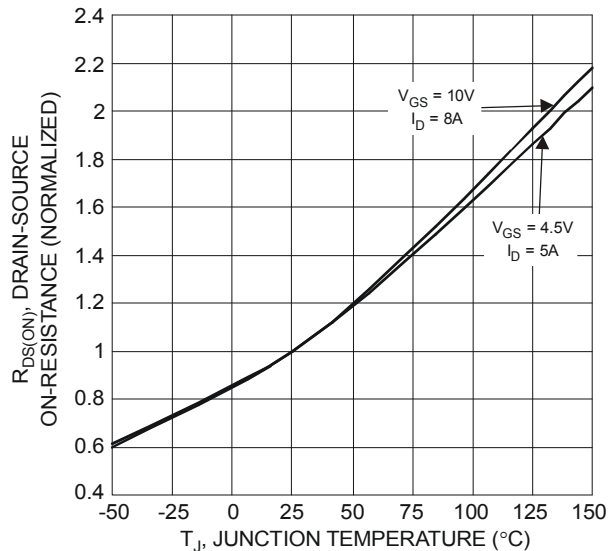


Figure 5 On-Resistance Variation with Temperature

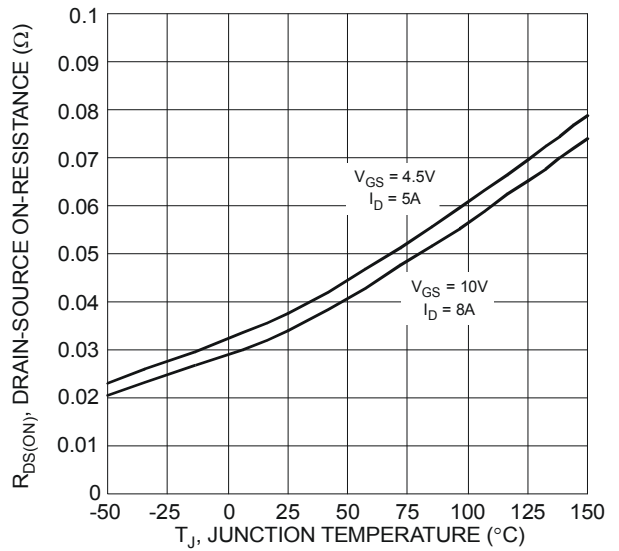


Figure 6 On-Resistance Variation with Temperature

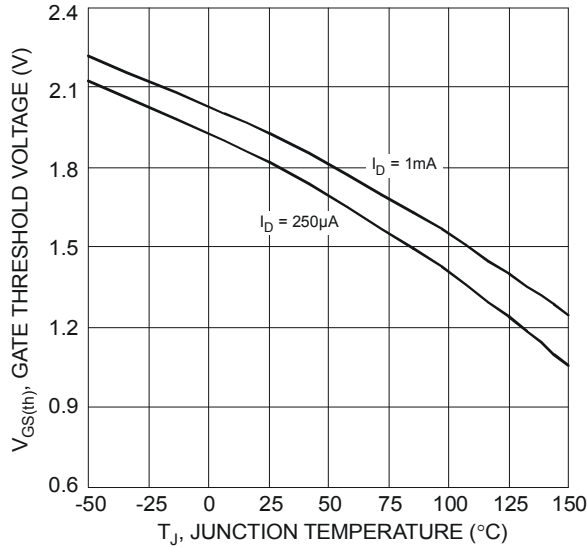


Figure 7 Gate Threshold Variation vs. Ambient Temperature

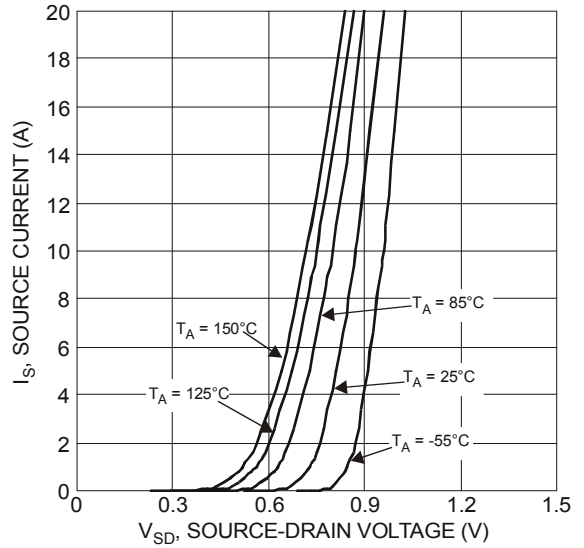


Figure 8 Diode Forward Voltage vs. Current

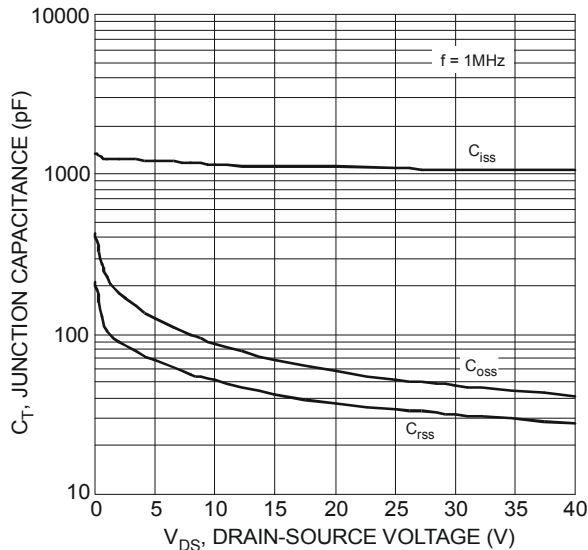


Figure 9 Typical Junction Capacitance

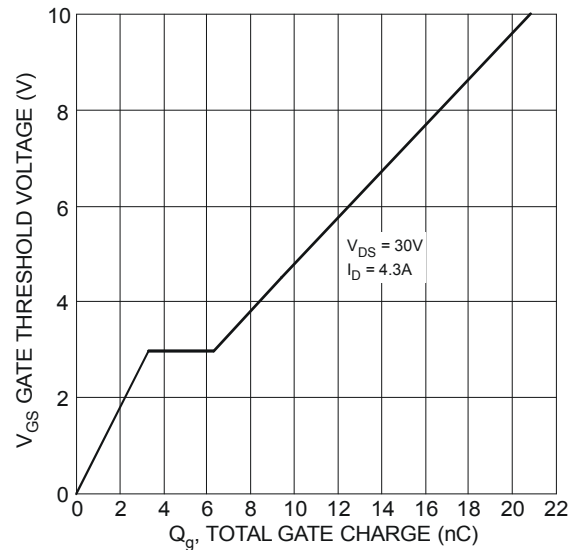


Figure 10 Gate Charge

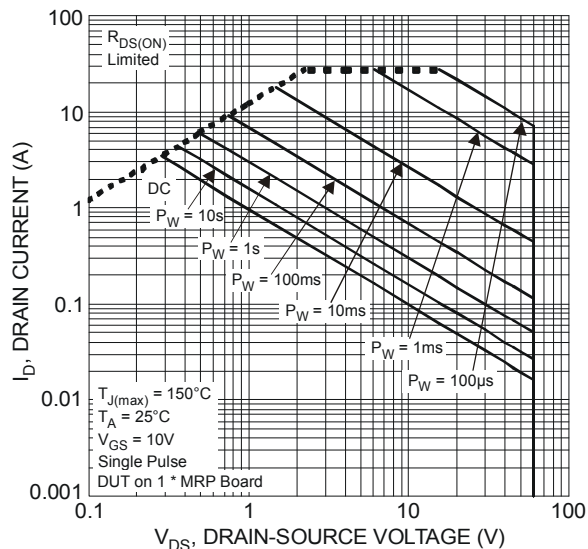
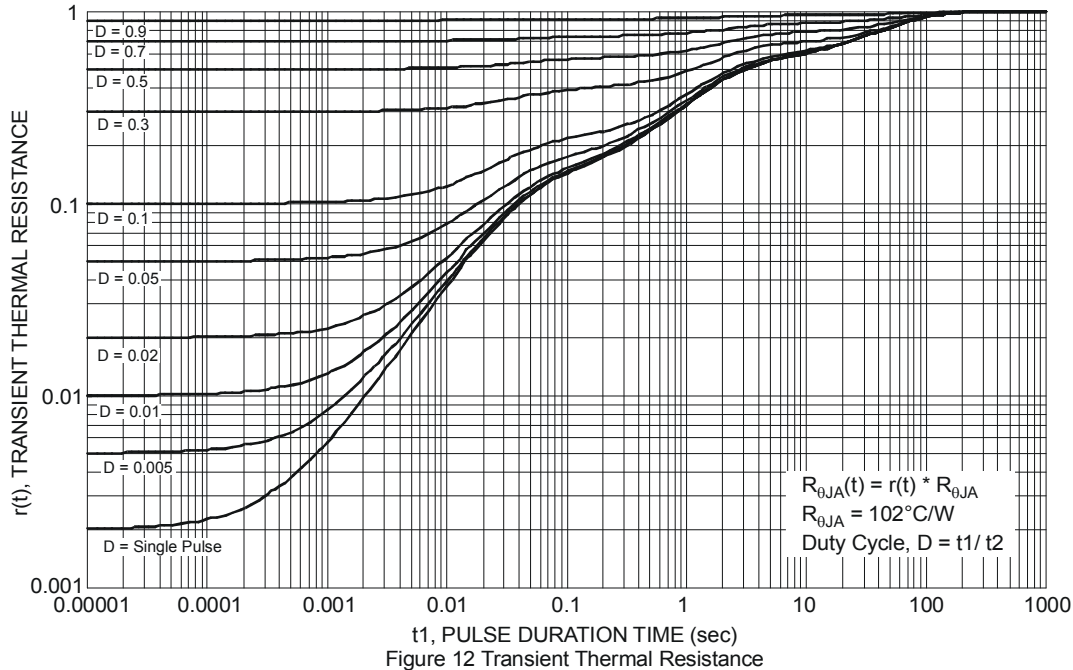


Figure 11 SOA, Safe Operation Area



Electrical Characteristics P-Channel Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	-60	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-1	μA	V _{DS} = -48V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	100	nA	V _{GS} = ±16V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(th)}	-1	—	-3	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(on)}	—	86	110	mΩ	V _{GS} = -10V, I _D = -4.5A
		—	98	130		V _{GS} = -4.5V, I _D = -3.5A
Diode Forward Voltage	V _{SD}	—	-0.7	-1.2	V	V _{GS} = 0V, I _S = -1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	1030	—	pF	V _{DS} = -30V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	49.1	—		
Reverse Transfer Capacitance	C _{rss}	—	38.7	—		
Gate Resistance	R _G	—	13.6	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge (V _{GS} = -4.5V)	Q _g	—	9.5	—	nC	V _{DS} = -30V, I _D = -5A
Total Gate Charge (V _{GS} = -10V)	Q _g	—	19.4	—		
Gate-Source Charge	Q _{gs}	—	2.3	—		
Gate-Drain Charge	Q _{gd}	—	3.6	—		
Turn-On Delay Time	t _{D(on)}	—	3.7	—	nS	V _{GS} = -10V, V _{DS} = -30V, R _{GEN} = 6Ω, I _D = -5A
Turn-On Rise Time	t _r	—	6.3	—		
Turn-Off Delay Time	t _{D(off)}	—	58.7	—		
Turn-Off Fall Time	t _f	—	26.1	—		
Body Diode Reverse Recovery Time	t _{rr}	—	14.85	—	nS	I _S = -5A, di/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q _{rr}	—	8.8	—	nC	I _S = -5A, di/dt = 100A/μs

- Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 7. UIS in production with L = 0.1mH, starting T_A = +25°C.
 8. Short duration pulse test used to minimize self-heating effect.
 9. Guaranteed by design. Not subject to product testing.

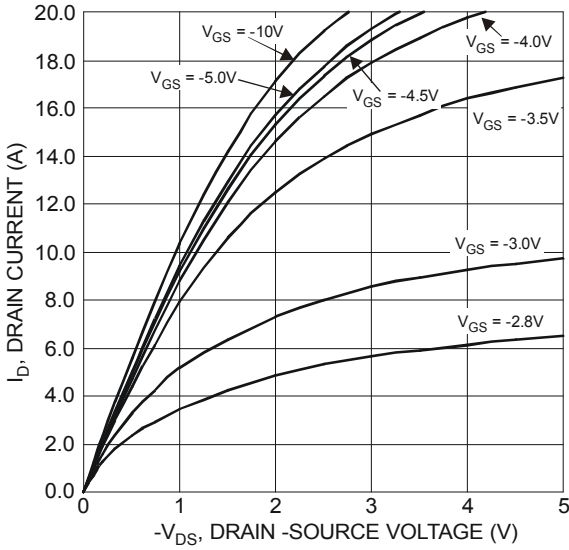


Figure 13 Typical Output Characteristics

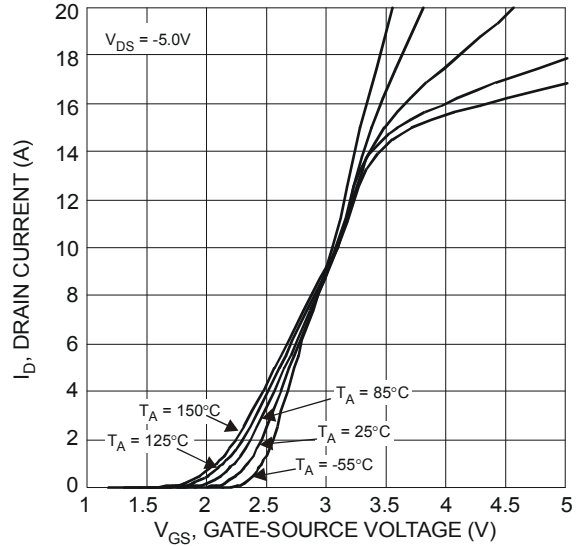


Figure 14 Typical Transfer Characteristics

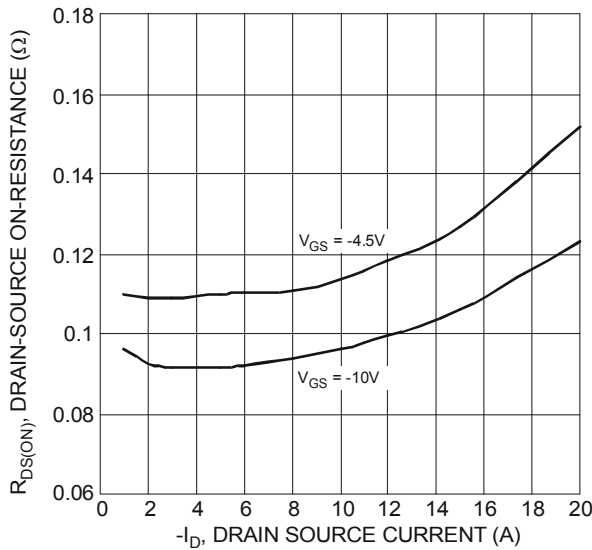


Figure 15 Typical On-Resistance vs. Drain Current and Gate Voltage

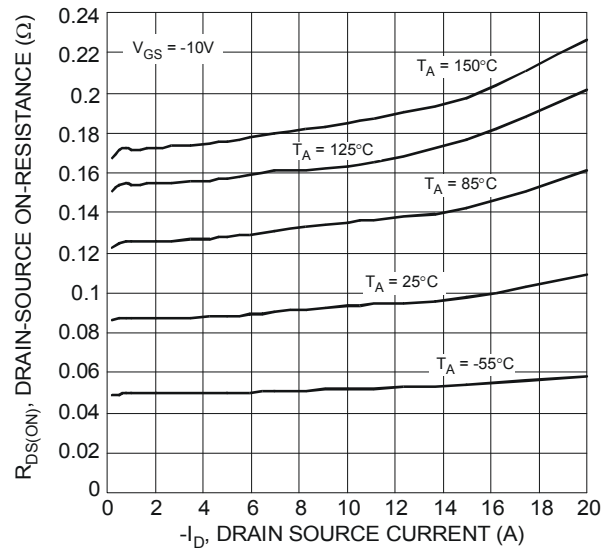


Figure 16 Typical On-Resistance vs. Drain Current and Temperature

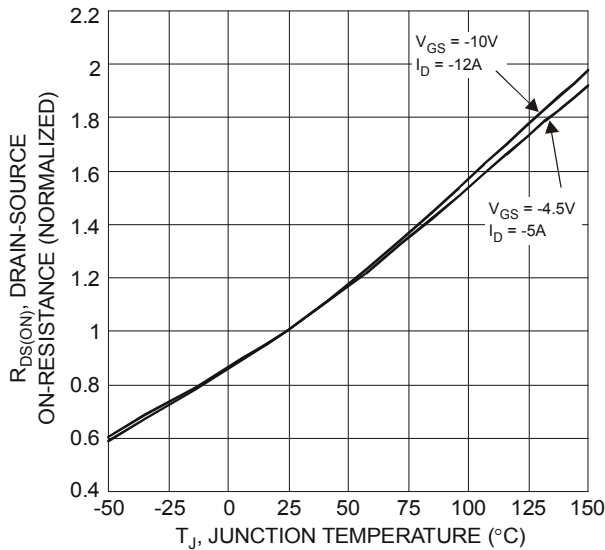


Fig. 17 On-Resistance Variation with Temperature

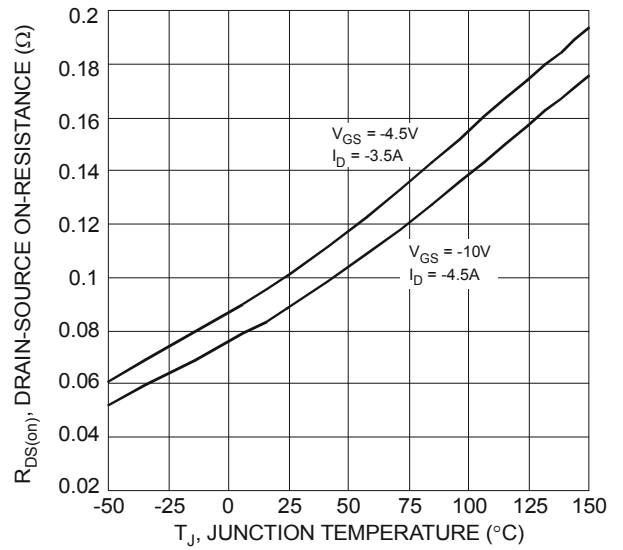


Figure 18 On-Resistance Variation with Temperature

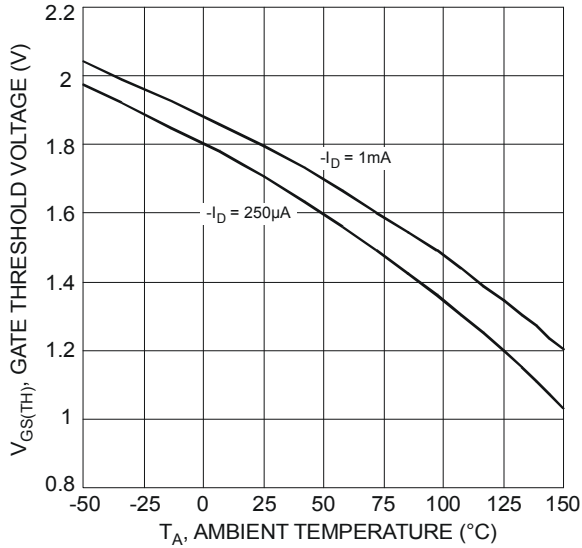


Figure 19 Gate Threshold Variation vs. Ambient Temperature

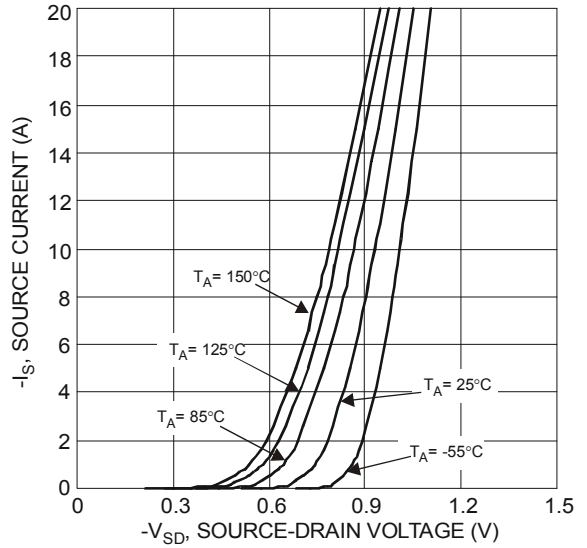


Figure 20 Diode Forward Voltage vs. Current

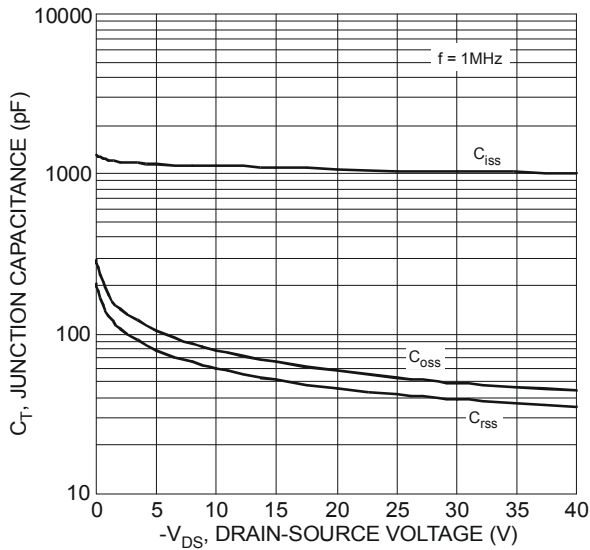


Figure 21 Typical Junction Capacitance

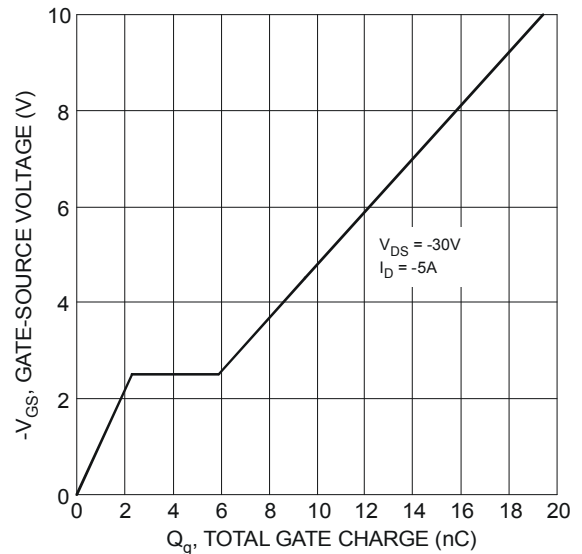


Figure 22 Gate-Charge Characteristics

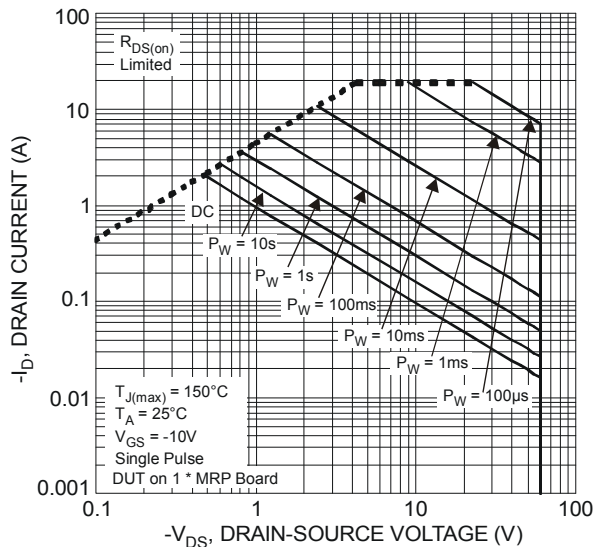
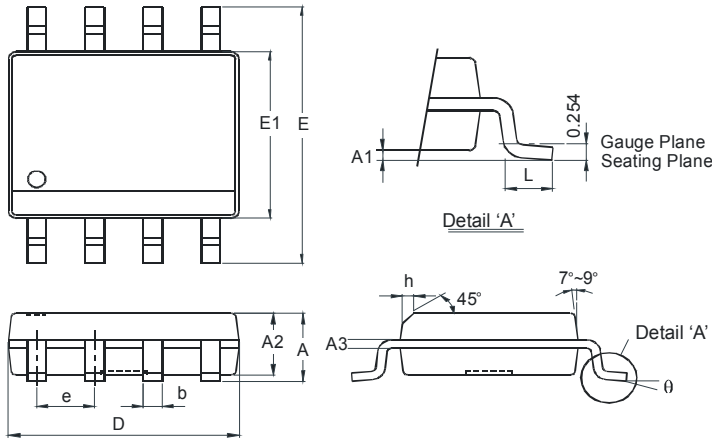


Figure 23 SOA, Safe Operation Area

Package Outline Dimensions

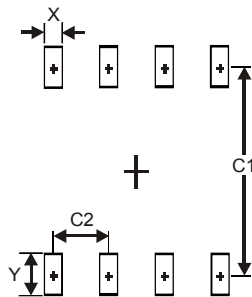
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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