

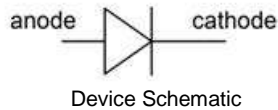
## Product Summary

$V_{RRM}$ (V)	$I_O$ (A)	$V_F$ Max (V)	$I_R$ Max ( $\mu$ A)
40	2.0	0.53	150

## Description and Applications

The SDM2U40CSP is a 40-volt 2A Schottky Barrier Rectifier that is optimized for low forward voltage drop and low leakage current, housed in a compact chip scale package (CSP) that occupies only 1.28mm<sup>2</sup> board space with low profile. The low thermal resistance enables designers to meet design challenges of increasing efficiency whilst at the same time reducing board space. It is ideally suited for use in portable applications as a:

- Blocking Diode
- Boost Diode
- Switching Diode
- Reverse Protection Diode

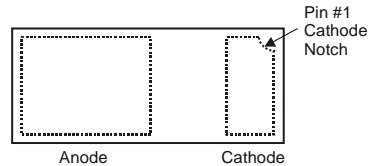


## Features and Benefits

- Low forward voltage ( $V_F$ ) minimizes conduction losses and improves efficiency.
- Reduced high temperature reverse leakage; Increased reliability against thermal runaway failure in high temperature operation.
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

## Mechanical Data

- Case: X3-WLB1608-2
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: NiAu Bump. Solderable per MIL-STD-202, Method 208 (e4)
- Polarity: Cathode Dot
- Weight: 0.001 grams (Approximate)

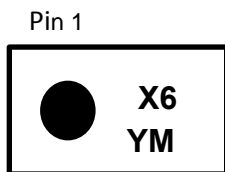


## Ordering Information (Note 4)

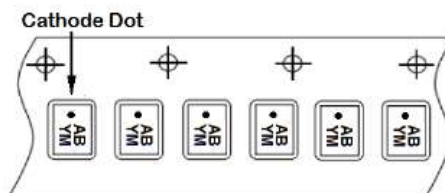
Part Number	Case	Packaging
SDM2U40CSP-7B	X3-WLB1608-2	10,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

## Marking Information



X6= Product Type Marking Code  
 YM=Date Code Marking  
 Y or  $\bar{Y}$ = Year (ex: F = 2018)  
 M=Month (ex: 9= September)  
 Dot Denotes Cathode Pin



### Date Code Key

Year	2014	2015	2016	2017	2018	2019	2020
Code	B	C	D	E	F	G	H

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Single phase, half wave, 60Hz, resistive or inductive load.  
For capacitive load, derate current by 20%.

Characteristic	Symbol	Value	Unit
Peak Repetitive Reverse Voltage	V <sub>RRM</sub>	40	V
Average Rectified Output Current	I <sub>O</sub>	2.0	A
Non-Repetitive Peak Forward Surge Current 8.3ms Single Half Sine-Wave Superimposed on Rated Load	I <sub>FSM</sub>	28	A

**Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Typical Thermal Resistance Junction to Ambient (Note 5)	R <sub>θJA</sub>	135	°C/W
Typical Thermal Resistance Junction to Ambient (Note 6)	R <sub>θJA</sub>	65	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Forward Voltage Drop	V <sub>F</sub>	—	0.39	0.44	V	I <sub>F</sub> = 1.0A, T <sub>J</sub> = +25°C
		—	0.48	0.53		I <sub>F</sub> = 2.0A, T <sub>J</sub> = +25°C
Reverse Current (Note 7)	I <sub>R</sub>	—	—	150	μA	V <sub>R</sub> = 40V, T <sub>J</sub> = +25°C
Junction Capacitance	C <sub>T</sub>	—	85	—	pF	V <sub>R</sub> = 5V, f = 1.0MHz

- Notes:
5. Device mounted on FR-4 PCB, 2oz. Copper, minimum recommended pad layout per <http://www.diodes.com/package-outlines.html>.
  6. Device mounted on 1inch sq. copper pad, 2oz.
  7. Short duration pulse test used to minimize self-heating effect.

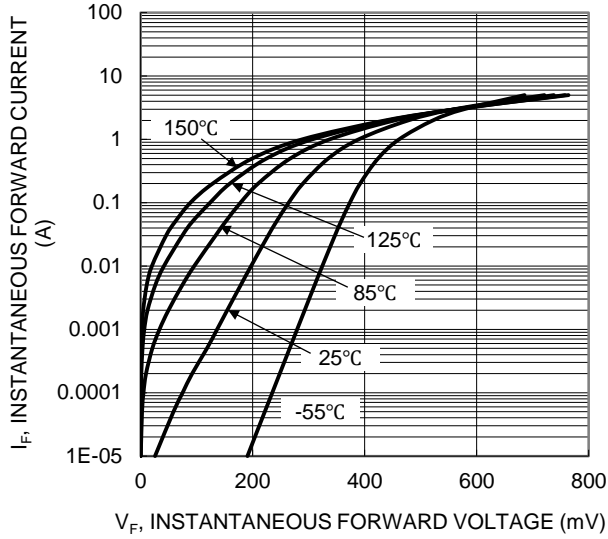


Figure 1. Typical Forward Characteristics

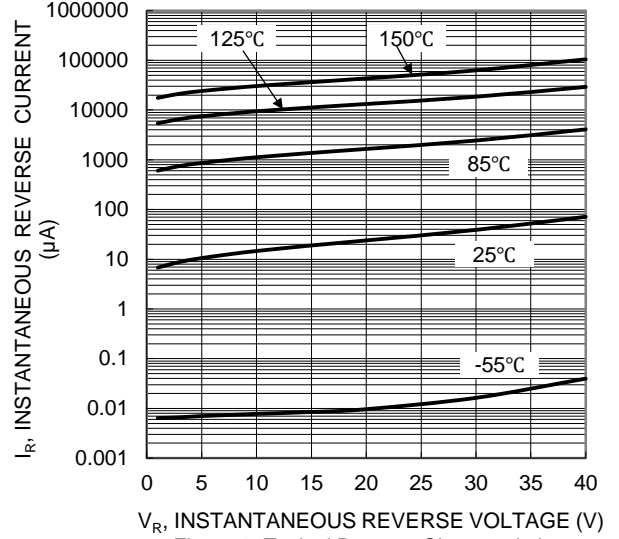


Figure 2. Typical Reverse Characteristics

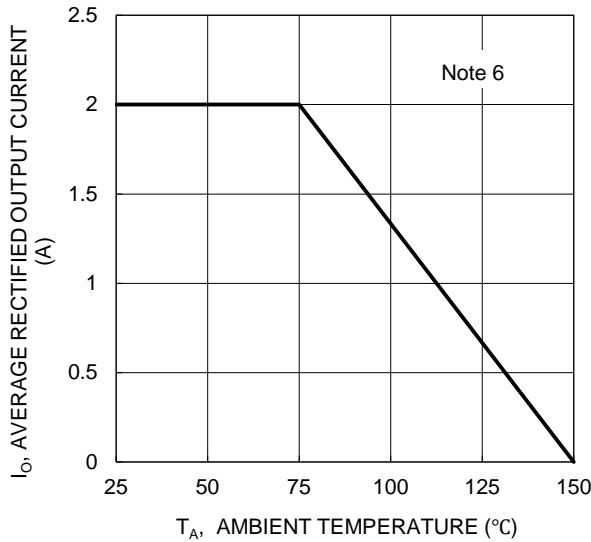


Figure 3. DC Forward Current Derating Curve

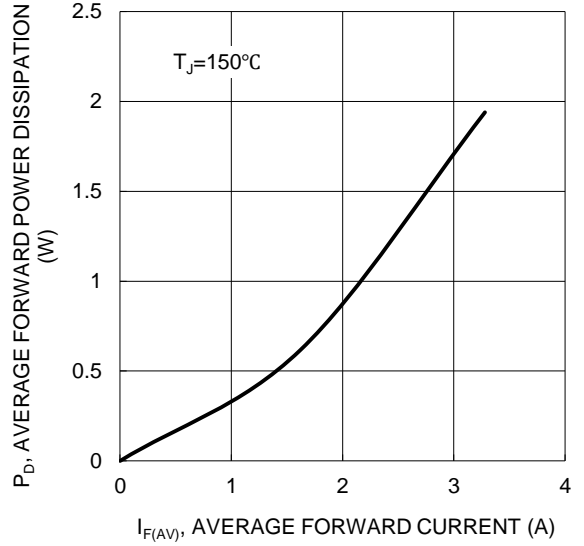


Figure 4. Forward Power Dissipation

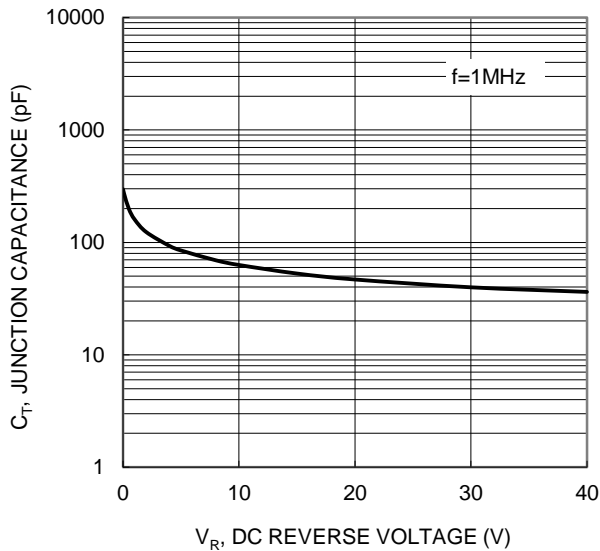
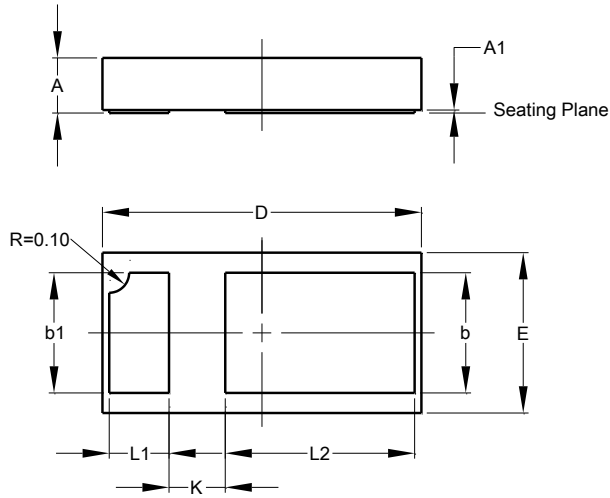


Figure 5. Typical Junction Capacitance

**Package Outline Dimensions** (Note 8)

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**X3-WLB1608-2**



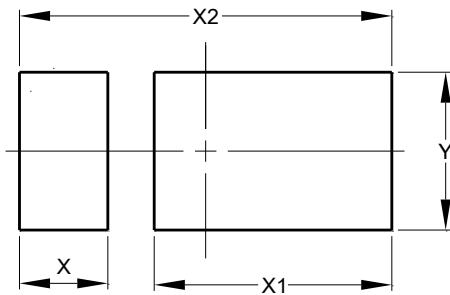
X3-WLB1608-2			
Dim	Min	Max	Typ
A	0.250	0.300	0.275
A1	-	0.015	-
b	-	-	0.600
b1	-	-	0.600
D	1.57	1.63	1.60
E	0.77	0.83	0.80
K	-	-	0.282
L1	0.25	0.35	0.30
L2	0.90	1.00	0.95
All Dimensions in mm			

Note 8: Device side walls are electrically active bare silicon. Avoid contact of solder or flux on the side walls during the PCB assembly process.

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**X3-WLB1608-2**



Dimensions	Value (in mm)
X	0.385
X1	1.035
X2	1.622
Y	0.690

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