



4 CHANNEL LOW CAPACITANCE TVS DIODE ARRAY

Product Summary

V _{BR} (Min)	I _{PP} (Max)	C _{I/O} (Typ)
4.5V	45A	2.1pF

Description

The D5V0P4UR6SO is a high-performance device suitable for protecting four high-speed I/Os. These devices are assembled in SOT26 package and have high ESD surge capability and low capacitance.

Applications

Typically used at high-speed ports such as USB 2.0, IEEE1394 (FireWire®, iLink), Serial ATA, DVI™, HDMI™ and PCI™.

Features

- Low Clamping Voltage: Typical 7.5V at 12A 100ns, TLP, I/O to Vss; Typical 5.8V at 12A 100ns, TLP, Vcc to Vss
- IEC 61000-4-2 (ESD): Air ±30kV, Contact ±30kV
- IEC 61000-4-4 (EFT): ±80A (5/50ns)
- IEC 61000-4-5 (Lighting): 20A, I/O to Vss; 45A, Vcc to Vss
- TLP Dynamic Resistance: 0.15Ω , I/O to Vss; 0.07Ω , Vcc to Vss
- Low Channel Input Capacitance of 2.1pF Typical
- 4 Channels of ESD Protection
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/

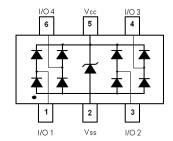
Mechanical Data

- Package: SOT26
- Package Material: Molded Plastic, "Green" Molding Compound.
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Schematic
- Terminals Finish Matte Tin Pleated Leadframe. Solderable per MIL-STD-202, Method 208 (63)
- Weight: 0.016 grams (Approximate)

SOT26



Top View



Device Schematic

Ordering Information (Note 4)

Part Number	Compliance	Bookaga	ckage Marking Reel Size (inche		Package Marking Reel Size (inches) Tape Width	Tape Width (mm)	Pa	cking
Fait Nullibei	Compliance	Package	Warking	Reel Size (Iliches)	rape widin (ililii)	Qty.	Carrier	
D5V0P4UR6SO-7	Standard	SOT26	DE1	7	8	3,000	Tape & Reel	

Notes:

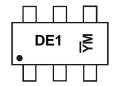
- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + CI) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

FireWire is a registered trademark of Apple Computer, Inc.

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Marking Information



DE1 = Product Type Marking Code YM = Date Code Marking Y = Year (ex: J = 2022)M = Month (ex: 2 = February)
Note: "—" Represents Internal Code

Date Code Kev

Year	2016		2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Code	D		J	K	L	М	N	0	Р	R	S	T
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Current, per IEC 61000-4-5	Ipp	20	Α	I/O to V _{SS} , 8/20µs
Peak Pulse Current, per IEC 61000-4-5	Ірр	45	Α	Vcc to Vss, 8/20µs
Peak Pulse Power, per IEC 61000-4-5	P _{PP}	180	W	I/O to Vss, 8/20µs
Operating Supply Voltage (DC)	V_{DC}	3.6	V	V _{CC} to V _{SS}
ESD Protection – Contact Discharge, per IEC 61000-4-2	Vesd_contact	±30	kV	I/O to V _{SS} , V _{CC} to V _{SS}
ESD Protection – Air Discharge, per IEC 61000-4-2	Vesd_air	±30	kV	I/O to Vss, Vcc to Vss
Operating and Storage Temperature Range	TJ, TSTG	-55 to +150	°C	_

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	PD	300	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	R _{θJA}	417	°C/W

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Conditions
Reverse Working Voltage	V_{RWM}	_	_	3.3	V	V _{CC} to V _{SS}
Reverse Leakage Current (Note 6)	ILEAK	_	_	5	μΑ	Vcc = 3.3V, Vcc to Vss
Channel Leakage Current (Note 6)	ICH-LEAK	_	_	1	μΑ	$V_{I/O} = 3.3V$, I/O to Vss
Reverse Breakdown Voltage	V _{BR}	4.5	_	7	V	IBR = 1mA, Vcc to Vss
Forward Clamping Voltage	VF	_	0.8	1.2	V	I _F = 15mA, V _{SS} to V _{CC}
Poverse Clemping Voltage (Note 7)	\/a - ·	_	6	_	V	IPP = 5A, I/O to Vss, 8/20μs
Reverse Clamping Voltage (Note 7)	Vc_5A	_	4.8	_	V	IPP = 5A, Vcc to Vss, 8/20µs
ESD Clamping Voltage	\/	_	7.5	_	V	TLP, 12A, tp = 100ns, I/O to Vss
ESD Clamping Voltage	VESD	_	5.8	_	V	TLP, 12A, tp = 100ns, Vcc to Vss
Dynamic Resistance	D-:-	_	0.15	_	Ω	TLP, 12A, t _P = 100ns, I/O to V _{SS}
Dynamic Resistance	Rdif	_	0.07	_	22	TLP, 12A, tp = 100ns, Vcc to Vss
Channel Innut Canacitance	Corr	_	2.1	2.5	pF	V _{I/O} = 1.65V, V _{CC} = 3.3V, f = 1MHz
Channel Input Capacitance	C _{I/O}	_	2.4	3.0	рF	V _{I/O} = 1.65V, V _{CC} = floated, f = 1MHz
			0.05		pF	Vss = 0V, I/O = 1.65V, Vcc = 3.3V, f = 1MHz,
Variation of Channel Input Capacitance	ΔCI/O	_	0.05	_	ρг	I/O_x to Vss - I/O_y to Vss
variation of charine input capacitance	ΔΟΙ/Ο	_	0.04	_	pF	Vss = 0V, I/O = 1.65V, Vcc = floated, f = 1MHz, I/O_x to Vss - I/O_y to Vss

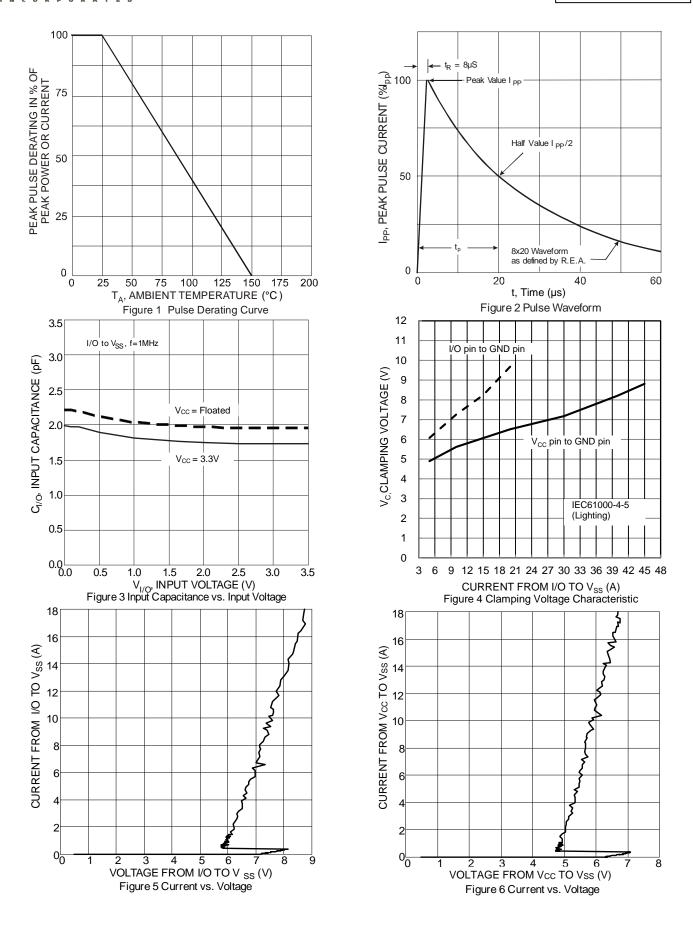
5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes Incorporated's website at http://www.diodes.com/package-outlines.html. Notes:

6. Short duration pulse test used to minimize self-heating effect.

7. Clamping voltage value is based on an 8x20µs peak pulse current (IPP) waveform.

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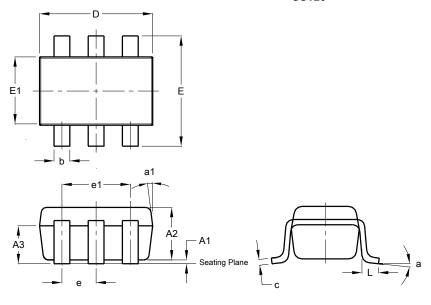




Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26

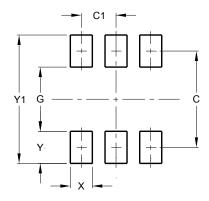


SOT26						
Dim	Min	Max	Тур			
A1	0.013	0.10	0.05			
A2	1.00	1.30	1.10			
A3	0.70	0.80	0.75			
b	0.35	0.50	0.38			
С	0.10	0.20	0.15			
D	2.90	3.10	3.00			
е	-	_	0.95			
e1	-	_	1.90			
Е	2.70	3.00	2.80			
E1	1.50	1.70	1.60			
L	0.35	0.55	0.40			
а	_	_	8°			
a1	_	_	7°			
All	Dimen	sions	in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26



Dimensions	Value (in mm)
C	2.40
C1	0.95
G	1.60
Х	0.55
Y	0.80
V1	3.20



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