A product Line of
Diodes Incorporated

**PI6LC48S0401**

# 5 Output HiFlex™ Ethernet Network Clock Generator

## Features

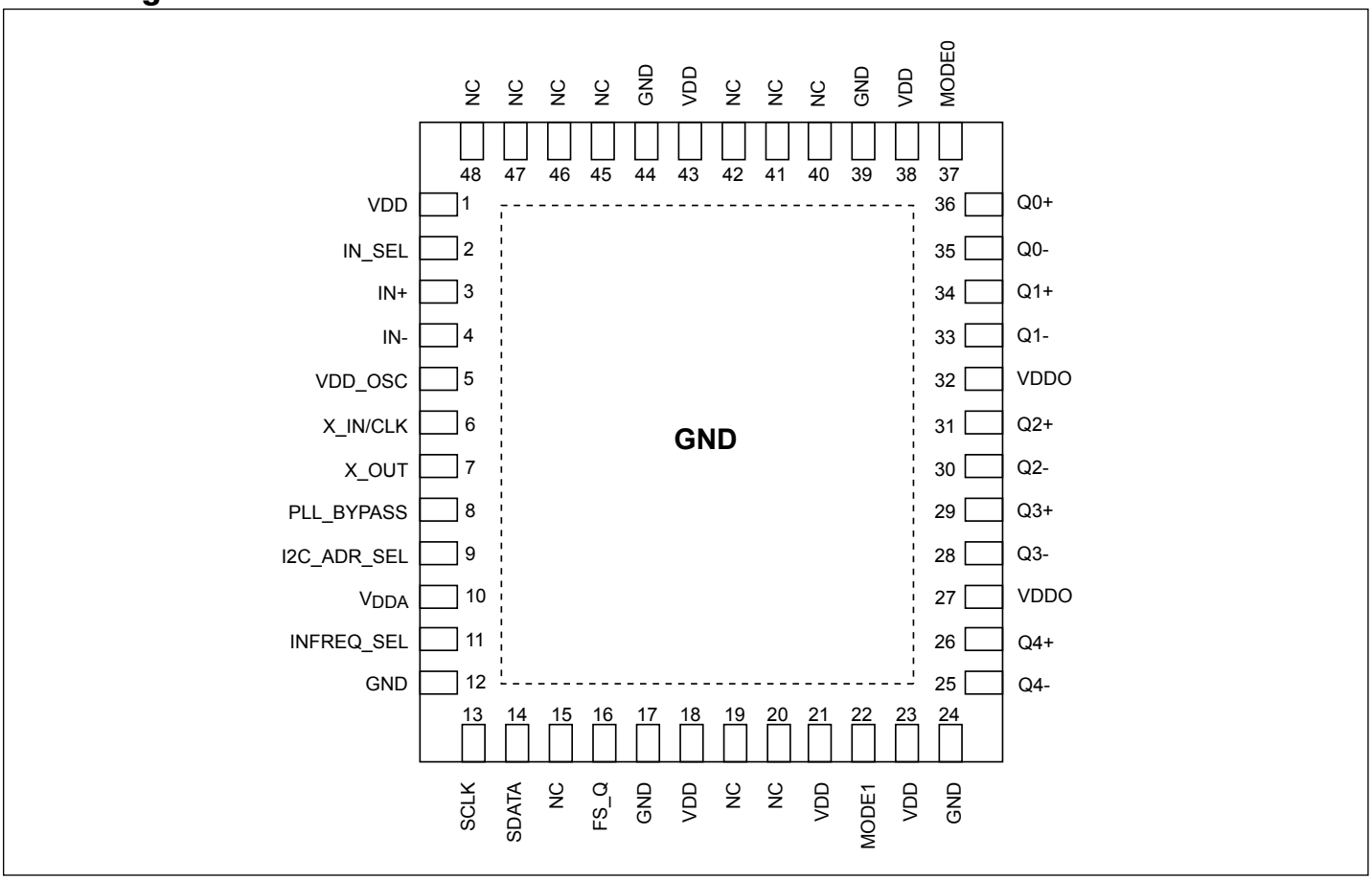
- 3.3V & 2.5V supply voltage
- Crystal/CMOS input: 25 MHz
- Differential input: 25MHz, 125MHz, and 156.25 MHz
- Output frequencies: 156.25, 125, 100, 50, 25MHz
- 5 outputs with selectable output signaling: LVPECL or LVDS
- Low 0.3ps typical integrated phase noise design: 156.25MHz (12kHz to 20MHz)
- PLL Bypass mode
- Power supply noise rejection: -52 dBc typical @ VDD
- Packaging (Pb-free & Green): 48 Contact 6×6mm TQFN
- Industrial temperature support: -40C to 85C

## Description

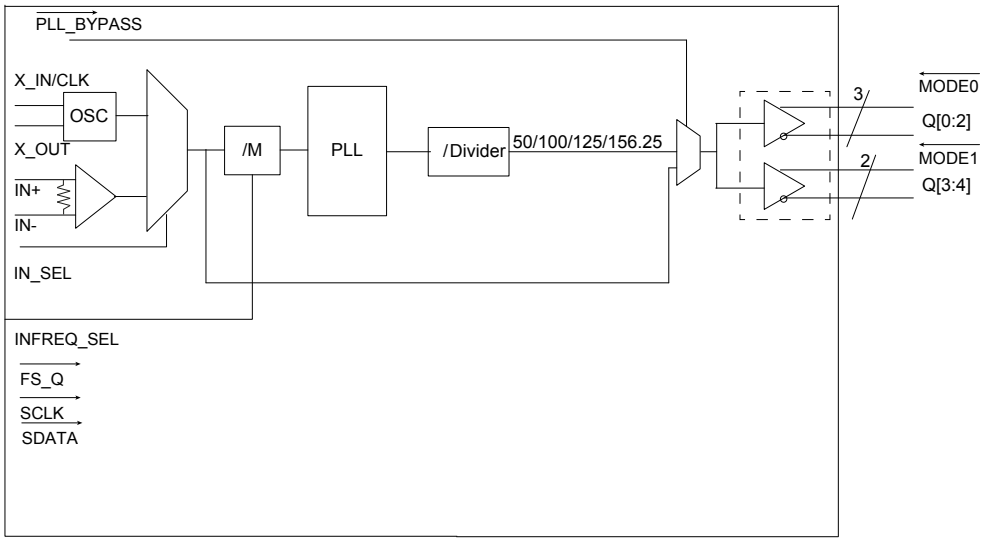
The PI6LC48S0401 is an LC VCO based low phase noise design intended for Ethernet applications. Typical 10GbE usage assumes a 25MHz crystal input, while the PLL loop is used to generate the 156.25MHz and other Ethernet clock frequencies.

For Ethernet applications other than 10GbE, programmable dividers allow for outputs of 156.25, 125, 100, 50, and 25MHz. This device offers both pin selection and $I^2C$ interface to give more options to meet various system needs.

## Pin Configuration



## Block Diagram




100MHz output frequency can be selected only in $I^2C$ mode

## Pin Description

| Pin Number | Pin Name | Type | | Description |
|---|---|---|---|---|
| 1, 18, 21, 23, 38, 43 | VDD | Power | – | Core supply |
| 2 | IN_SEL | Input | CMOS | Input select between Xtal and differential input |
| 3 | IN+ | Input | LVPECL | Differential reference input, also accepts AC-coupled LVDS, CML, HCSL or LVPECL. Differential inputs have an internal 100Ω cross resistor. |
| 4 | IN- | Input | | |
| 5 | VDD_OSC | Power | - | Power supply for Xtal Oscillator circuit |
| 6 | X_IN/CLK | Input | | Xtal or clock input, connect to a 25MHz Xtal or single-ended clock |
| 7 | X_OUT | Output | | Xtal output |
| 8 | PLL_BYPASS | Input | CMOS | PLL bypass, provide input frequency to outputs |
| 9 | I2C_ADR_SEL | Input | CMOS | I2C address selection. |
| 10 | VDDA | Power | – | Analog supply |
| 11 | INFREQ_SEL | Input | Tri-level | Input frequency selection for reference input |
| 12, 17, 24, 39, 44 | GND | Power | | Connect to ground |
| 15, 19, 20, 40, 41, 42, 45, 46, 47, 48 | NC | - | | No connect |

## Pin Description (cont.)

| Pin Number | Pin Name | Type | | Description |
|---|---|---|---|---|
| 13 | SCLK | Input | | $I^2C$ clock input |
| 14 | SDATA | Input/ Output | | $I^2C$ Data line |
| 16 | FS_Q | Input | Tri-level | Output frequency select |
| 22 | MODE1 | Input | Tri-level | Q3 ~ Q4 output control |
| 25, 26 | Q4-, Q4+ | Output | LVPECL/ LVDS | Differential outputs |
| 27, 32 | VDDO | Power | | Power supply for differential outputs |
| 28, 29 | Q3-, Q3+ | Output | LVPECL/ LVDS | Differential outputs |
| 30, 31 | Q2-, Q2+ | Output | LVPECL/ LVDS | Differential outputs |
| 33, 34 | Q1-, Q1+ | Output | LVPECL/ LVDS | Differential outputs |
| 35, 36 | Q0-, Q0+ | Output | LVPECL/ LVDS | Differential outputs |
| 37 | MODE0 | Input | Tri-level | Q0 ~ Q2 output control |
| E-pad | GND | Power | | Connect to ground, use thermal vias |

## Input MUX Selection

| IN_SEL | Input Source |
|---|---|
| 0 | Crystal Input (X_IN/CLK, X_OUT) |
| 1 | Differential Input (IN+, IN-) |
| NC | Crystal Input (X_IN/CLK, X_OUT) |

## Reference Input Frequency Select Table

| INFREQ_SEL | Reference Input |
|---|---|
| 0 | 25MHz |
| 1 | 125MHz |
| NC | 156.25MHz |

## PLL Bypass Control Function

| PLL_BYPASS | PLL operation |
|---|---|
| 0 | PLL enabled |
| 1 | PLL bypassed |

## Differential Output Control

| MODE0 | Q[0:2] | MODE1 | Q[3:4] |
|---|---|---|---|
| 0 | LVPECL | 0 | LVPECL |
| 1 | LVDS | 1 | LVDS |
| NC | Hi-Z | NC | Hi-Z |

## Output Frequency Control Table

| FS_Q | Output Freq. |
|---|---|
| 0 | 156.25MHz |
| 1 | 125MHz |
| NC | 50MHz |

## I2C Address Selection Table

| $I^2C$_ADR_SEL | I2C Address |
|---|---|
| 0 | DC (h) |
| 1 | DE (h) |

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Supply Voltage to Ground Potential, $V_{DD}$, $V_{DDA}$ $V_{DDO}$ –0.5V to +4.6V
ESD Protection (HBM) ..... 2000 V
Junction Temperature ..... 125 °C max

**Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

## Operating Conditions

| Symbol | Parameters | Conditions | Min.. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Power Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| $V_{DDO}$ | Output Power Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| $V_{DDA}$ | Analog Power Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Power Supply Current | | | | 100 | mA |
| $I_{DDO}$ | Power Supply Current for Outputs | All outputs loaded, Diff. outputs are LVPECL | | | 300 | mA |
| | | All outputs loaded, Diff. outputs are LVDS | | | 130 | mA |
| $I_{DDA}$ | Analog Power Supply Current | | | | 45 | mA |
| $T_A$ | Ambient Temperature | | –40 | | 85 | °C |

## Input Electrical Characteristics

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $R_{pu}$ | Internal pull up resistance | | | 51 | | KΩ |
| $R_{dn}$ | Internal pull down resistance | | | 51 | | KΩ |
| $C_{XTAL}$ | Internal capacitance on X_IN and X_OUT pins | | | 12 | | pF |

## LVCMOS DC Electrical Characteristics

| Symbol | Parameters | Conditions | Min.. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | $V_{DD}$ = 3.3V ±10% | 2 | | $V_{DD}$ +0.3 | V |
| | | $V_{DD}$ = 2.5V ±5% | 1.7 | | $V_{DD}$ +0.3 | V |
| $V_{IL}$ | Input Low Voltage | $V_{DD}$ = 3.3V ±10% | -0.3 | | 0.8 | V |
| | | $V_{DD}$ = 2.5V ±5% | -0.3 | | 0.5 | V |
| $I_{IH}$ | Input High Current | $V_{IN}$ = $V_{DD\ max.}$ | | | 150 | µA |
| $I_{IL}$ | Input Low Current | $V_{IN}$ = 0V | -150 | | | µA |
| $T_{DC}$ | Input Duty Cycle | | 35 | | 65 | % |
| $C_{IN}$ | Input Capacitance | | | 3.5 | | pF |

## Differential Input DC Characteristics

| Symbol | Parameters | Conditions | Min.. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | | $V_{DD}$ - 0.7 | V |
| $V_{IL}$ | Input Low Voltage | | $V_{DD}$ - 2.0 | | | V |
| $V_{CM}$ | Input Bias Voltage | | 0.5 | | $V_{DD}$ - 0.85 | V |
| $R_{IN}$ | Input Differential Impedance[1] | | 80 | 100 | 120 | Ω |
| $V_{IN-PP}$ | Input Differential Swing | Differential peak to peak | 0.3 | | 2.6 | V |

**Note: 1.** Differential input can be AC or DC coupled.

## Crystal Characteristic

| Parameters | Description | Min. | Typ | Max. | Units |
|---|---|---|---|---|---|
| OSCmode | Mode of Oscillation | | Fundamental | | |
| FREQ | Frequency | 10 | 25 | 40 | MHz |
| ESR[1] | Equivalent Series Resistance | | | 50 | Ω |
| Cload | Load Capacitance | | 18 | | pF |
| Cshunt | Shunt Capacitance | | | 7 | pF |
| | Drive Level | | | 250 | uW |

**Note: 1.** ESR value is dependent upon frequency of oscillation

## LVPECL Output DC Characteristics (1)

| Symbol | Parameters | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OPP}$ | Output peak-peak Voltage | Single-ended | | 0.78 | | V |
| $V_{OH}$ | Output High Voltage | Outputs terminated with 50Ω to $V_{DDO}$ - 2V | $V_{DDO}$ - 1.4 | | $V_{DDO}$ - 0.7 | V |
| $V_{OL}$ | Output Low Voltage | | $V_{DDO}$ - 2.0 | | $V_{DDO}$ - 1.3 | V |

## LVDS Output DC Characteristics (1)

| Symbol | Parameters | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OPP}$ | Output Peak-peak Voltage | Single-ended | 0.247 | | 0.454 | V |
| $DV_{OPP}$ | $V_{OPP}$ Magnitude Change | | | | 50 | mV |
| $V_{OS}$ | Output Offset Voltage | | 1.125 | | 1.375 | V |
| $DV_{OS}$ | $V_{OS}$ Magnitude Change | | | | 50 | mV |

## AC Output Characteristics (see test configurations) (1)

$T_A$=-40C to 85C; $V_{DD}$=3.3V±10%, $V_{DDO}$=3.3V±10%

| Symbol | Parameters | Condition | | Min.. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | LVPECL | | | | 156.25 | MHz |
| | | LVDS | | | | 156.25 | MHz |
| $t_{R\,/\,tF}$ | Rise and Fall Time; 20% ~80% | LVPECL, LVDS | | | 250 | 400 | ps |
| $t_{DC}$ | Duty Cycle | LVPECL, LVDS | | 48 | | 52 | % |
| $tj_{PHASE}$ | Integrated phase jitter (RMS) | 12kHz-20MHz @ 156.25MHz, 25MHz Xtal input | | | 0.25 | 0.4 | ps |
| | | 10kHz-5MHz @ 25MHz, 25MHz Xtal input | | | 0.33 | 0.4 | ps |
| $tj_{c\text{-}c}$ | Cycle to cycle jitter | | | | 28 | 30 | ps |
| $tj_{Pk\text{-}Pk}$ | Peak to Peak jitter | | | | 30 | 35 | ps |
| $f_N$ | Single-Side Band Phase Noise | 156.25MHz, 25MHz Xtal input | Offset 1kHz | | -117 | | dBc/Hz |
| | | | Offset 10kHz | | -130 | | |
| | | | Offset 100kHz | | -134 | | |
| | | | Offset 1MHz | | -139 | | |
| | | | Offset 10MHz | | -154 | | |

## AC Output Characteristics (continued)

$T_A$=-40C to 85C; $V_{DD}$=3.3V±10%, $V_{DDO}$=3.3V±10%

| Symbol | Parameters | Condition | Min.. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| PSNR | Power Supply Noise Rejection | $V_{DD}$, 50mVpp, 10k-1.5MHz | | -52 | | dBc |
| | | $V_{DDA}$, 50mVpp, 10k-1.5MHz | | -65 | | |
| | | $V_{DDO}$, 50mVpp, 10k-1.5MHz | | -50 | | |
| $t_{STARTUP}$ | Start time | | | | 10 | ms |
| $t_{LOCK}$ | PLL lock time | | | | 20 | ms |

**Note:**

1. $V_{DDO}$= 3.3V is not valid with $V_{DD}$= 2.5V

## Serial Data Interface ($I^2C$ compatible)

PI6LC48S0401 is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer.

For full electrical I2C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 50kΩ typical.

### Address Assignment

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 1 | 1 | $I^2C$_ADR_SEL | 1/0 |

### How to Write

| 1 bit | 7 bits | 1 bit | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | | 8 bits | 1 bit | 1 bit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Start bit | Address | W(0) | Ack | Data Byte (D) | Ack | Data Byte (D+1) | Ack | ..... | Data Byte (D+N) | Ack | Stop bit |

### How to Read

| 1 bit | 7 bits | 1 bit | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | | 8 bits | 1 bit | 1 bit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Start bit | Address | R(1) | Ack | Data Byte (D) | Ack | Data Byte (D+1) | Ack | ..... | Data Byte (D+N) | Ack | Stop bit |

## Output Frequency I2C bit Control Table

| FS_Q (2-bit) | Output Freq. |
|---|---|
| 0 0 | 156.25MHz |
| 0 1 | 50MHz |
| 1 0 | 125MHz |
| 1 1 | 100MHz |

## Input Freq. I2C bit Control Table

| INFREQ_SEL (2-bit) | Input Freq. |
|---|---|
| 0 0 | 25MHz |
| 0 1 | 156.25MHz |
| 1 0 | 125MHz |
| 1 1 | 100MHz |

## Byte 0: Output Frequency Selection Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | | | |
| 6 | Reserved | | | | | |
| 5 | FS_Q (1) | Output divider | RW | 0 | See FS_Q $I^2C$ control table | |
| 4 | FS_Q (0) | | RW | 0 | | |
| 3 | Reserved | | | | | |
| 2 | Reserved | | | | | |
| 1 | Vendor ID | | RW | 0 | | |
| 0 | Vendor ID | | RW | 0 | | |

## Byte 1: Output Frequency Selection and Misc. Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | $I^2C$ pin control | Determine external pins or $I^2C$ control mode | RW | 0 | External pins | $I^2C$ |
| 6 | I2C_ADR_SEL | Select $I^2C$ write address | RW | 0 | DC(h) | DE(h) |
| 5 | INFREQ_SEL (1) | Input frequency selection | RW | 0 | See INFREQ_SEL $I^2C$ control table | |
| 4 | INFREQ_SEL (0) | | RW | 0 | | |
| 3 | Reserved | | | | | |
| 2 | Reserved | | | | | |
| 1 | Reserved | | | | | |
| 0 | Reserved | | | | | |

## Byte 2: Output Enable Selection

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | | | |
| 6 | Reserved | | | | | |
| 5 | OE for Q4 | Output enable bit for Q4 | RW | 0 | Enable | Disable |
| 4 | OE for Q3 | Output enable bit for Q3 | RW | 0 | Enable | Disable |
| 3 | OE for Q2 | Output enable bit for Q2 | RW | 0 | Enable | Disable |
| 2 | OE for Q1 | Output enable bit for Q1 | RW | 0 | Enable | Disable |
| 1 | OE for Q0 | Output enable bit for Q0 | RW | 0 | Enable | Disable |
| 0 | Reserved | | | | | |

## Byte 3: Reserved

## Byte 4: Output Type Selection

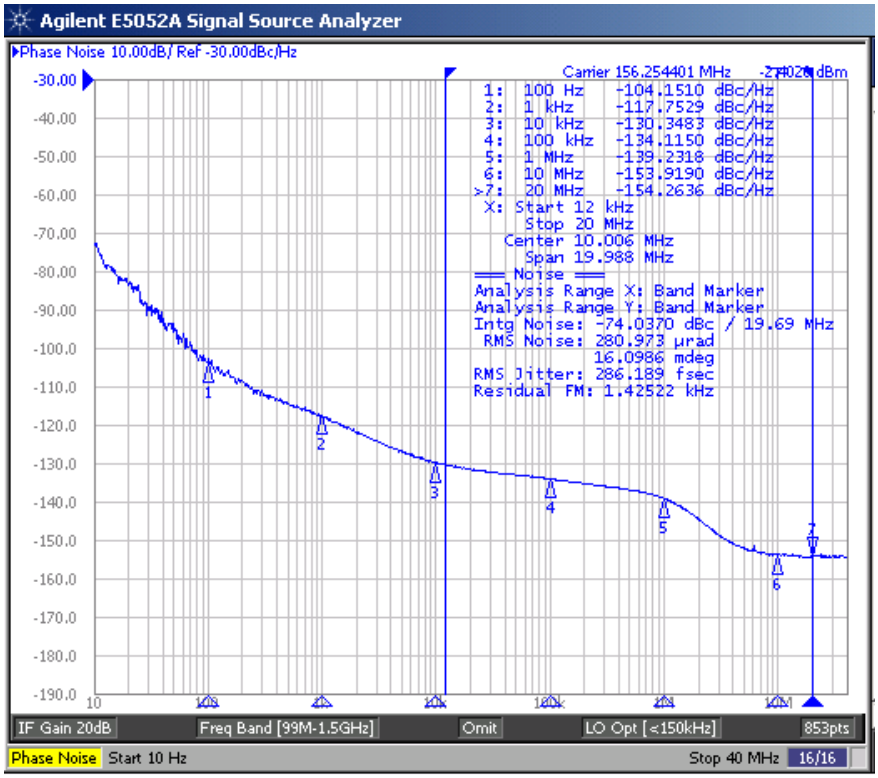
| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | | | |
| 6 | Reserved | | | | | |
| 5 | Q4 | Output Type Select Q4 | RW | 0 | LVPECL | LVDS |
| 4 | Q3 | Output Type Select Q3 | RW | 0 | LVPECL | LVDS |
| 3 | Q2 | Output Type Select Q2 | RW | 0 | LVPECL | LVDS |
| 2 | Q1 | Output Type Select Q1 | RW | 0 | LVPECL | LVDS |
| 1 | Q0 | Output Type Select Q0 | RW | 0 | LVPECL | LVDS |
| 0 | Reserved | | | | | |

## Byte 5: Misc. Register

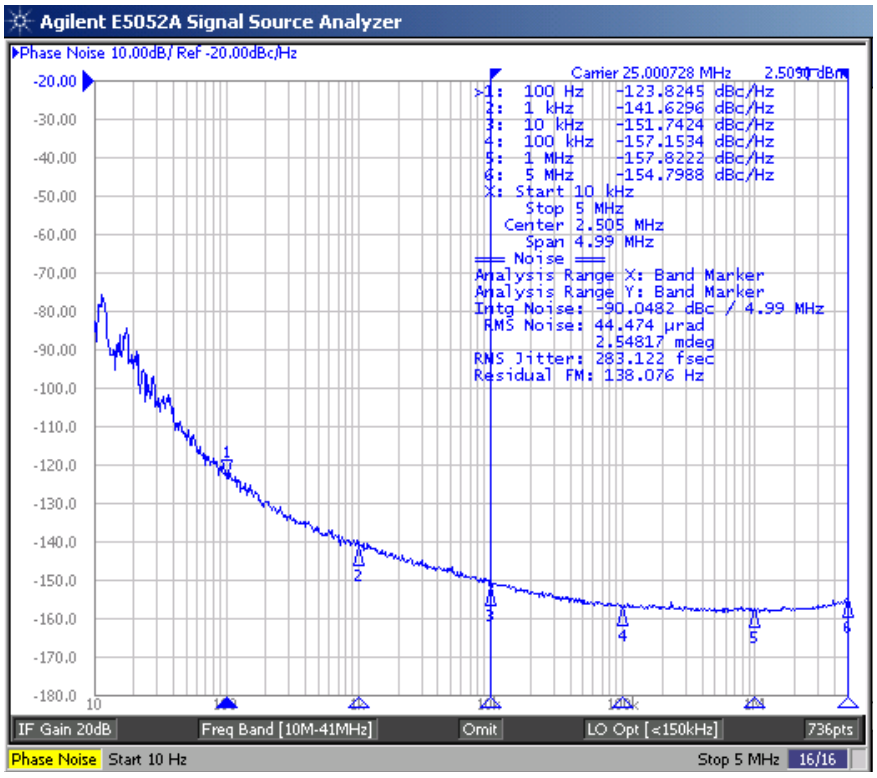
| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | | | |
| 6 | Reserved | | | | | |
| 5 | Reserved | | | | | |
| 4 | Reserved | | | | | |
| 3 | PLL_BYPASS | PLL bypass function | RW | 0 | PLL is enabled | PLL is by-passed |
| 2 | Reserved | | | | | |
| 1 | Reserved | | | | | |
| 0 | IN_SEL | Input selection | RW | 0 | Crystal | Reference |

## Phase Noise Plots

### 156.25MHz LVDS Clock




### 25MHz LVPECL Clock



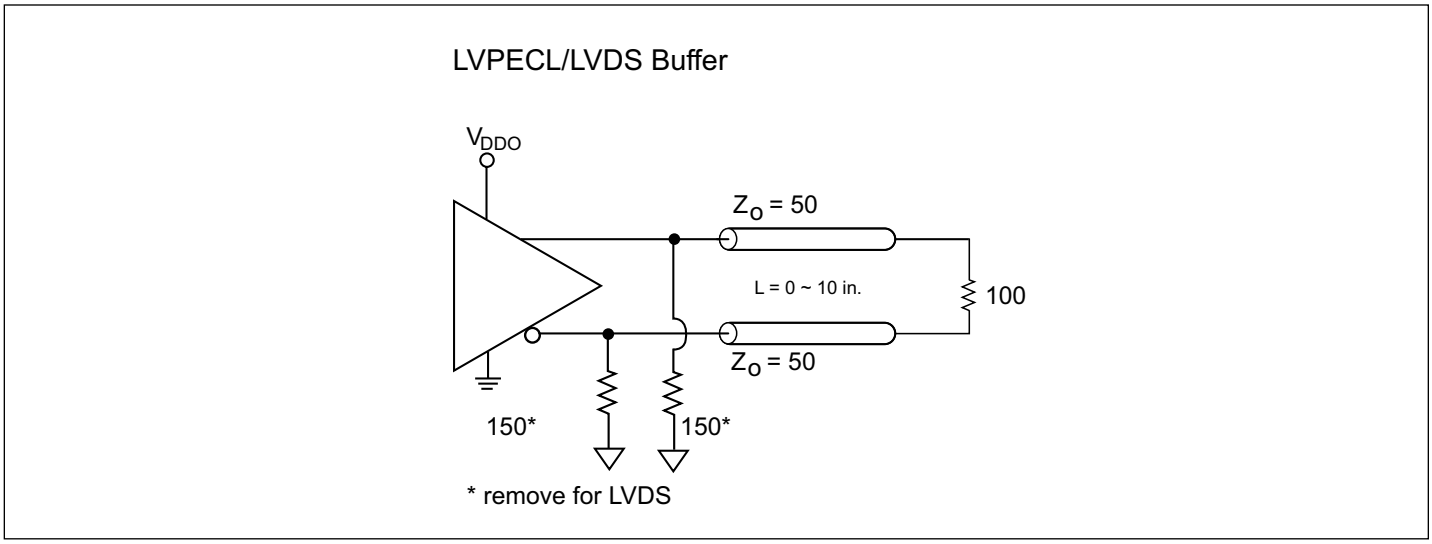



**Figure 1. LVPECL and LVDS Test Circuit**

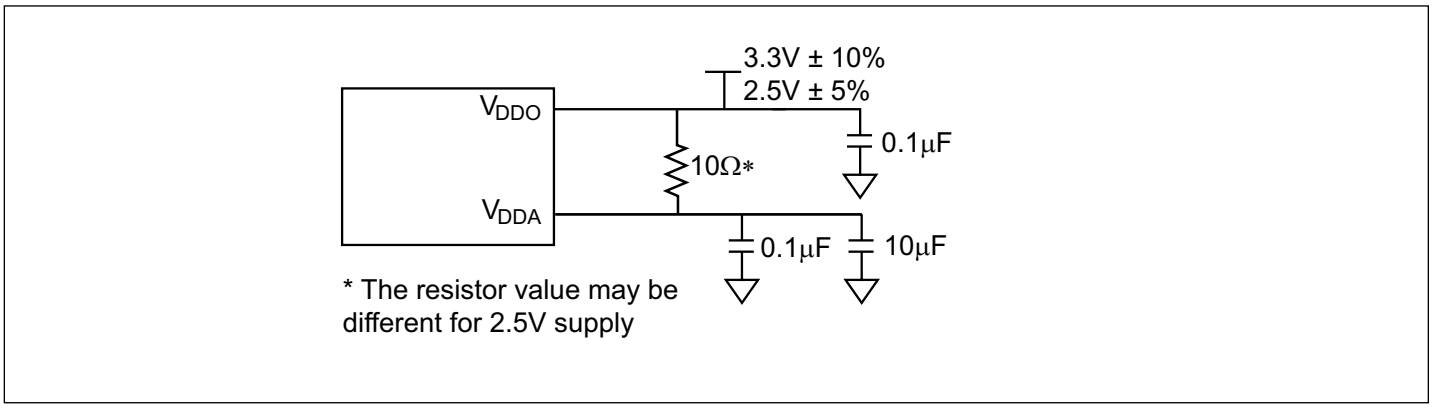
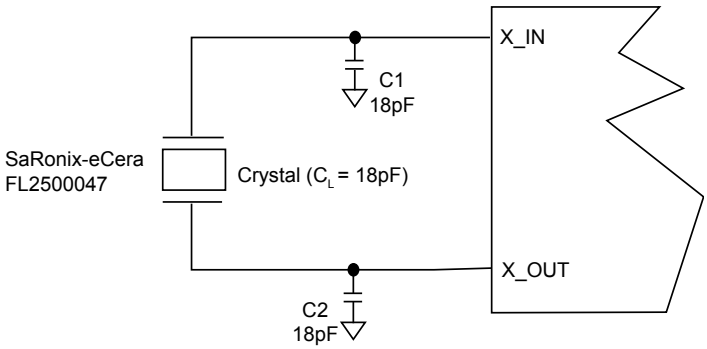



**Figure 2. Power Supply Filter**

## Crystal circuit connection

The following diagram shows PI6LC48S0401 crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1=18pF, C2=18pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

## Crystal Oscillator Circuit




## Crystal Circuit Oscillator

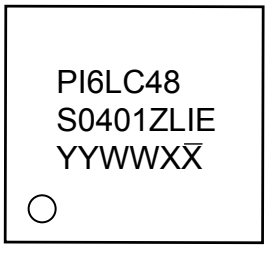
## Recommended Crystal Specification

**Pericom recommends:**

a) FY2500081, SMD 5x3.2(4P), 25MHz, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

b) FL2500047, SMD 3.2x2.5(4P), 25MHz, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

## Part Marking

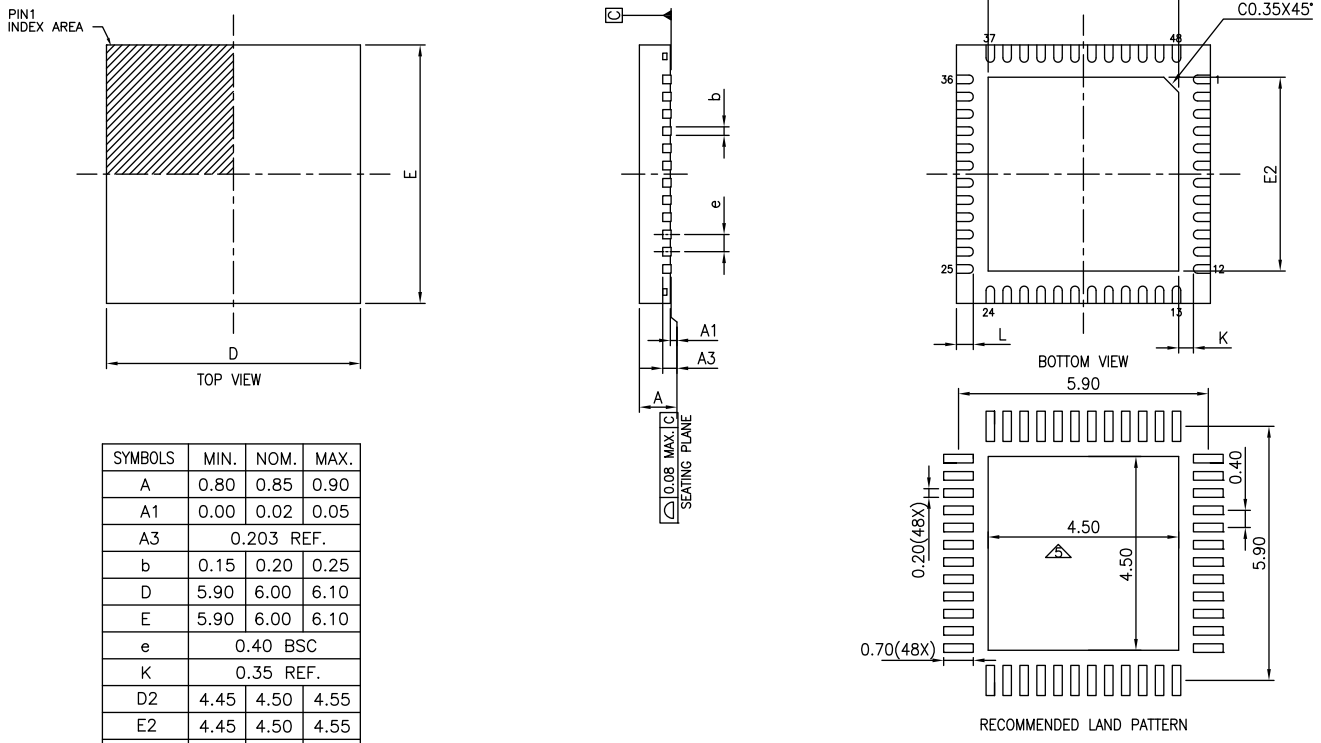



YY : Year
WW : Workweek
1st X : Assembly Code
2nd X : Fab Code

**Note:**

1. For latest datecode info, please check: https://www.diodes.com/assets/MediaList-Attachments/Pericom-Datecode-Format-Explanation.pdf

## Packaging Mechanical: 48-Contact TQFN (ZL)




| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.203 REF. | |
| b | 0.15 | 0.20 | 0.25 |
| D | 5.90 | 6.00 | 6.10 |
| E | 5.90 | 6.00 | 6.10 |
| e | | 0.40 BSC | |
| K | | 0.35 REF. | |
| D2 | 4.45 | 4.50 | 4.55 |
| E2 | 4.45 | 4.50 | 4.55 |
| L | 0.35 | 0.40 | 0.45 |

NOTE :
1. ALL DIMENSIONS ARE IN mm, ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

PERICOM Enabling Serial Connectivity

DATE: 10/26/15

DESCRIPTION: 48-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZL (ZL48)

DOCUMENT CONTROL #: PD-2201 REVISION: A

15-0244

**Note:**

1. For latest package info, please check: https://www.diodes.com/design/support/packaging/pericom-packaging/

## Ordering Information[1-3]

| Ordering Code | Package Code | Package Description | Operating Temperature |
|---|---|---|---|
| PI6LC48S0401ZLIEX | ZL | 48-Contact, Pb-free & Green (TQFN), Tape & Reel | Industrial |

**Notes:**

1. Thermal characteristics can be found on the company web site at https://www.diodes.com/design/support/packaging/pericom-packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel

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