# ULN2003V12, ULN2003F12

**Multi-Channel Relay and Inductive Load Sink Driver**

## Description

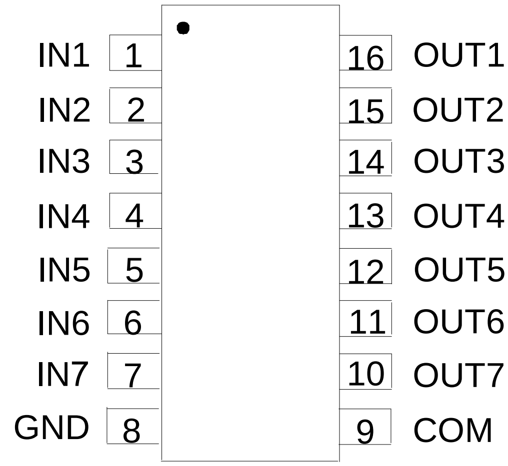
The ULN2003V12 and ULN2003F12 are multi-channel sink drivers comprised of 7-channel and 4-channel output stages respectively. The ULN2003V12 sink driver features 7 low output impedance drivers that minimize on-chip power dissipation and an actual low power upgrade version for popular ULN2003A family in real applications. When driving a typical 12V relay coil, a ULN2003V12 will dissipate 12 times lower power compared to ULN2003A. ULN2003F12 is a lower power variant benefiting from fewer channel integration and a better fit for applications requiring only 4-channel drivers, such as driving low voltage stepping motors, etc.

The ULN2003V12 and ULN2003F12 both support 3.3V to 5V CMOS logic input interface, thus making it compatible to a wide range of micro-controllers and other logic interfaces, and also feature an improved input interface that minimizes the input DC current drawn from the external drivers. The input RC snubber circuit integrated at ULN2003V12 and ULN2003F12 improves the performance in noisy operating conditions, and the internal pull-down resistor at input stage helps allow input logic to be tri-stated.

As shown in the Functional Diagram, each output of the ULN2003V12 and ULN2003F12 features an internal free-wheeling diode connected in a common-cathode configuration at the COM pin which provides flexibility of increasing current sink capability through combining several adjacent channels in parallel. Under typical conditions the ULN2003V12 can support up to 1.0A of load current when all 7-channels are connected in parallel.

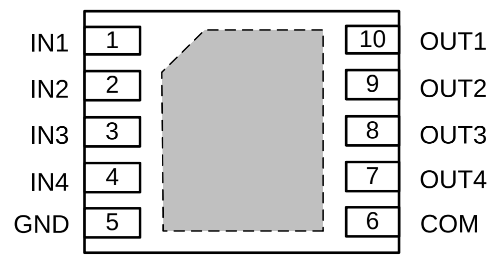
## Pin Assignments

**( Top View )**




**SO-16 / TSSOP-16**

**(Top View)**




**U-DFN3030-10**

## Features

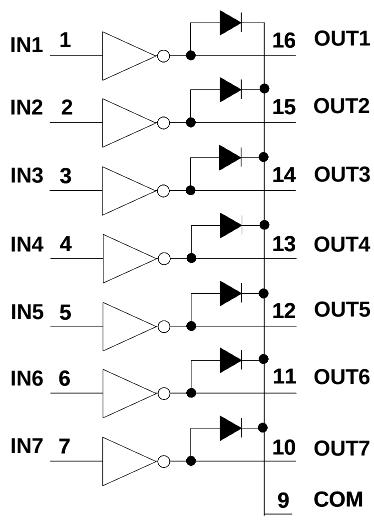
- 4- and 7-Channel High Current Sink Drivers
- Supports up to 20V Output Pull-up Voltage
- Low Output VOL of 0.6V (Typical) with
  - 100mA (Typ.) Current Sink per Channel at 3.3V Logic Input
  - 140mA (Typ.) Current Sink per Channel at 5.0V Logic Input
- Compatible to 3.3V and 5.0V Micro-Controllers and Logic Interface
- Internal Free-wheeling Diodes for Inductive Kick-back Protection
- Input Pull-down Resistors Allows Tri-Stating the Input Driver
- Input RC-Snubber to Eliminate Spurious Operation in Noisy Environments
- ESD: 4kV HBM, 1kV CDM
- Available in 16-Pin SOIC, 16-Pin TSSOP and 10-Pin DFN3030 packages
- Available in "Green" Molding Compound (No Br, Sb)
  - **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
  - **Halogen and Antimony Free. "Green" Device (Note 3)**

## Applications

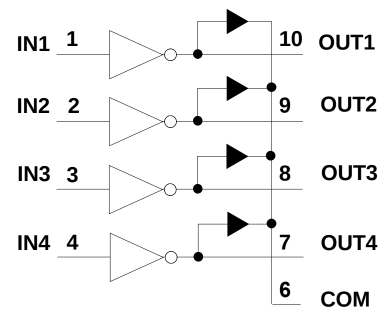
- Inputs Compatible with Popular Logic Types
- Relay Driver Applications
- Stepping Motor Applications
- Logic Level Shifter

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Functional Diagram




ULN2003V12

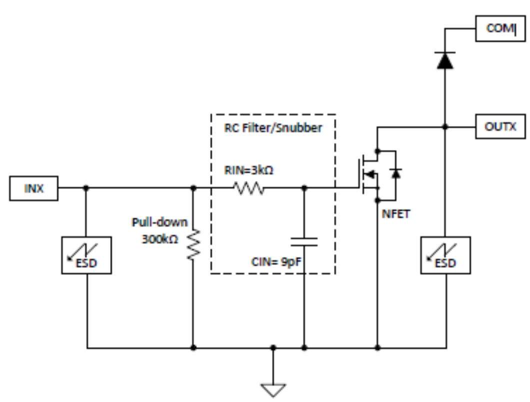



ULN2003F12

## Pin Descriptions

| Pin Name | Pin Number | | | Description |
|---|---|---|---|---|
| | SO16 | TSSOP16 | DFN3030-10 | |
| IN1 ~ IN7 | 1~7 | 1~7 | 1~4 | Logic Input Pins IN1 through IN7 |
| GND | 8 | 8 | 5 | Ground Reference Pin |
| COM | 9 | 9 | 6 | Internal Free-Wheeling Diode Common Cathode Pin |
| OUT7 ~ OUT1 | 10~16 | 10~16 | 7~10 | Channel Output Pins OUT7 through OUT1 |

## Functional Block Diagram (Single Channel)



## Absolute Maximum Ratings (@$T_A$ = +25°C, unless otherwise specified.)

| Symbol | Parameter | | Rating MIN | Rating MAX | Unit |
|---|---|---|---|---|---|
| $V_{IN}$ | Pin2 IN1~IN7 to GND Voltage | | -0.3 | 5.5 | V |
| $V_{OUT}$ | Pins OUT1~OUT7 to GND Voltage | | — | 20 | V |
| $V_{COM}$ | Pin COM to GND Voltage | | — | 20 | V |
| $I_{GND}$ | Max GND-Pin Continuous Current (+100°C <$T_J$< +125°C) | | — | 700 | mA |
| | Max GND-Pin Continuous Current ($T_J$< +100°C) | | — | 1.0 | A |
| $P_D$ | Total Device Power Dissipation at $T_A$ = +85°C | 16 Pin – SOIC | TBD | | W |
| | | 16 Pin – TSSOP | TBD | | W |
| | | 10 Pin – DFN3030 | TBD | | W |
| $θ_{JA}$ | Thermal Resistance Junction-to-Ambient (Note 6) | 16 Pin – SOIC | TBD | | °C/W |
| | | 16 Pin – TSSOP | TBD | | |
| | | 10 Pin – DFN3030 | TBD | | |
| $θ_{JC}$ | Thermal Resistance Junction-to-Case (Note 7) | 16 Pin – SOIC | TBD | | °C/W |
| | | 16 Pin – TSSOP | TBD | | |
| | | 10 Pin – DFN3030 | TBD | | |
| ESD | HBM | | — | 4 | kV |
| | CDM | | — | 1 | kV |
| $T_J$ | Junction Temperature | | -55 | 150 | °C |
| $T_{STG}$ | Storage Temperature | | -55 | 150 | °C |

Notes:
4. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
5. All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
6. Maximum power dissipation is a function of $T_J$(max), $θ_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/θ_{JA}$. Operating at the absolute maximum $T_J$ of +150°C can affect reliability.
7. Maximum power dissipation is a function of $T_J$(max), $θ_{JC}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_C)/θ_{JA}$. Operating at the absolute maximum $T_J$ of +150°C can affect reliability.

## Recommended Operating Conditions (@$T_A$ = +25°C, unless otherwise specified.)

| Symbol | Parameter | | Min | TYP | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OUT}$ | Channel Off-Stage Output Pull-Up Voltage | | — | — | 16 | V |
| $V_{COM}$ | COM Pin Voltage | | — | — | 16 | V |
| $I_{OUT(ON)}$ | Per Channel Continuous Sink Current | VINx = 3.3V | — | — | 100(5) | mA |
| | | VINx = 5.0V | — | — | 140(5) | |
| $T_J$ | Operating Junction Temperature | | -40 | — | 125 | °C |

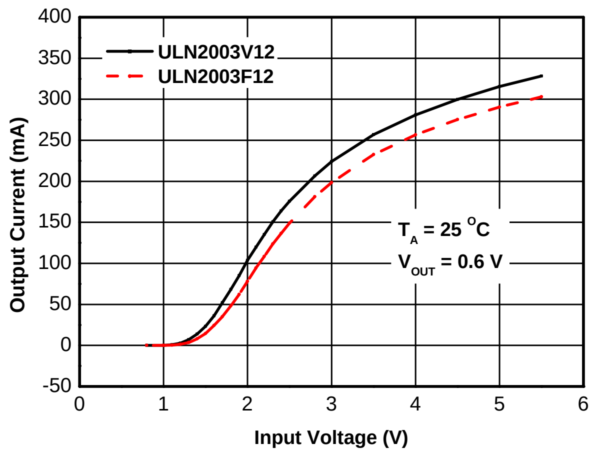
## Electrical Characteristics (@$T_A$ = +25°C, unless otherwise specified.)

Specified over the recommended junction temperature range $T_J$ = -40°C to +125°C and over recommended operating conditions unless otherwise noted. Typical values are at $T_J$ = +25°C.

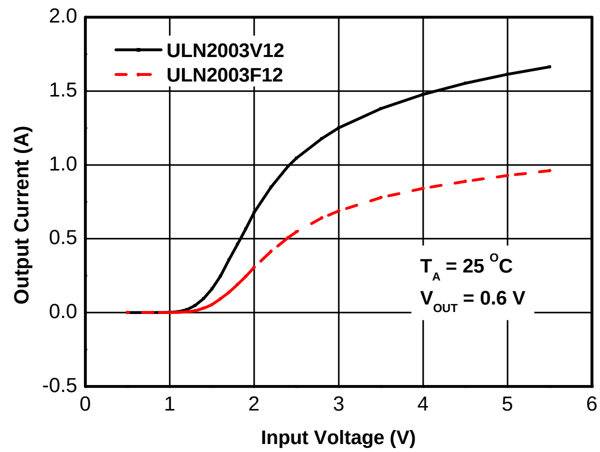
| Parameter | | Test conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUTS IN1 THROUGH IN7 PARAMETERS** | | | | | | |
| $V_{I(on)}$ | IN1~IN7 logic high input voltage | $V_{CE}$ = 2V, $I_C$ = 300mA | 1.65 | — | — | V |
| $V_{I(OFF)}$ | IN1~IN7 logic low input voltage | $I_I$ = 250µA, $I_C$ = 100mA | — | — | 0.6 | V |
| $I_{I(ON)}$ | IN1~IN7 ON state input current | $I_F$ = 350mA | — | 12 | 25 | uA |
| $I_{I(OFF)}$ | IN1~IN7 OFF state input leakage | | — | — | 250 | nA |
| **OUTPUTS OUT1 THROUGH OUT7 PARAMETERS** | | | | | | |
| $V_{OL(VCE-SAT)}$ | OUT1~OUT7 low-level output voltage | $V_{INX}$ = 3.3V, $I_{OUTX}$ = 20mA | — | 0.12 | 0.15 | V |
| | | $V_{INX}$ = 3.3V, $I_{OUTX}$ = 100mA | — | 0.6 | 0.75 | |
| | | $V_{INX}$ = 5.0V, $I_{OUTX}$ = 20mA | — | 0.09 | 0.11 | |
| | | $V_{INX}$ = 5.0V, $I_{OUTX}$ = 140mA | — | 0.6 | 0.75 | |
| $I_{OUT(ON)}$ | OUT1~OUT7 ON-state continuous current at $V_{OUTX}$ = 0.6V | $V_{INX}$ = 3.3V, $V_{OUTX}$ = 0.6V | 80 | 100 | — | mA |
| | | $V_{INX}$ = 5.0V, $V_{OUTX}$ = 0.6V | 95 | 140 | — | |
| $I_{OUT(ON)}$ | OUT1~OUT7 OFF-state leakage current | $V_{INX}$ = 0V, $V_{OUTX}$ = $V_{COM}$ =16V | — | 0.5 | — | uA |
| **SWITCHING PARAMETERS** | | | | | | |
| $t_{PHL}$ | OUT1~OUT7 logic high propagation delay | $V_{INX}$ = 3.3V, $V_{pull-up}$ = 12V, $R_{pull-up}$ = 1kΩ | — | 50 | 70 | ns |
| $t_{PLH}$ | OUT1~OUT7 logic low propagation delay | $V_{INX}$ = 3.3V, $V_{pull-up}$ = 12V, $R_{pull-up}$ = 1kΩ | — | 121 | 140 | ns |
| $t_{CHANNEL}$ | Channel to channel delay | Over recommended operating conditions and with same test conditions on channels. | — | 15 | 50 | ns |
| $R_{PD}$ | IN1~IN7 input pull-down resistance | — | 210k | 300k | 390k | Ω |
| ζ | IN1~IN7 input filter time constant | — | — | 9 | — | ns |
| $C_{OUT}$ | OUT1~OUT7 output capacitance | $V_{INX}$ = 3.3V, $V_{OUTX}$ = 0.4V | — | 15 | — | pF |
| **FREE-WHEELING DIODE PARAMETERS** | | | | | | |
| VF | Forward voltage drop | $I_{F-peak}$ = 140mA, VF = $V_{OUTx}$ -$V_{COM}$ | — | 1.2 | — | V |
| $I_{F-peak}$ | Diode peak forward current | — | — | 140 | — | mA |

## Performance Characteristics

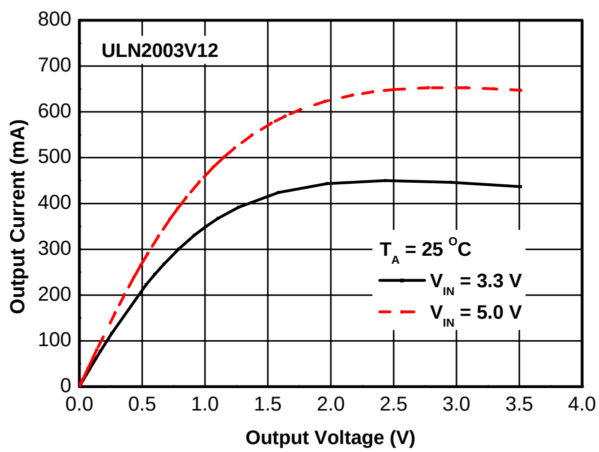
Output Current vs. Input Voltage (One Darlington)



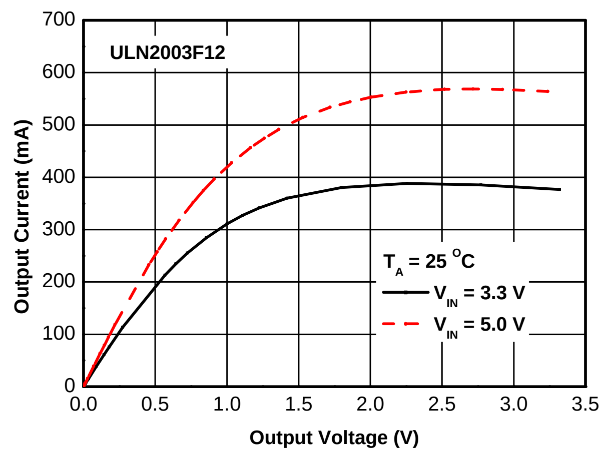

Output Current vs. Input Voltage (All Darlingtons in Parallel)




Output Current vs. Output Voltage

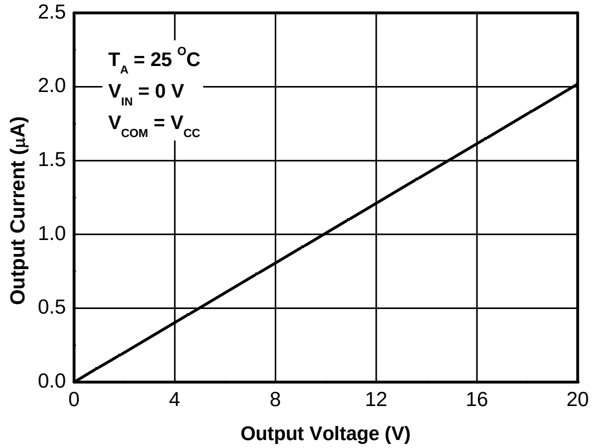



Output Current vs. Output Voltage

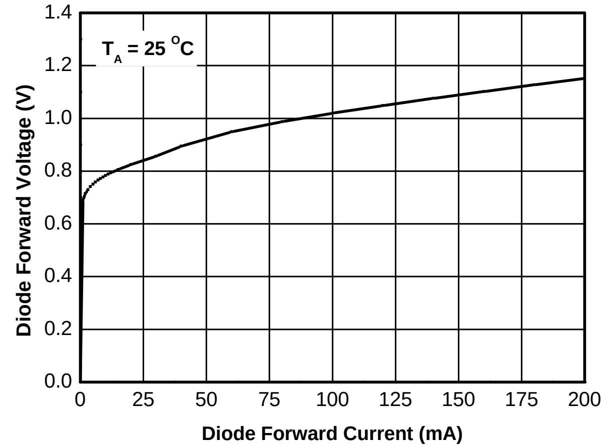


## Performance Characteristics (Cont.)

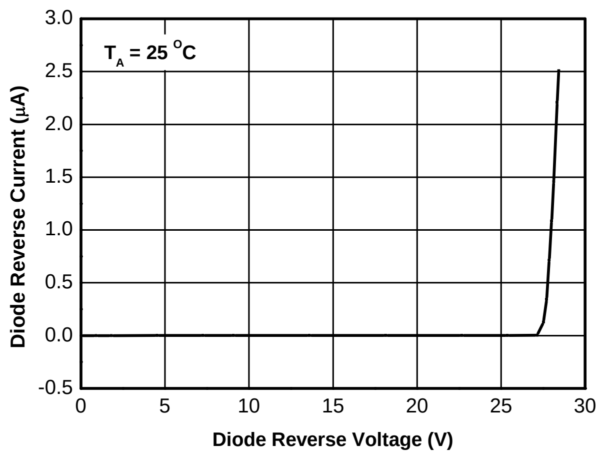
Output Current vs. Output Voltage




Diode Forward Voltage vs. Diode Forward Current




Diode Reverse Current vs. Diode Reverse Voltage



## Ordering Information

**ULN2003 XXX XXX - X**

| Device | Package | Packing |
|---|---|---|
| V12 : 7 Channels<br>F12 : 4 Channels | S16 : SO-16<br>T16 : TSSOP-16<br>FN : U-DFN3030-10 | 7/13 : Tape & Reel |

| Device | Package Code | Packaging (Note 11) | 7"/13" Tape and Reel | |
|---|---|---|---|---|
| | | | Quantity | Part Number Suffix |
| ULN2003V12S16-13 | S16 | SO-16 | 2,500/Tape & Reel | -13 |
| ULN2003V12T16-13 | T16 | TSSOP-16 | 2,500/Tape & Reel | -13 |
| ULN2003F12FN-7 | FN | DFN3030-10 | 3,000/Tape & Reel | -7 |

Note: 8. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

## Marking Information

**(1) SO-16 and TSSOP-16**

**( Top View )**

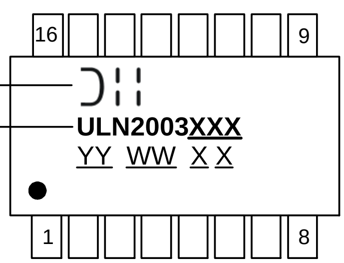
Logo

Part Number

Device:

V12 : 7 Channels

F12 : 4 Channels



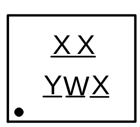

YY : Year : 08, 09,10~

WW : Week : 01~52; 52 represents 52 and 53 week

XX : Internal Code

**(2) DFN3030-10**

**( Top View )**




XX : Identification Code

Y : Year : 0~9

W : Week : A~Z : 1~26 week; a~z : 27~52 week; z represents 52 and 53 week

X : Internal Code

| Part Number | Package | Identification Code |
|---|---|---|
| ULN2003F12FN-7 | DFN3030-10 | A3 |