



#### **N-CHANNEL ENHANCEMENT MODE MOSFET**

### **Product Summary**

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> Max T <sub>C</sub> = +25°C		
00)/	$11m\Omega @ V_{GS} = 4.5V$	21A		
20V	$13m\Omega @ V_{GS} = 2.5V$	20A		

# **Description and Applications**

This MOSFET is designed to minimize the on-state resistance  $(R_{DS(ON)})$ , yet maintain superior switching performance, making it ideal for high efficiency power management applications.

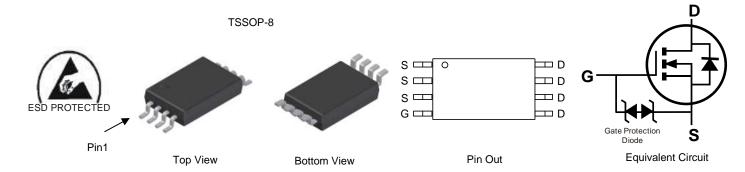
- Battery Management Application
- Power Management Functions
- DC-DC Converters

### **Features and Benefits**

- Low Gate Threshold Voltage
- Low On-Resistance
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

### **Mechanical Data**

- Case: TSSOP-8
- Case Material: Molded Plastic, "Green" Molding Compound.
   UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (a)
- Weight: 0.039 grams (Approximate)



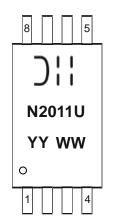
### **Ordering Information** (Note 4)

Part Number	Case	Packaging
DMN2011UTS-13	TSSOP-8	2.500/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

# **Marking Information**



]|| = Manufacturer's Marking N2011U = Product Type Marking Code YYWW = Date Code Marking YY = Year (ex: 17 = 2017) WW = Week (01 to 53)



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Characteristic	Symbol	Value	Unit		
Drain-Source Voltage	$V_{DSS}$	20	V		
Gate-Source Voltage	$V_{GSS}$	±12	V		
Continuous Drain Current (Note 6) V 4 5V	Steady State	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$	I <sub>D</sub>	9.0 7.2	А
Continuous Drain Current (Note 6) V <sub>GS</sub> = 4.5V	Steady State	$T_C = +25$ °C $T_C = +70$ °C	I <sub>D</sub>	21 17	А
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	70	A		
Continuous Source-Drain Diode Current (Note 6)	Is	3	Α		
Pulsed Source-Drain Diode Current (10µs Pulse, Du	I <sub>SM</sub>	25	А		
Avalanche Current (Note 7) L = 0.1mH	I <sub>AS</sub>	18	Α		
Avalanche Energy (Note 7) L = 0.1mH	E <sub>AS</sub>	17	mJ		

### Thermal Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 5)	$T_A = +25$ °C	$P_{D}$	0.9	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{ heta JA}$	144	°C/W
Total Power Dissipation (Note 6)	$T_A = +25^{\circ}C$	P <sub>D</sub>	1.3	W
Thermal Resistance, Junction to Ambient (Note 6)  Steady State		$R_{\theta JA}$	93	°C/W
Thermal Resistance, Junction to Case (Note 6) Steady State		Rejc	16	C/VV
Operating and Storage Temperature Range	T <sub>J,</sub> T <sub>STG</sub>	-55 to +150	°C	

## **Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	20	1	_	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	I <sub>DSS</sub>	-	_	1	μA	$V_{DS} = 16V, V_{GS} = 0V$	
Gate-Source Leakage			1	±10	μA	$V_{GS} = \pm 10V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	0.4		1.0	V	$V_{DS} = V_{GS}$ , $I_D = 250\mu A$	
			7.2	11		$V_{GS} = 4.5V, I_D = 7A$	
Static Drain-Source On-Resistance	Б		9.0	13	mΩ	$V_{GS} = 2.5V, I_D = 7A$	
Static Dialii-Source Off-Resistance	R <sub>DS(ON)</sub>		11.5	25	11122	$V_{GS} = 1.8V, I_D = 5A$	
			19.1	50		$V_{GS} = 1.5V, I_D = 3A$	
Diode Forward Voltage	V <sub>SD</sub>	_	0.7	1.2	V	$V_{GS} = 0V, I_S = 8.5A$	
DYNAMIC CHARACTERISTICS (Note 9)					•		
Input Capacitance	C <sub>ISS</sub>	-	2,248	_	pF		
Output Capacitance	Coss	_	295	_	pF	$V_{DS} = 10V, V_{GS} = 0V,$ - f = 1.0MHz	
Reverse Transfer Capacitance	C <sub>RSS</sub>	_	265	_	pF	1 = 1.0lvin2	
Gate Resistance	$R_{G}$	_	1.5	_	Ω	$V_{DS} = 0V$ , $V_{GS} = 0V$ , $f = 1MHz$	
Total Gate Charge (V <sub>GS</sub> = 4.5V)	$Q_{G}$	_	24	_	nC		
Total Gate Charge (V <sub>GS</sub> = 10V)	$Q_{G}$	_	56	_	nC	101/ 1 0.54	
Gate-Source Charge	Q <sub>GS</sub>	_	3.5	_	nC	$V_{DS} = 10V, I_D = 8.5A$	
Gate-Drain Charge	$Q_GD$		5.1	_	nC	1	
Turn-On Delay Time	t <sub>D(ON)</sub>	_	3.6	_	ns		
Turn-On Rise Time	t <sub>R</sub>		2.6	_	ns	$V_{DS} = 10V, I_D = 8.5A$	
Turn-Off Delay Time	t <sub>D(OFF)</sub>		21.6	_	ns	$V_{GS} = 4.5V, R_{G} = 1.8\Omega$	
Turn-Off Fall Time	t <sub>F</sub>		13.5	_	ns	1	
Reverse Recovery Time	t <sub>RR</sub>		12.8	_	ns		
Reverse Recovery Charge	$Q_{RR}$	_	6.9	_	nC	I <sub>F</sub> = 8.5A, di/dt = 210A/μs	

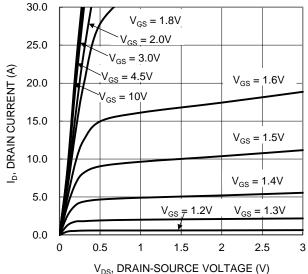
Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

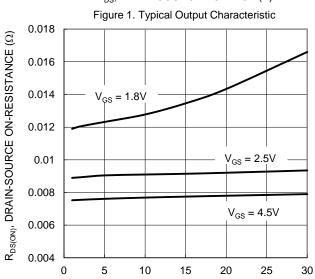
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

- 7. IAS and EAS ratings are based on low frequency and duty cycles to keep  $T_J = +25^{\circ}C$ .
- 8. Short duration pulse test used to minimize self-heating effect.
- 9. Guaranteed by design. Not subject to product testing.

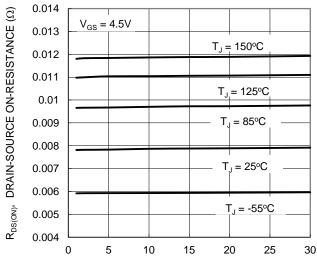
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I<sub>D</sub>, DRAIN-SOURCE CURRENT (A) Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage



I<sub>D</sub>, DRAIN CURRENT (A)
Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

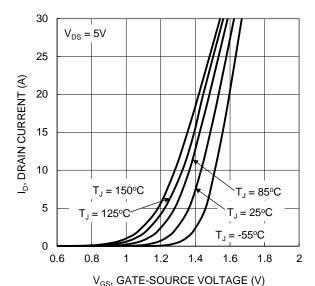


Figure 2. Typical Transfer Characteristic

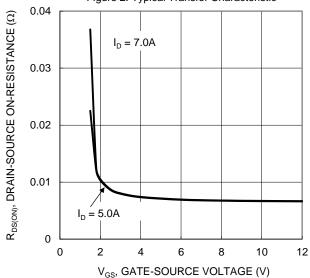


Figure 4. Typical Transfer Characteristic

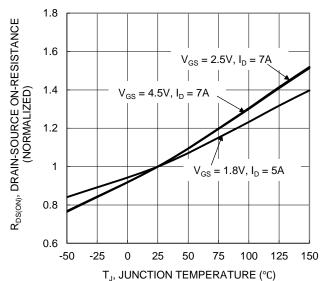


Figure 6. On-Resistance Variation with Junction
Temperature





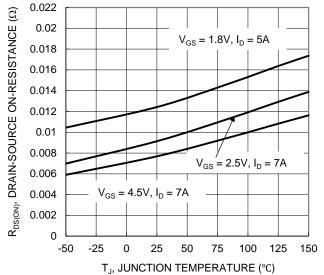
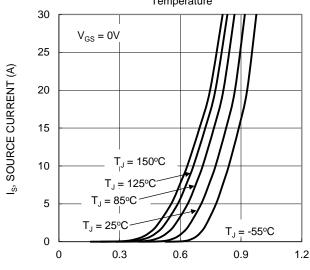


Figure 7. On-Resistance Variation with Junction Temperature



V<sub>SD</sub>, SOURCE-DRAIN VOLTAGE (V) Figure 9. Diode Forward Voltage vs. Current

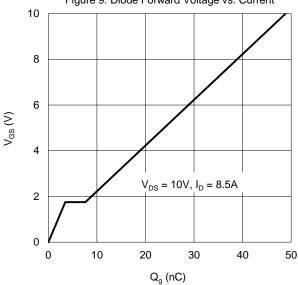


Figure 11. Gate Charge

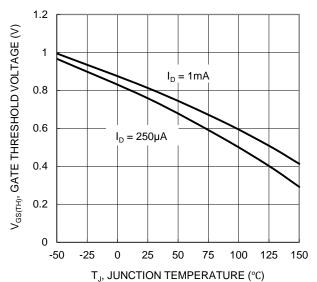


Figure 8. Gate Threshold Variation vs. Junction
Temperature

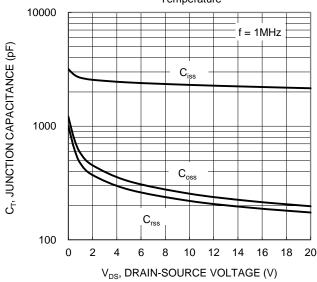
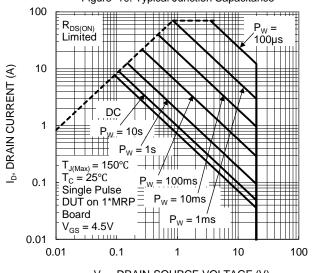


Figure 10. Typical Junction Capacitance



V<sub>DS</sub>, DRAIN-SOURCE VOLTAGE (V) Figure 12. SOA, Safe Operation Area



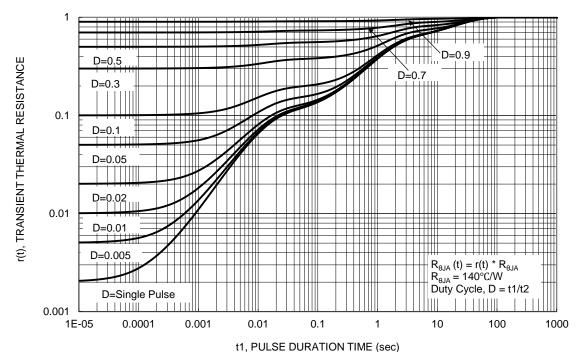


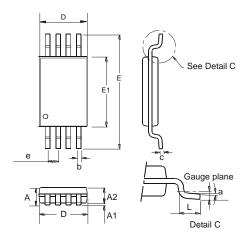
Figure 13. Transient Thermal Resistance



## **Package Outline Dimensions**

Please see http://www.diodes.com/package-outlines.html for the latest version.

#### TSSOP-8

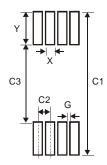


TSSOP-8					
Dim	Min	Max	Тур		
а	0.09	-	-		
Α	-	1.20	-		
A1	0.05	0.15	-		
A2	0.825	1.025	0.925		
b	0.19	0.30	-		
С	0.09	0.20	-		
D	2.90	3.10	3.025		
е	_	_	0.65		
E	_	_	6.40		
E1	4.30	4.50	4.425		
L	0.45	0.75	0.60		
All Dimensions in mm					

## **Suggested Pad Layout**

Please see http://www.diodes.com/package-outlines.html for the latest version.

#### TSSOP-8



Dimensions	Value (in mm)		
X	0.45		
Υ	1.78		
C1	7.72		
C2	0.65		
C3	4.16		
G	0.20		



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