DUAL 150mA HIGH PSRR LOW NOISE LDO WITH ENABLE

Description

The AP7342 is a dual low dropout regulator with high output voltage accuracy, low R_{DSON}, high PSRR, low output noise and low quiescent current. This regulator is based on a CMOS process.

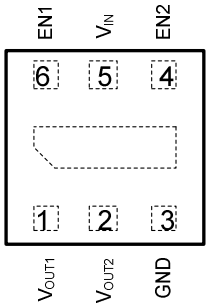
Each regulator includes a voltage reference, error amplifier, current limit circuit and an enable input to turn on/off output. With the integrated resistor network, fixed output voltage versions can be delivered.

With its low power consumption and line and load transient response, the AP7342 is well suited for low power handheld communication equipment.

The AP7342 is packaged in X2-DFN1212-6 package and allows for smallest footprint and dense PCB layout.

Pin Assignments

Top View



X2-DFN1212-6

Features

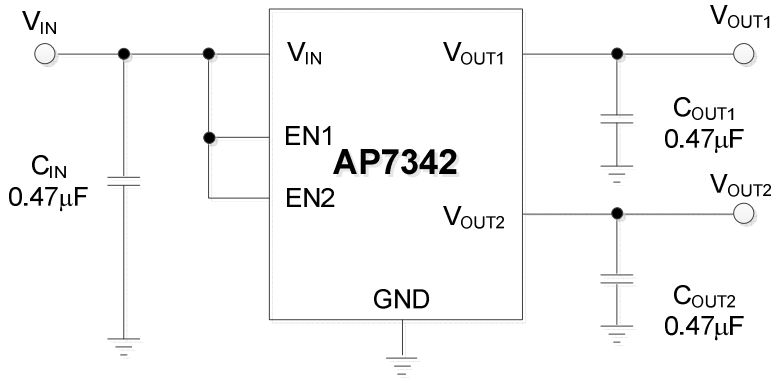
- Low V_{IN} and Wide V_{IN} Range: 1.7V to 5.25V
- Guarantee Output Current: 150mA
- V_{OUT} Accuracy ±1%
- Ripple Rejection: 75dB at 1kHz
- Low Output Noise: 60μVrms from 10Hz to 100kHz
- Quiescent Current as Low as 35μA
- V_{OUT} Fixed 1.2V to 3.6V
- **Totally Lead-Free & and Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free, Green Device (Note 3)**

Applications

- Smart Phone/PAD
- RF Supply
- Cameras
- Portable Video
- Portable Media Player
- Wireless Adapter
- Wireless Communication

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

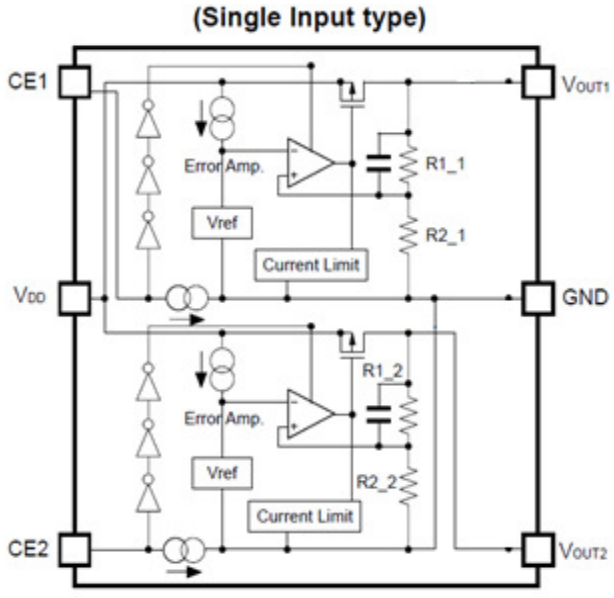
Typical Applications Circuit



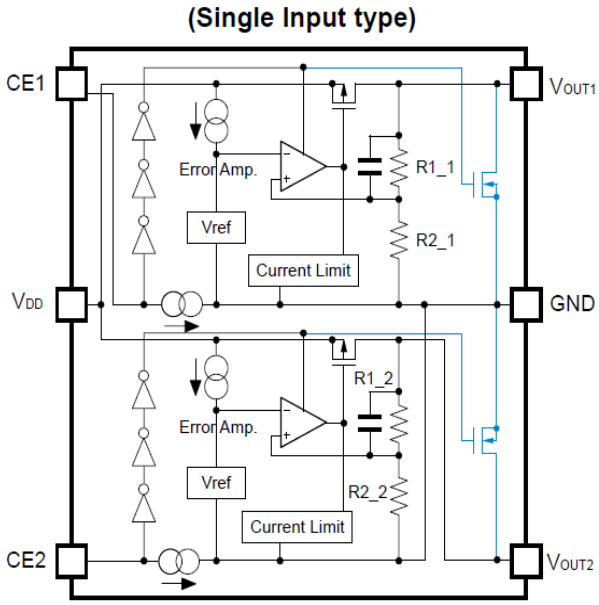
Pin Descriptions

Pin Number	Pin Name	Function
1	V_{OUT1}	Channel 1 Output Voltage Pin
2	V_{OUT2}	Channel 2 Output Voltage Pin
3	GND	Ground
4	EN2	Chanel 2 Enable Pin This pin should be driven either high or low and must not be floating. Driving this pin high enables channel 2 output, while pulling it low puts Chanel 2 regulator into shutdown mode.
5	V_{IN}	Power Input Pin
6	EN1	Chanel 1 Enable Pin This pin should be driven either high or low and must not be floating. Driving this pin high enables channel 1 output, while pulling it low puts Chanel 1 regulator into shutdown mode.
–	Thermal PAD	In PCB layout, it is preferred to use large copper area to cover this pad for better thermal dissipation, then connect this area to GND or leave it open. However, do not use it as GND electrode function alone.

Functional Block Diagram



AP7342 (No Discharge)



AP7342 (With Discharge)

Absolute Maximum Ratings (@T_A = +25℃, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	6.0	V
V_{EN}	Input Voltage at EN Pins	6.0	V
V_{OUT}	Output Voltage	-0.3 to V_{IN} +0.3	V
I_{OUT}	Output Current	180	mA
P_D	Power Dissipation	600	mW
T_A	Operating Ambient Temperature	-40 to +85	℃
T_{STG}	Storage Temperature	-55 to +125	℃

Note: 4. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions (@T_A = +25℃, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	1.7	5.25	V
I_{OUT}	Output Current	0	150	mA
T_A	Operating Ambient Temperature	-40	+85	℃

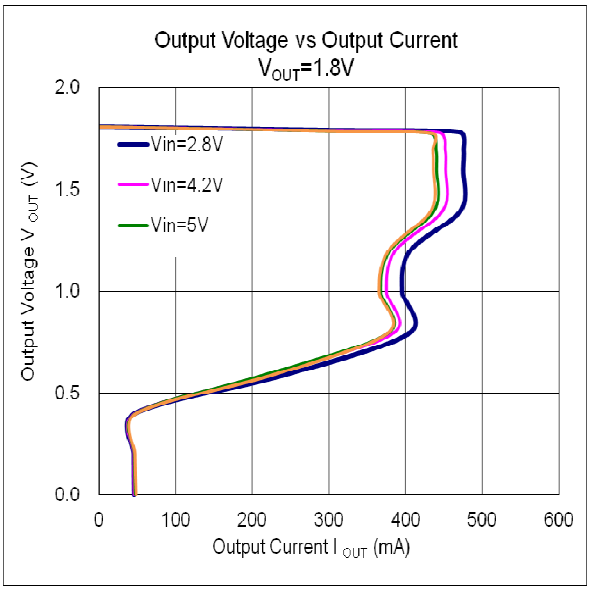
Electrical Characteristics

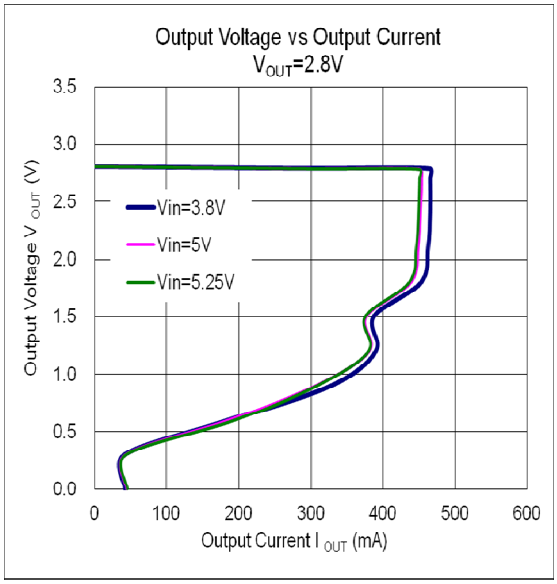
(@T_A = +25℃, V_{IN} = V_{OUT}+1V (V_{OUT} > 1.5V), V_{IN} = 2.5V (V_{OUT} ≤ 1.5V), I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1.0μF, unless otherwise specified.)

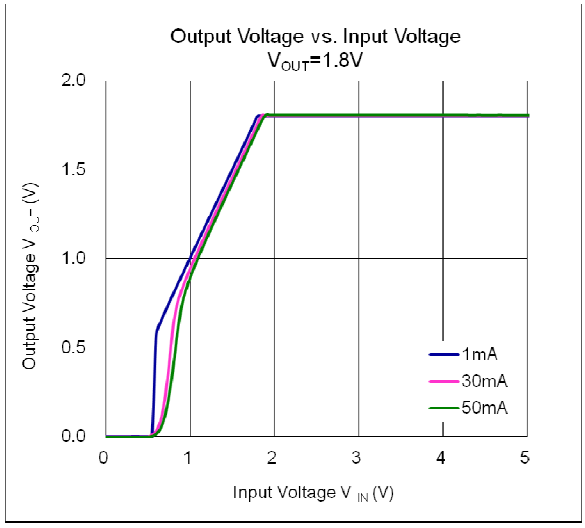
Parameter	Conditions		Min	Typ	Max	Unit
Input Voltage	T_A = -40℃ to +85℃		1.7	–	5.25	V
Output Voltage Accuracy (Note 11)	V_{IN} = ($V_{OUT-Nom}$+1.0V) to 5.25V, I_{OUT} = 1mA to 150mA	T_A = +25℃	-1	–	1	%
		T_A = -40℃ to +85℃	-1.5	–	1.5	
Line Regulation ($\Delta V_{OUT}/\Delta V_{IN}/V_{OUT}$)	V_{IN} = ($V_{OUT-Nom}$+1.0V) to 5.25V, I_{OUT} = 1.0mA		–	0.02	0.1	%/V
Load Regulation ($\Delta V_{OUT}/\Delta I_{OUT}$)	V_{IN} = $V_{OUT-Nom}$+1.0V, I_{OUT} = 1mA to 150mA		–	15	30	mV
Quiescent Current (Note 6)	Set EN1 high, set EN2 low, or set EN2 high, set EN1 low, No load		–	35	50	μA
	Set EN1/EN2 high, No load		–	70	100	μA
$I_{STANDBY}$	Set EN1/EN2 low, No load		–	0.1	1.0	μA
Output Current	–		300	–	–	mA
Fold-back Short Current (Note 7)	V_{OUT} short to ground		–	55	–	mA
PSRR (Note 8)	V_{IN} = (V_{OUT}+1V) V_{DC} + 0.2Vp-pAC, V_{OUT} ≥1.8V, I_{OUT} = 30mA	f = 1kHz	–	75	–	dB
Output Noise Voltage (Notes 8 & 9)	BW = 10Hz to 100kHz, I_{OUT} = 30mA		–	60	–	μVrms
Dropout Voltage (Note 5)	I_{OUT} = 150mA	V_{OUT} ≤ 1.2V	–	0.48	0.59	V
		1.2V < V_{OUT} ≤ 1.4V	–	0.39	0.50	
		1.4V < V_{OUT} ≤ 1.7V	–	0.35	0.44	
		1.7V < V_{OUT} ≤ 2.1V	–	0.30	0.39	
		2.1V < V_{OUT} ≤ 2.5V	–	0.26	0.34	
		2.5V < V_{OUT} ≤ 3.0V	–	0.25	0.30	
		3.0V < V_{OUT} ≤ 3.6V	–	0.22	0.29	
Output Voltage Temperature Coefficient	I_{OUT} = 30mA, T_A = -40℃ to +85℃		–	±30	–	ppm/℃
EN Input Low Voltage	–		0	–	0.5	V
EN Input High Voltage	–		1.3	–	5.25	V
EN Input Leakage	V_{EN} = 0V, V_{IN} = 5.0V or V_{EN} = 5.0V, V_{IN} = 0V		-1.0	–	1.0	μA
On Resistance of N-Channel for Auto-Discharge (Note 10)	V_{IN} = 4.0V, V_{EN} = 0V (Disabled)	D Version, Chanel 1 & 2	–	50	–	Ω

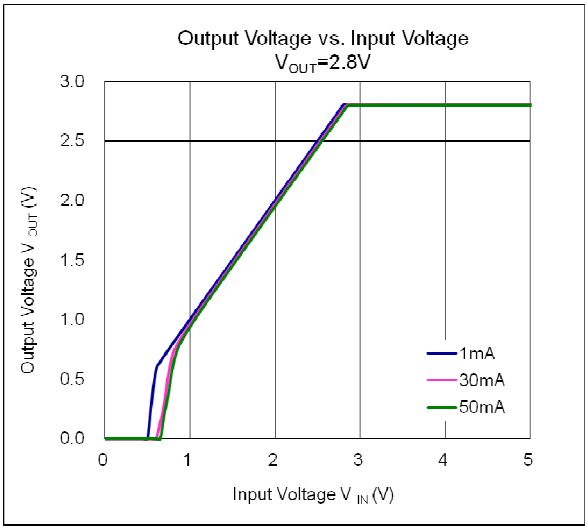
Notes:
5. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.
6. Quiescent current is defined here is the difference in current between the input and the output.
7. Short circuit current is measured with V_{OUT} pulled to GND.
8. This specification is guaranteed by design.
9. To make sure lowest environment noise minimizes the influence on noise measurement.
10. AP7342 has 2 options for output, built-in discharge and non-discharge
11. Potential multiple grades based on following output voltage accuracy.

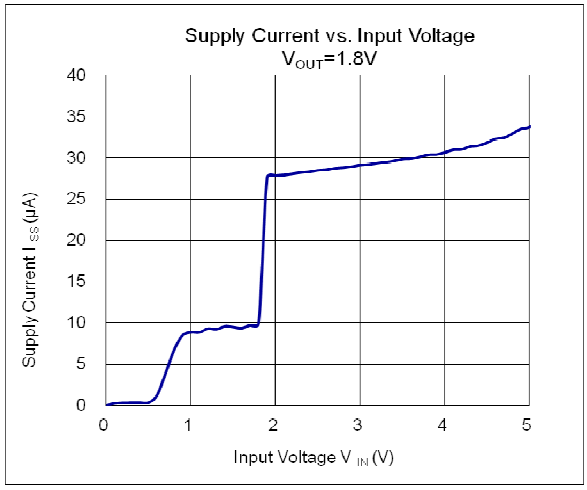
Typical Characteristics

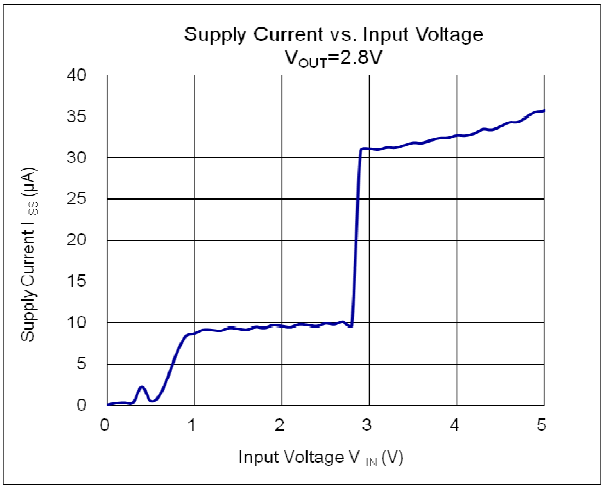












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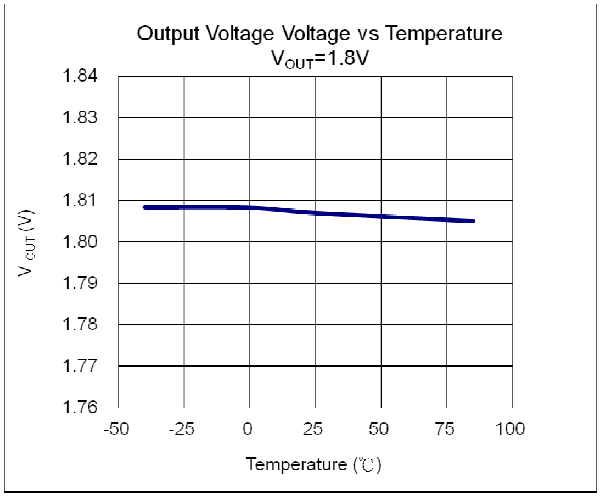

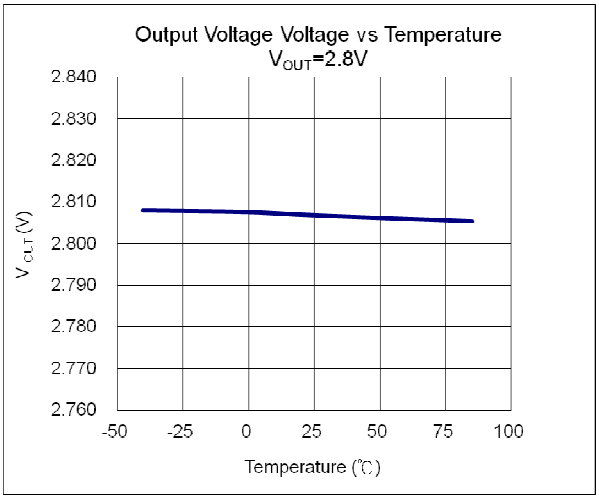

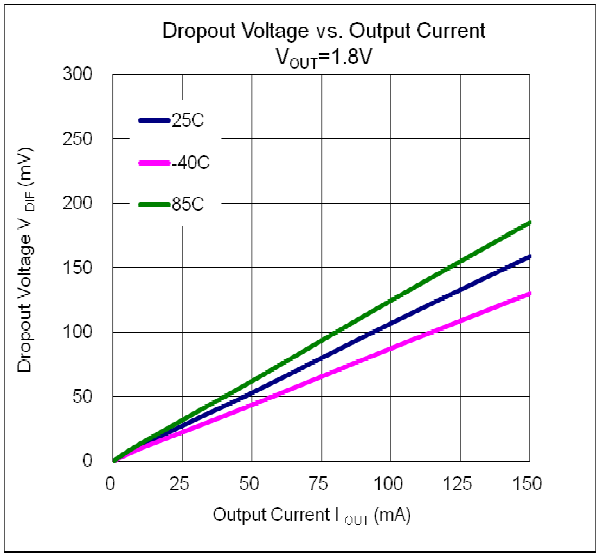

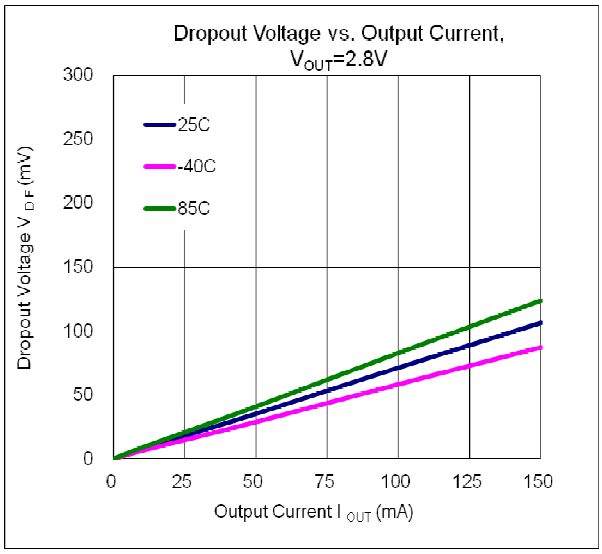

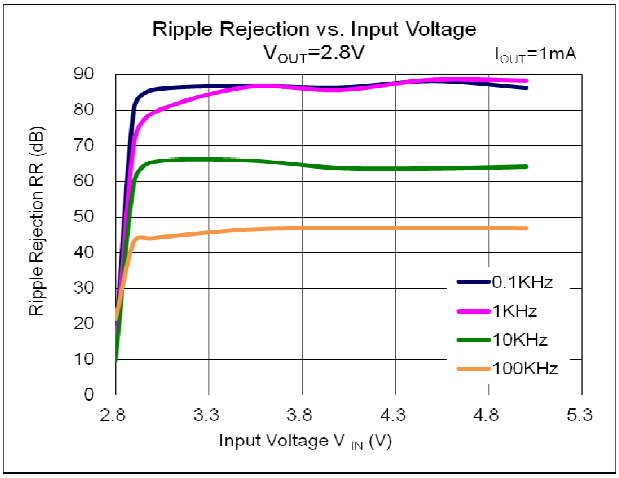

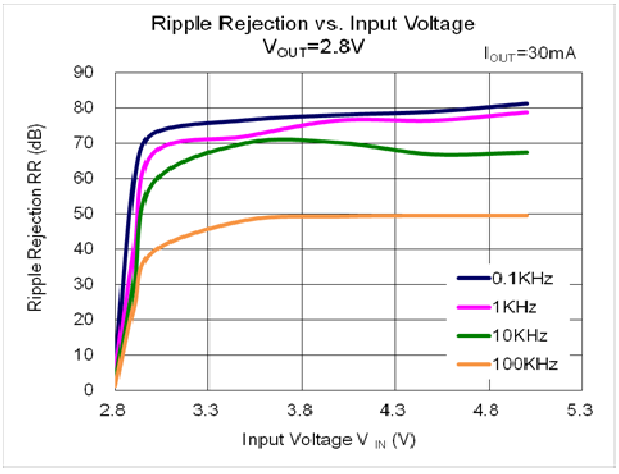

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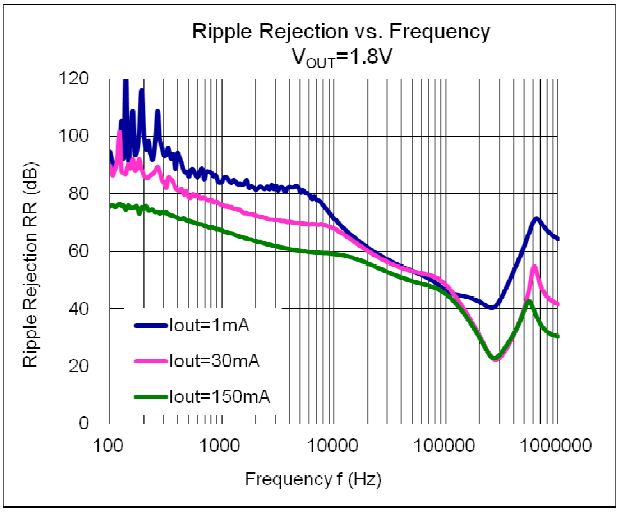
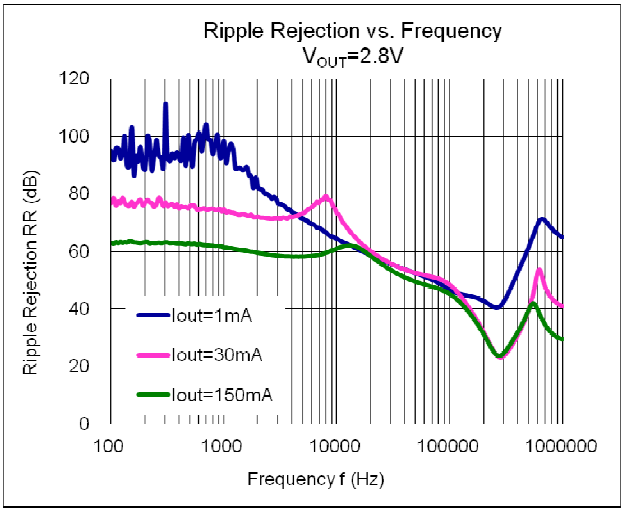
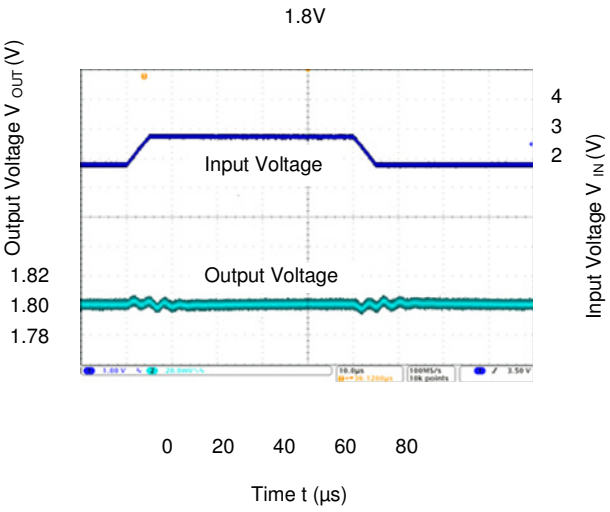
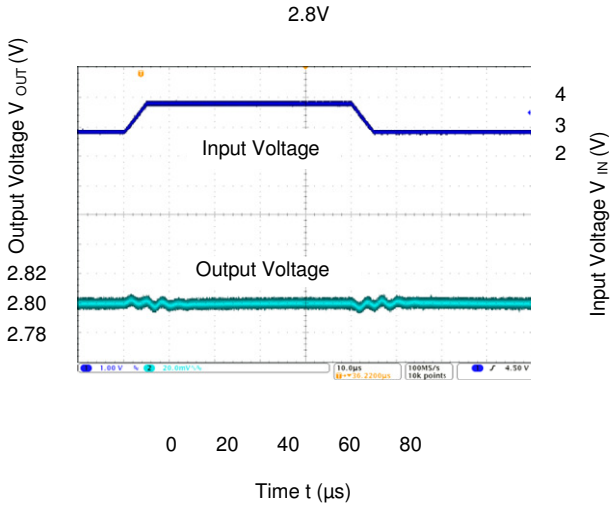




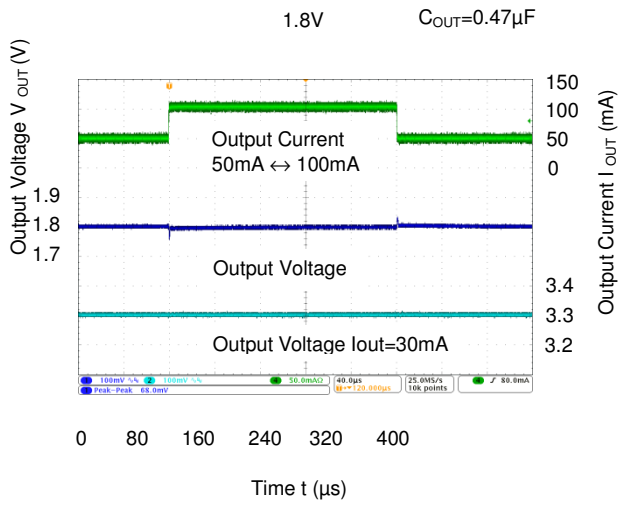
Load Transient Response Waveforms(V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT1}=C_{OUT2}=0.47μF, T_A=25℃)

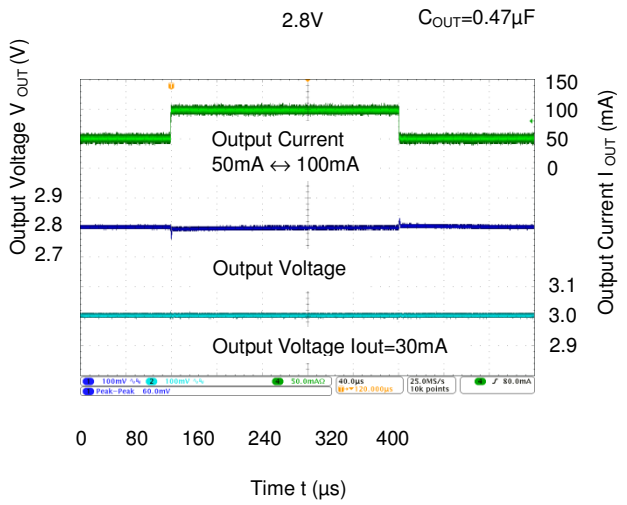


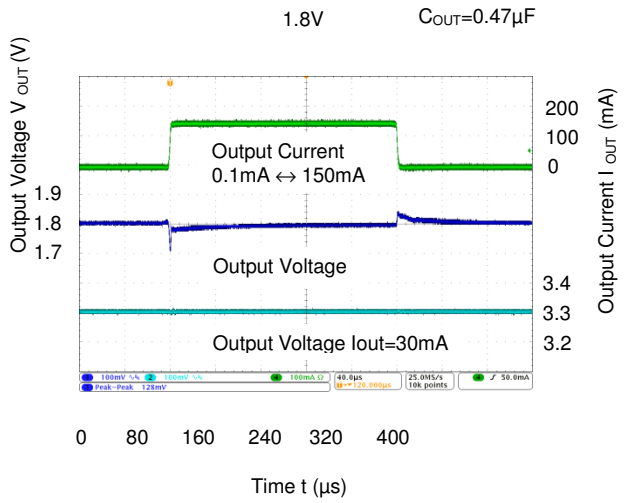


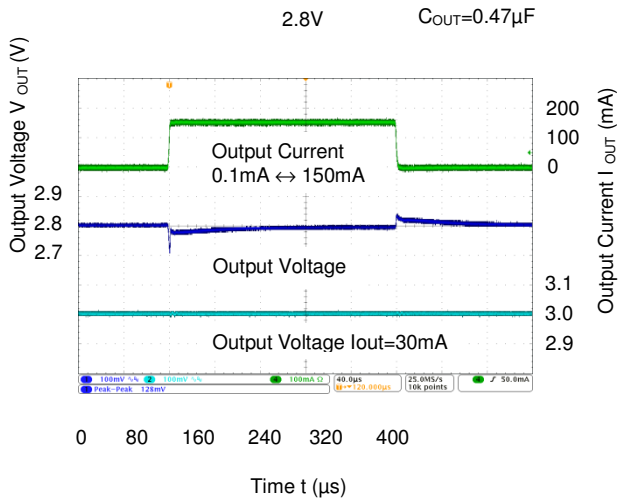
Typical Characteristics (cont.)

Load Transient Response Waveforms(V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT1}=C_{OUT2}=0.47μF, T_A = +25℃)

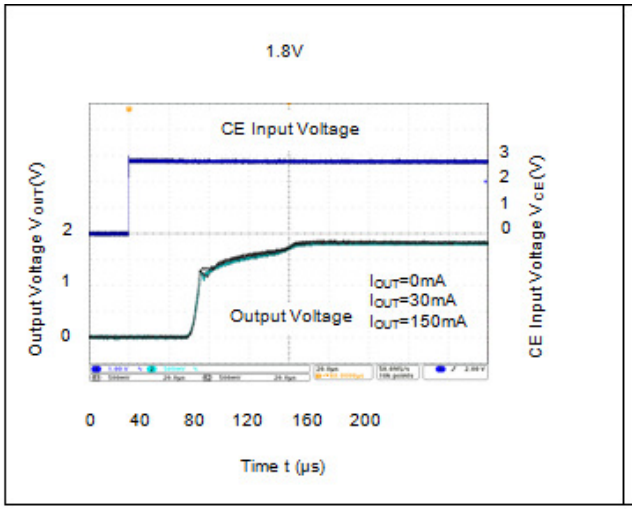


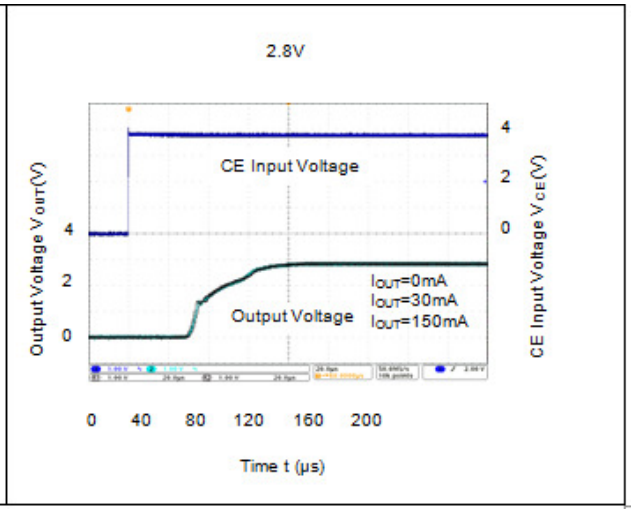






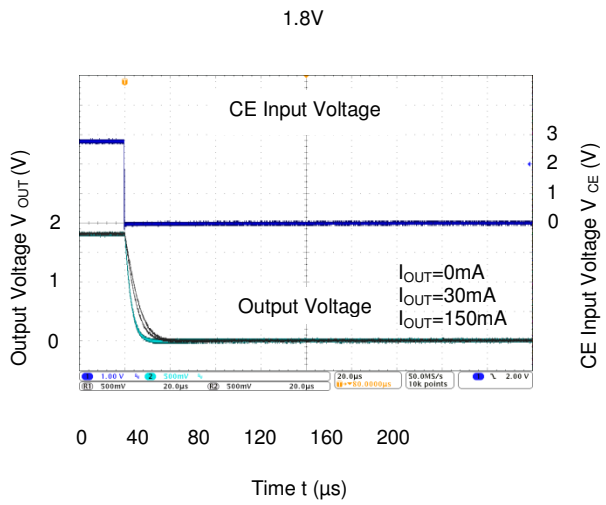
Turn On Waveform of Output Discharge versions (V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT1}=C_{OUT2}=0.47μF, T_A = +25℃)

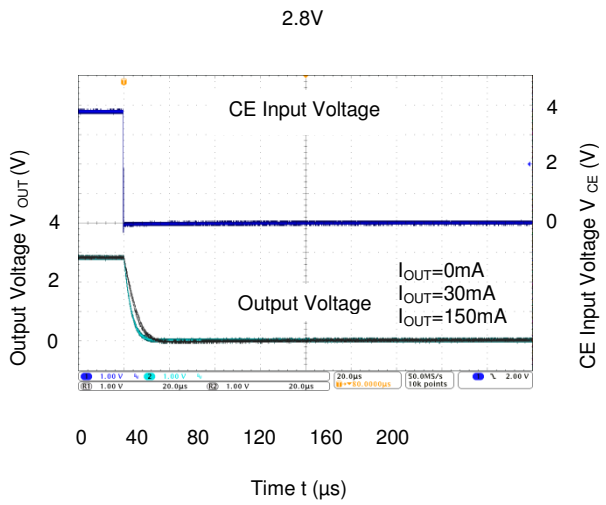




Typical Characteristics (cont.)

Turn Off Waveform of Output Discharge versions (V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT1}=C_{OUT2}=0.47μF, T_A = +25℃)





Application Information

Output Capacitor

An output capacitor (C_{OUT}) is needed to improve transient response and maintain stability. The AP7342 is stable with very small ceramic output capacitors. The ESR (Equivalent Series Resistance) and capacitance drives the selection. If the application has large load variations, it is recommended to utilize low-ESR bulk capacitors. It is recommended to place ceramic capacitors as close as possible to the load and the GND pin and care should be taken to reduce the impedance in the layout.

Input Capacitor

To prevent the input voltage from dropping during load steps, it is recommended to utilize an input capacitor (C_{IN}). A minimum 0.47μF ceramic capacitor is recommended between V_{IN} and GND pin to decouple input power supply glitch. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND pin.

Enable Control

The AP7342 is turned on by setting the EN pins high, and is turned off by pulling it low. If this feature is not used, the EN pins should be tied to V_{IN} pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pins must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section.

Short Circuit Protection

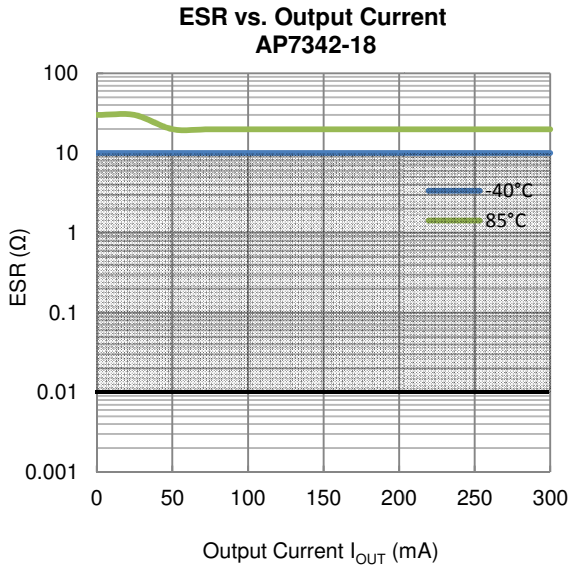
When V_{OUT} pins are short-circuit to GND, short circuit protection will be triggered and clamp the output current to approximately 60mA. This feature protects the regulator from overcurrent and damage due to overheating.

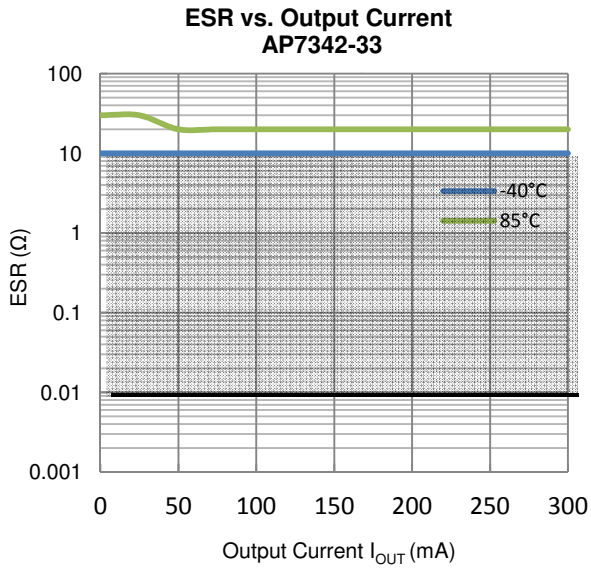
Layout Considerations

For good ground loop and stability, the input and output capacitors should be located close to the input, output, and GND pin of the device. The regulator GND pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance. Wide trace should be used for large current paths from V_{IN} to V_{OUT} and load circuit.

ESR vs. Output Current

Ceramic type output capacitor is recommended for this series; however, the other output capacitors with low ESR can also be used. The relations between I_{OUT} (Output Current) and ESR of an output capacitor are shown below. The stable region is marked as the hatched area in the graph. Measurement Conditions: Frequency Band: 10Hz to 2MHz, Temperature: –40℃ to +85℃.





Ordering Information

AP7342X XXXX FS6 – 7

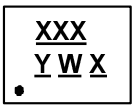
Output Discharge	CH1/CH2 Output Voltage		Package	Packing
Blank : Non-discharge	CH1	CH2	FS6 : X2-DFN1212-6	7 : Tape & Reel
D : Output Discharge	12 : 1.2V	12 : 1.2V		
	15 : 1.5V	15 : 1.5V		
	18 : 1.8V	18 : 1.8V		
	25 : 2.5V	25 : 2.5V		
	28 : 2.8V	28 : 2.8V		
	30 : 3.0V	30 : 3.0V		
	33 : 3.3V	33 : 3.3V		
	36 : 3.6V			

Device	Package Code	Packaging	7" Tape and Reel	
			Quantity	Part Number Suffix
AP7342-XXXXFS6-7	FS6	X2-DFN1212-6	5,000/Tape & Reel	-7
AP7342D-XXXXFS6-7	FS6	X2-DFN1212-6	5,000/Tape & Reel	-7

Marking Information

(1) X2-DFN1212-6

(Top View)

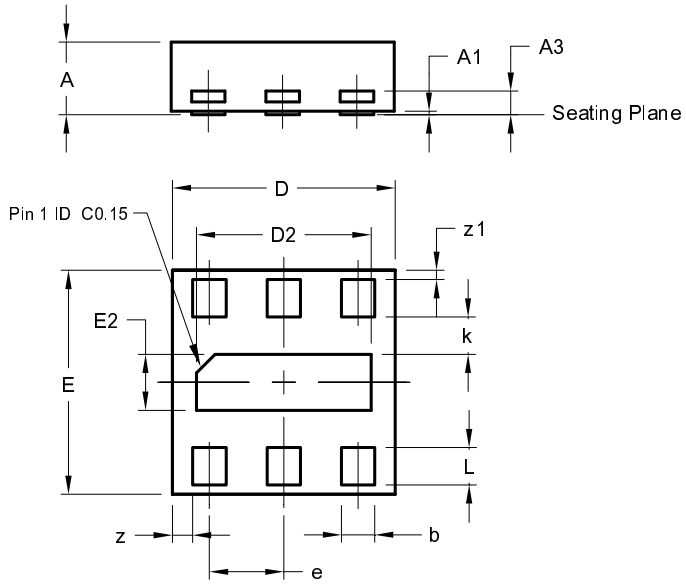


XXX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal code

Part Number	V_{OUT1}/V_{OUT2}	Package	Identification Code
AP7342-3028FS6-7	3.0V/2.8V	X2-DFN1212-6	CAA
AP7342-3328FS6-7	3.3V/2.8V	X2-DFN1212-6	CAB
AP7342D-1218FS6-7	1.2V/1.8V	X2-DFN1212-6	CAC
AP7342D-1528FS6-7	1.5V/2.8V	X2-DFN1212-6	CAD
AP7342D-1815FS6-7	1.8V/1.5V	X2-DFN1212-6	CAE
AP7342D-1818FS6-7	1.8V/1.8V	X2-DFN1212-6	CAF
AP7342D-1828FS6-7	1.8V/2.8V	X2-DFN1212-6	CAG
AP7342D-1833FS6-7	1.8V/3.3V	X2-DFN1212-6	CAH
AP7342D-2518FS6-7	2.5V/1.8V	X2-DFN1212-6	CAJ
AP7342D-2812FS6-7	2.8V/1.2V	X2-DFN1212-6	CAK
AP7342D-2818FS6-7	2.8V/1.8V	X2-DFN1212-6	CAM
AP7342D-2825FS6-7	2.8V/2.5V	X2-DFN1212-6	CAN
AP7342D-2833FS6-7	2.8V/3.3V	X2-DFN1212-6	CAP
AP7342D-3018FS6-7	3.0V/1.8V	X2-DFN1212-6	CAR
AP7342D-3028FS6-7	3.0V/2.8V	X2-DFN1212-6	CAS
AP7342D-3030FS6-7	3.0V/3.0V	X2-DFN1212-6	CAT
AP7342D-3318FS6-7	3.3V/1.8V	X2-DFN1212-6	CAU
AP7342D-3328FS6-7	3.3V/2.8V	X2-DFN1212-6	CAV
AP7342D-3330FS6-7	3.3V/3.0V	X2-DFN1212-6	CAW
AP7342D-3333FS6-7	3.3V/3.3V	X2-DFN1212-6	CAX
AP7342D-3612FS6-7	3.6V/1.2V	X2-DFN1212-6	CAY

Package Outline Dimensions (All dimensions in mm.)

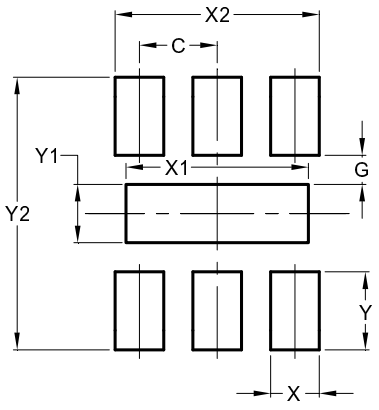
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



X2-DFN1212-6			
Dim	**Min**	**Max**	**Typ**
A	-	0.40	0.39
A1	0.00	0.05	0.020
A3	-	-	0.13
b	0.13	0.23	0.18
D	1.15	1.25	1.20
D2	0.89	0.99	0.94
E	1.15	1.25	1.20
E2	0.25	0.35	0.30
e	-	-	0.40
k	0.15	0.25	0.20
L	0.15	0.25	0.20
z	-	-	0.11
z1	-	-	0.05
All Dimensions in mm			

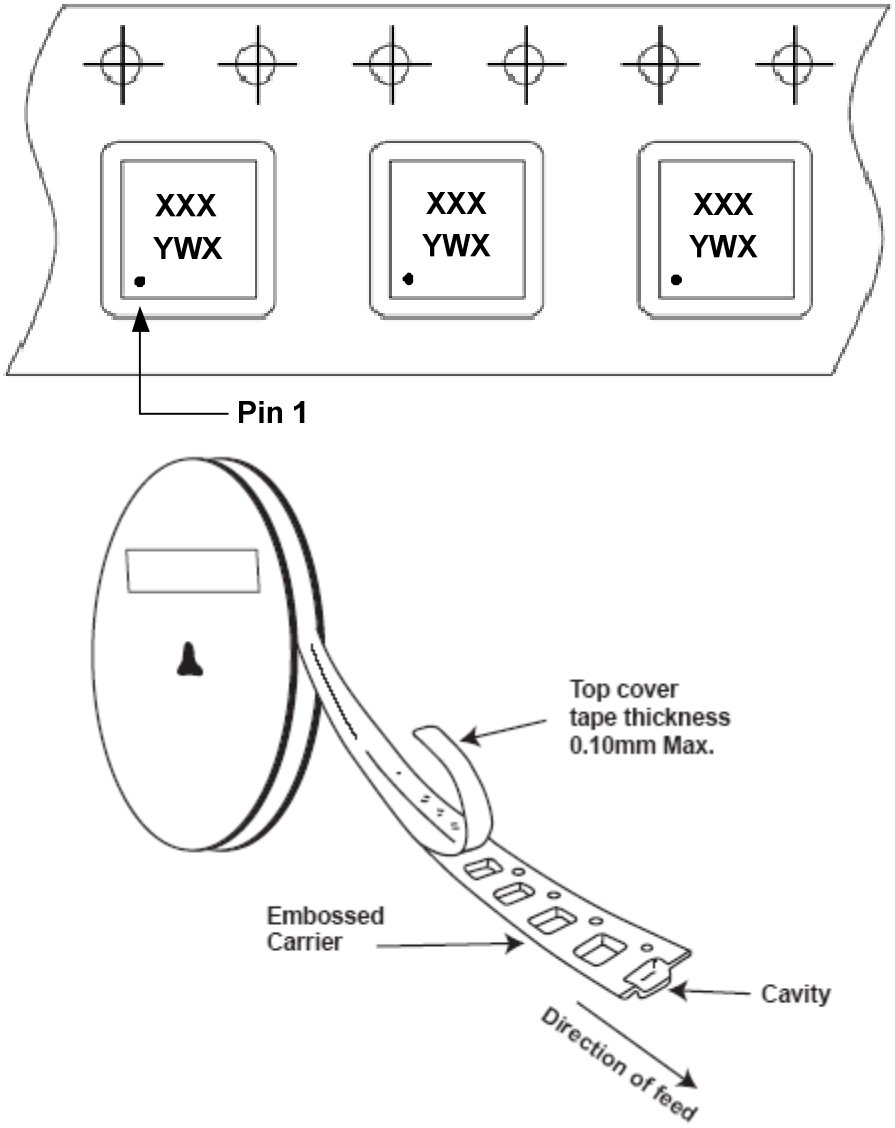
Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
C	0.400
G	0.150
X	0.250
X1	0.940
X2	1.050
Y	0.400
Y1	0.300
Y2	1.400

Tape Orientation



Note: The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf.

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