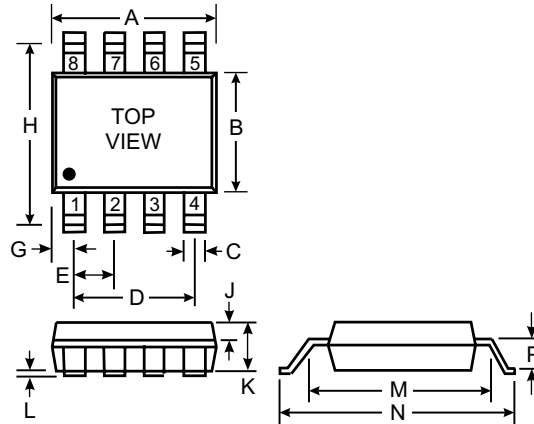


**SINGLE P-CHANNEL ENHANCEMENT MODE  
FIELD EFFECT TRANSISTOR**

**Features**

- High Cell Density DMOS Technology
- Low On-State Resistance
- High Power and Current Capability
- Fast Switching Speed
- High Transient Tolerance



SO-8		
Dim	Min	Max
A	3.94	4.19
B	3.20	3.40
C	0.381	0.495
D	2.67	3.05
E	0.89	1.02
G	0.527	0.679
J	0.41 Nominal	
K	0.94	1.09
L	0.025	0.152
M	4.37	4.62
N	4.39	4.70
P	0.939 Nominal	
All Dimensions in mm		

**Mechanical Data**

- SO-8 Plastic Case
- Terminal Connections: See Outline Drawing and Internal Circuit Diagram above

**Maximum Ratings** 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-20	V
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current	$I_D$	Note 1a Continuous @ $T_A = 25^\circ\text{C}$ Note 1a Continuous @ $T_A = 70^\circ\text{C}$ Pulsed @ $T_A = 25^\circ\text{C}$	A
Maximum Power Dissipation	$P_d$	Note 1a Note 1b Note 1c	W
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

**Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	25	$^\circ\text{C/W}$

Notes: 1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance ( $R_{\theta JC} + R_{\theta CA}$ ) where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  in this instance is  $25^\circ\text{C/W}$  but is dependent on the specific circuit board thermal design.

- 1a. With 1 in<sup>2</sup> of 2 oz. copper mounting pad  $R_{\theta JA} = 50^\circ\text{C/W}$ .
- 1b. With 0.04 in<sup>2</sup> of 2 oz. copper mounting pad  $R_{\theta JA} = 105^\circ\text{C/W}$ .
- 1c. With 0.006 in<sup>2</sup> of 2 oz. copper mounting pad  $R_{\theta JA} = 125^\circ\text{C/W}$ .

**Electrical Characteristics** <sup>25°C unless otherwise specified</sup>

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	-20	—	—	V	$V_{GS} = 0V, I_D = -25 \mu A$
Zero Gate Voltage Drain Current $T_j = 55^\circ C$	$I_{DSS}$	—	—	-1.0 -10	$\mu A$	$V_{DS} = -16V, V_{GS} = 0V$
Gate-Body Leakage, Forward	$I_{GSSF}$	—	—	100	nA	$V_{GS} = 20V, V_{DS} = 0V$
Gate-Body Leakage, Reverse	$I_{GSSR}$	—	—	-100	nA	$V_{GS} = -20V, V_{DS} = 0V$
<b>ON CHARACTERISTICS (Note 2)</b>						
Gate Threshold Voltage $T_j = 125^\circ C$	$V_{GS(th)}$	-1.0 -0.85	-2.0 -1.7	-3.0 -2.6	V	$V_{DS} = V_{GS}, I_D = -25 \mu A$
Static Drain-Source On-Resistance $T_j = 125^\circ C$	$R_{DS(ON)}$	—	0.055 0.077 0.067 0.082 0.120	0.060 0.090 0.080 0.115 0.190	$\Omega$	$V_{GS} = -10V, I_D = -5.3A$ $V_{GS} = -10V, I_D = -5.3A$ $V_{GS} = -6.0V, I_D = -3.6A$ $V_{GS} = -4.5V, I_D = -2.0A$ $V_{GS} = -4.5V, I_D = -2.0A$
On-State Drain Current	$I_{D(ON)}$	-15 -3.6	—	—	A	$V_{GS} = -10V, V_{DS} = -5.0V$ $V_{GS} = -4.5V, V_{DS} = -5.0V$
Forward Transconductance	$g_{FS}$	—	8.0	—	m	$V_{DS} = -15V, I_D = -5.3A$
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	$C_{ISS}$	—	1430	—	pF	$V_{DS} = -10V, V_{GS} = 0V$ $f = 1.0MHz$
Output Capacitance	$C_{OSS}$	—	810	—	pF	
Reverse Transfer Capacitance	$C_{RSS}$	—	375	—	pF	
<b>SWITCHING CHARACTERISTICS (Note 2)</b>						
Turn-On Delay Time	$t_{D(ON)}$	—	13	30	ns	$V_{DD} = -10V, I_D = -1A$ $V_{GEN} = -10V, R_{GEN} = 6.0\Omega$
Turn-On Rise Time	$t_r$	—	22	60	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	66	120	ns	
Turn-Off Fall Time	$t_f$	—	28	100	ns	
Total Gate Charge	$Q_g$	—	38	—	nC	$V_{DS} = -10V, I_D = -5.3A.$ $V_{GS} = -10V$
Gate-Source Charge	$Q_{gs}$	—	3.0	—	nC	
Gate-Drain Charge	$Q_{gd}$	—	12	—	nC	
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
Max Continuous Drain-Source Diode Forward Current	$I_S$	—	—	-2.2	A	
Drain-Source Diode Forward Voltage	$V_{SD}$	—	-1.04	-1.2	V	$V_{GS} = 0V, I_S = -5.3A$ (Note 2)
Reverse Recovery Time	$t_{rr}$	—	80	100	ns	$V_{GS} = 0V, I_F = -5.3A,$ $di_F/dt = 100A/\mu s$

Note: 2. Pulse Test width  $\leq 300 \mu s$ , duty cycle  $\leq 2\%$ .

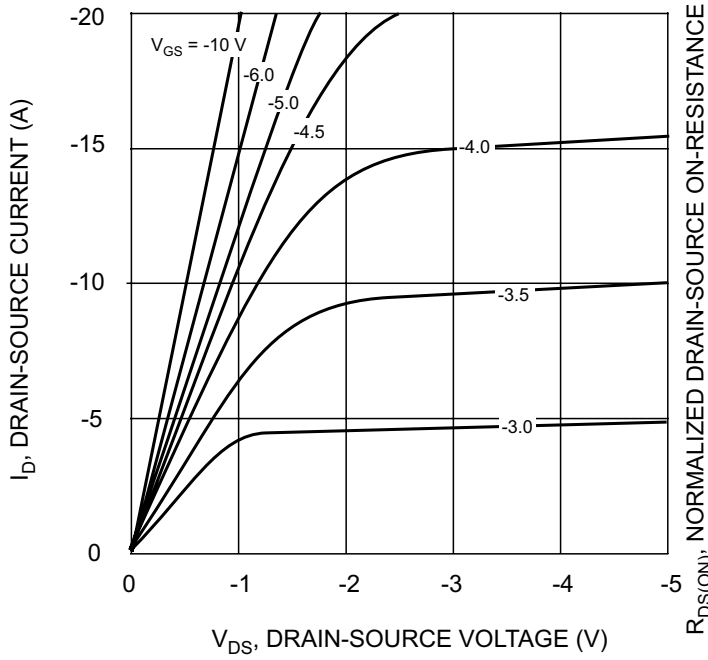


Fig. 1, On-Region Characteristics

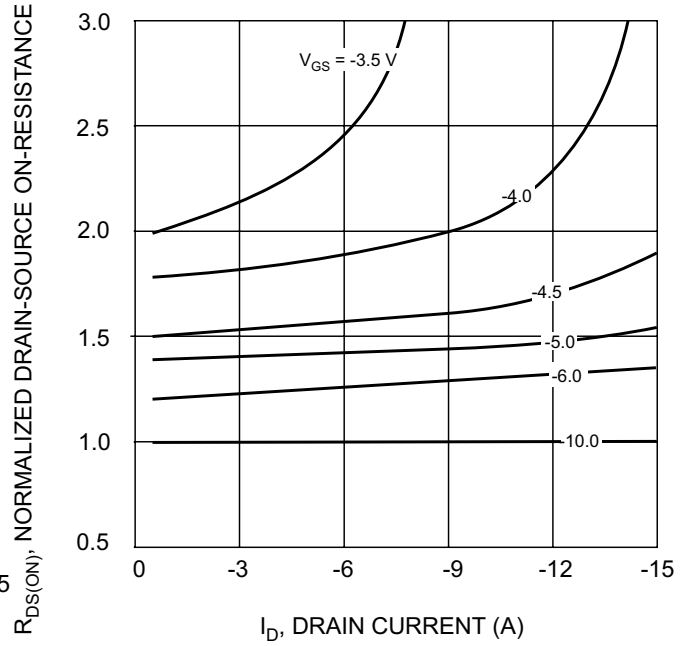


Fig. 2, On-Resistance vs Gate Voltage & Drain Current

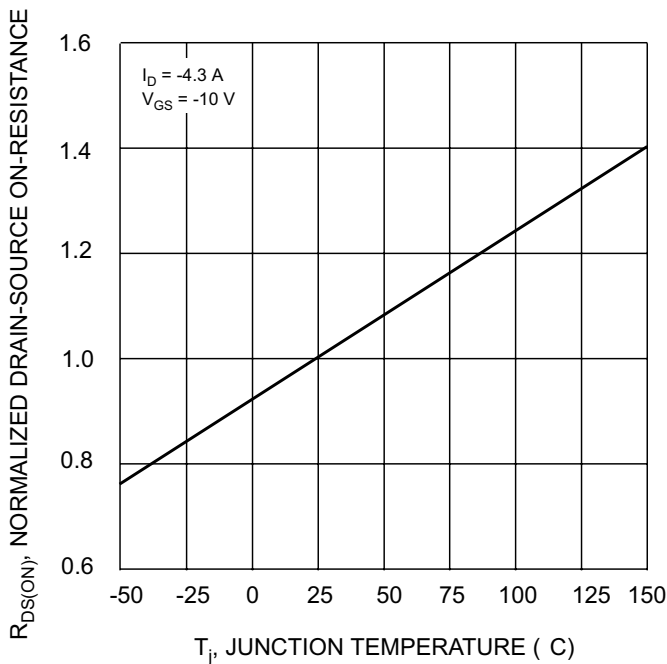


Fig. 3, On-Resistance vs Junction Temperature

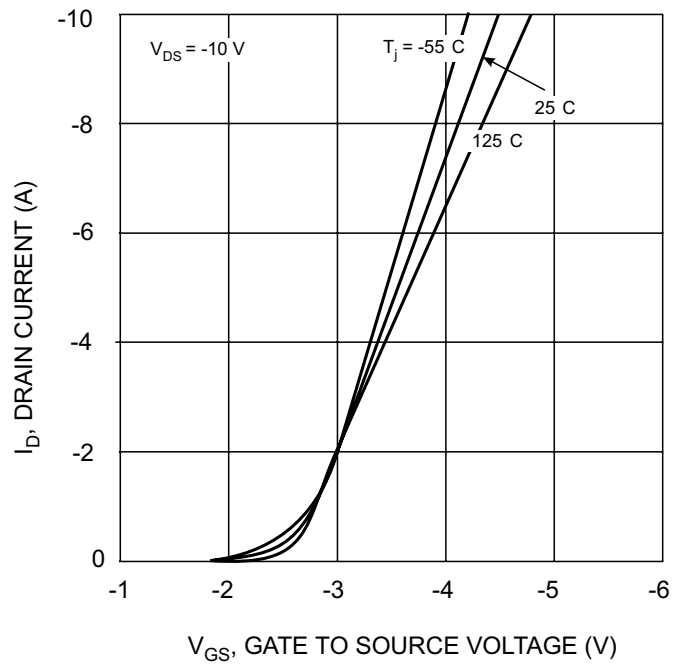
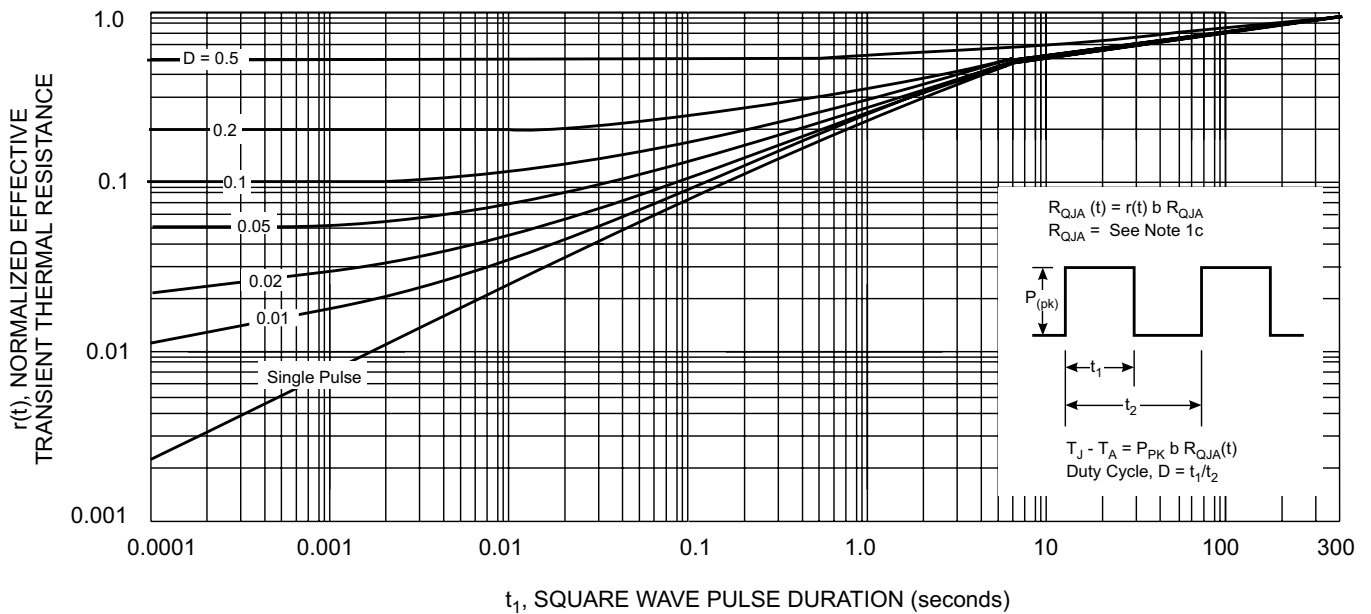
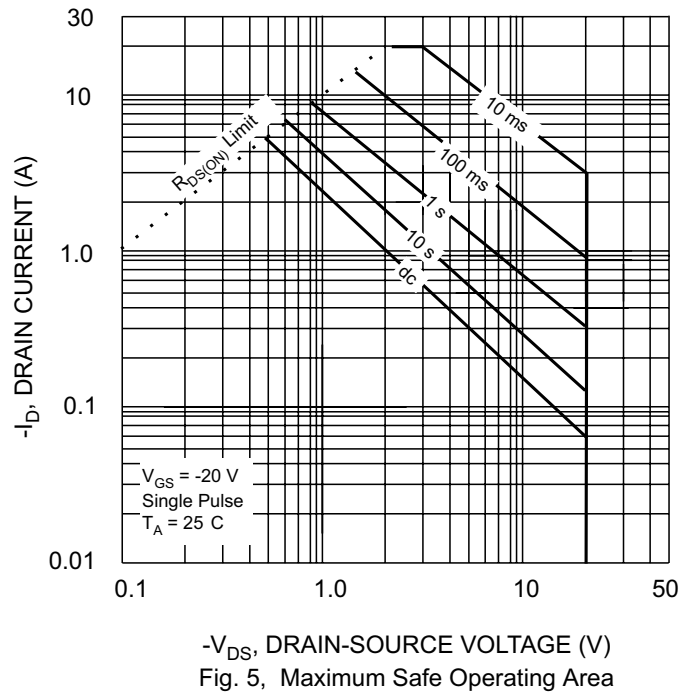


Fig. 4, Transfer Characteristics



Remark: Thermal characterization performed under conditions of Note 1c. Better thermal design such as shown in Notes 1a and 1b or 1d will offer lower  $R_{\theta JA}$  values and allow junction to reach thermal equilibrium sooner.

单击下面可查看定价，库存，交付和生命周期等信息

[>>Diodes Incorporated\(达达科技\(美台\)\)](#)