Low Power Networking Clock Generator

Features

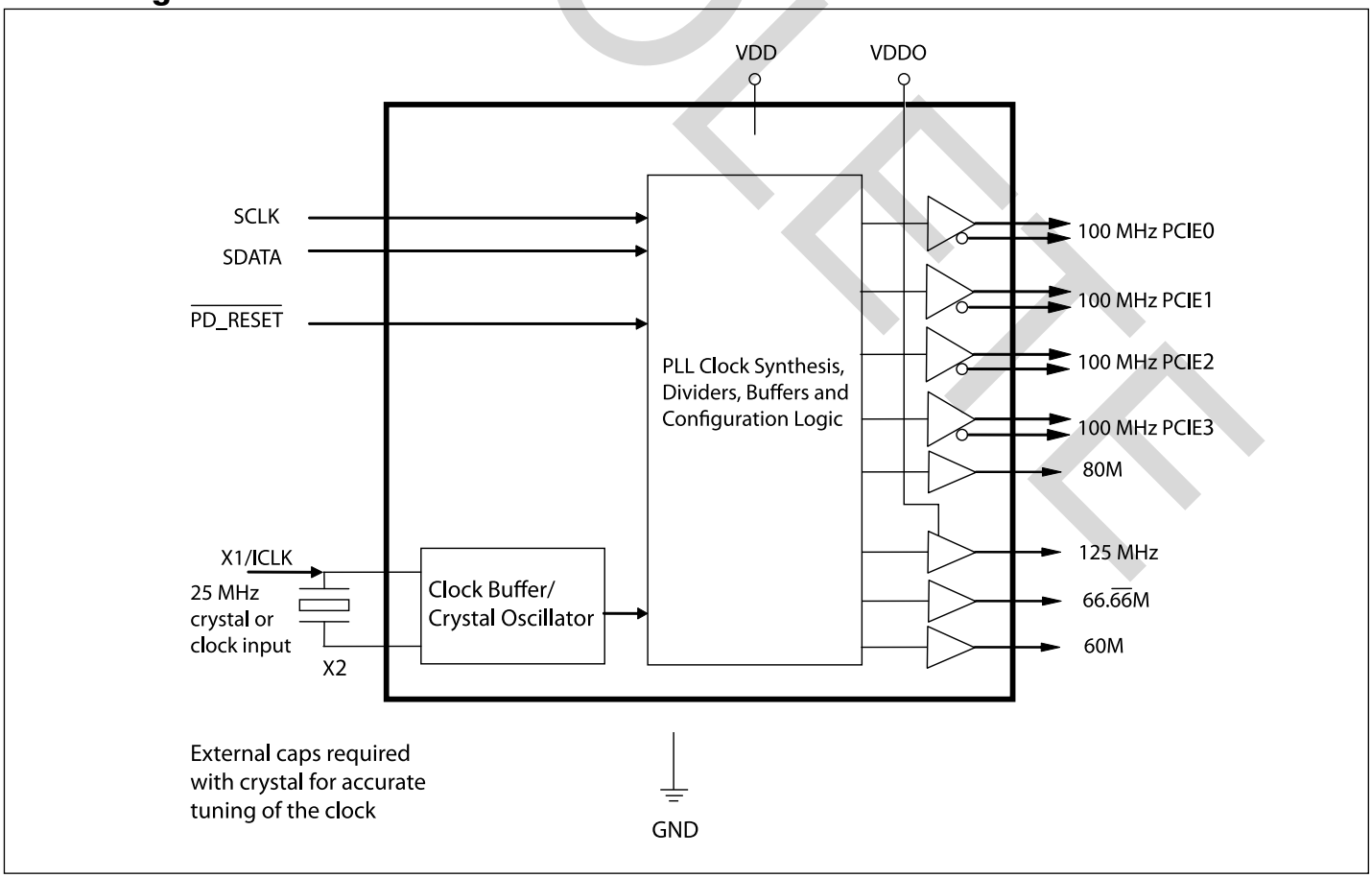
- 25 MHz crystal or clock input
- Four differential 100 MHz PCI-Express clock outputs – Low power HCSL
- Spread spectrum capability on all 100 MHz PCI-e clock outputs with -0.5% down spread
- One single-ended 66.66 MHz output
- One single-ended 125 MHz output for Gigabit Ethernet at 2.5V
- One single-ended 80 MHz output with selectable down spread
- 40-pin TQFN package
- Operating voltage 3.3 V ±5%
- Industrial temperature (-40 to +85°C)

Description

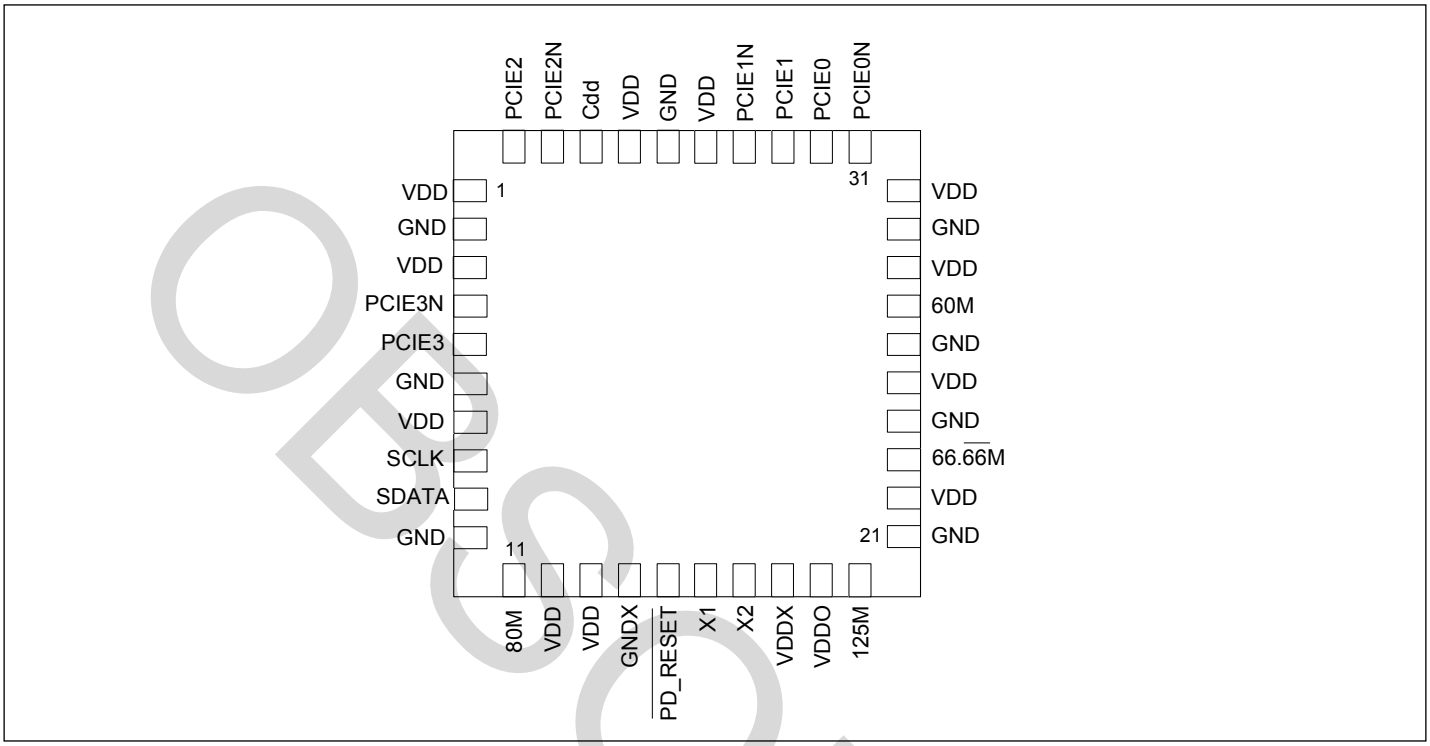
The PI6C49018 is a clock generator device intended for PCI-Express/networking applications. The device includes four 100 MHz differential outputs for PCI-Express with low power HCSL structure, one CMOS 125 MHz output, and one CMOS 66.66 MHz, and one CMOS 80 MHz output with spread spectrum.

Using a serially programmable SMBus interface, the PI6C49018 incorporates spread spectrum modulation on the four 100 MHz PCI-Express outputs with -0.5% down spread and the 80 MHz output with selectable down spread.

Block Diagram



Pin Configuration



Pin Description

Pin#	Pin Name	Pin Type	Pin Description
1	VDD	Power	3.3V Supply Pin
2	GND	Power	Ground
3	VDD	Power	3.3V Supply Pin
4	PCIE3N	Output	Differential 100 MHz PCI Express Clock output
5	PCIE3	Output	Differential 100 MHz PCI Express Clock output
6	GND	Power	Ground
7	VDD	Power	3.3V Supply Pin
8	SCLK	Input	SMBus clock input
9	SDATA	I/O	SMBus data input
10	GND	Power	Ground
11	80M	Output	80 MHz LVCMOS output. Tri-state with weak pull-down when disabled
12	VDD	Power	3.3V Supply Pin
13	VDD	Power	3.3V Supply Pin
14	GNDX	Power	Ground

Pin Description

Pin#	Pin Name	Pin Type	Pin Description
15	$\overline{\text{PD\_RESET}}$	Input	Global reset input powers down PLLs plus tri-states outputs and sets the I2C tables to their default state when pulled low. Controlled by external POR
16	X1	XI	Crystal input. Connect to 25 MHz fundamental mode crystal or clock
17	X2	XO	Crystal output. Connect to 25 MHz fundamental mode crystal. Float for clock input
18	VDDX	Power	3.3V Supply Pin for oscillator
19	VDDO	Power	125 MHz output supply voltage. Connect to +2.5 V
20	125M	Output	125 MHz, +2.5 V LVCMOS output. Tri-stated with a weak pull-down when disabled
21	GND	Power	Ground
22	VDD	Power	3.3V Supply Pin
23	66.$\overline{66}$M	Output	66.$\overline{66}$ MHz LVCMOS output. Tri-stated with a weak pull-down when disabled
24	GND	Power	Ground
25	VDD	Power	3.3V Supply Pin
26	GND	Power	Ground
27	60M	Output	60 MHz LVCMOS output. Tri-state with weak pull-down when disabled
28	VDD	Power	3.3V Supply Pin
29	GND	Power	Ground
30	VDD	Power	3.3V Supply Pin
31	PCIE0N	Output	Differential 100 MHz PCI Express Clock output
32	PCIE0	Output	Differential 100 MHz PCI Express Clock output
33	PCIE1	Output	Differential 100 MHz PCI Express Clock output
34	PCIE1N	Output	Differential 100 MHz PCI Express Clock output
35	VDD	Power	3.3V Supply Pin
36	GND	Power	Ground
37	VDD	Power	3.3V Supply Pin
38	Cdd	Input	Input pin for off chip bypass capacitor. Connect to 0.01 µF capacitor
39	PCIE2N	Output	Differential 100 MHz PCI Express Clock output
40	PCIE2	Output	Differential 100 MHz PCI Express Clock output

Selection Table 1 – 80M Spread Spectrum

SS1	SS0	SSC
0	0	-1%
0	1	OFF
1	0	-0.5%
1	1	-0.75%

NOTE: Refer to Byte0 control register.
Default setting is SS1:SS0 = 01

Serial Data Interface (SMBus)

This part is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	0	0	1	0/1

How to Write

1 bit	8 bits	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	D2H	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	…	Data Byte N - 1	Ack	Stop bit

Note:

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

How to Read (M: abbreviation for Master or Controller; S: abbreviation for slave/clock)

1 bit	8 bits	1 bit	8 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	…	8 bits	1 bit	1 bit
M: Start bit	M: Send "D2h"	S: sends Ack	M: send starting databyte location: N	S: sends Ack	M: Start bit	M: Send "D3h"	S: sends Ack	S: sends # of data bytes that will be sent: X	M: sends Ack	S: sends starting data byte N	M: sends Ack	…	S: sends data byte N+X-1	M: Not Acknowledge	M: Stop bit

Byte 0: Spread Spectrum Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Spread Select for 100 MHz push-pull PCI-Express clocks	RW	0	All 100MHz PCI-Express outputs	0=spread off 1 = -0.5% down spread
6	Enables hardware or software control of OE bits (see Byte 0-Bit 6 and Bit 5 Functionality table)	RW	0	$\overline{\text{PD\_RESET}}$, bit 5	0 = hardware cntl 1 = software ctrl
5	Software $\overline{\text{PD\_RESET}}$ bit. Enables or disables all outputs. (see Byte 0-Bit 6 and Bit 5 Functionality table)	RW	1	All outputs	0 = disabled 1 = enabled
4	Spread Select for 80MHz SS1	RW	0	80M	See Table 1 on Page4
3	Spread Select for 80MHz SS0	RW	1		
2	OE for 66.66 MHz output	RW	1	66.66M	0 = disabled 1 = enabled
1	Reserved	R	-	-	-
0	OE for single-ended 125MHz	RW	1	Single-ended 125MHz	0 = disabled 1 = enabled

Byte 0: Bit 6 and Bit 5 Functionality

Bit 6	Bit 5	Description
0	X	($\overline{\text{PD\_RESET}}$= "H" will enable all outputs; SMBus cannot control each output.)
1	0	Disables all outputs and tri-states the outputs, $\overline{\text{PD\_RESET}}$ HW pin/signal = DO NOT CARE
1	1	Enable outputs according to the SMBus default values; SMBus can control each output. $\overline{\text{PD\_RESET}}$ HW pin/signal = DO NOT CARE

Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	OE for 80 MHz output	RW	1	80MHz	0 = disabled 1 = enabled
6 to 0	Reserved	R	-	-	-

Byte 2: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	-	-	-

Byte 3: Spread Spectrum Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	OE for 60MHz output	RW	0	60M	1 = enabled 0 = disabled
6	Reserved	R	-	-	-
5	OE for 100MHz HCSL PCI-Express output PCIE3	RW	0	100MHz HCSL PCI-Express output PCIE3	1 = enabled 0 = disabled
4	OE for 100MHz HCSL PCI-Express output PCIE2	RW	1	100MHz HCSL PCI-Express output PCIE2	1 = enabled 0 = disabled
3	Reserved	R	-	-	-
2	OE for 100MHz HCSL PCI-Express output PCIE1	RW	1	100MHz HCSL PCI-Express output PCIE1	1 = enabled 0 = disabled
1	OE for 100MHz HCSL PCI-Express output PCIE0	RW	1	100MHz HCSL PCI-Express output PCIE0	1 = enabled 0 = disabled
0	Reserved	R	-	-	-

Byte 4: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	-	-	-

Byte 5: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Revision ID bit 3	R	0	-	-
6	Revision ID bit 2	R	0	-	-
5	Revision ID bit 1	R	0	-	-
4	Revision ID bit 0	R	0	-	-
3	Vendor ID bit 3	R	0	-	-
2	Vendor ID bit 2	R	0	-	-
1	Vendor ID bit 1	R	0	-	-
0	Vendor ID bit 0	R	0	-	-

Byte 6: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	-	-	-

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Maximum Supply Voltage, V_{DD}	7V
All Inputs and Outputs	–0.5V to V_{DD} +0.5V
Ambient Operating Temperature	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Junction Temperature	125°C
Peak Soldering Temperature	260°C
ESD Protection (HBM)	2000V

Note:
Stresses above the ratings listed below can cause permanent damage to the PI6C49018. These ratings, which are standard values for Pericom commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Recommended Operation Conditions

Parameters	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.135	3.3	+3.465	V
Output Supply Voltage, V_{DDO}	+2.25		+3.6	V
Minimum Pulse Width of $\overline{PD\_RESET}$ Input	100			ns

DC Electrical Characteristics

Unless otherwise specified, V_{DD}=3.3V±10%, V_{DDO}=2.5V,Ambient Temperature –40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Supply Voltage	V_{DD}		3.135	3.3	3.465	V
Output Supply Voltage	V_{DDO}		2.25	2.5	3.6	
Input High Voltage	V_{IH}	X1/SCLK, SDATA	2		V_{DD}	
Input Low Voltage	V_{IL}	X1/SCLK, SDATA	–0.3		0.8	
Operating Supply Current	I_{DD}	No load, all supply pins, $\overline{PD\_RESET}$ = 1	50	75	105	mA
IDD at Output Disable Condition	I_{DDPD}	$\overline{PD\_RESET}$ = 0		1		
Short Circuit Current	I_{OS}	All single-ended clocks		±35		
Internal Pull-Up/Pull-Down Resistor	R_{PU}/R_{PD}	$\overline{PD\_RESET}$		240		kΩ
		All single-ended clocks		110		
Output Capacitance	Z_O			30		pF
Input Capacitance	C_{IN}	All input pins		6		Ω

Electrical Characteristics - Single-Ended

Unless otherwise specified, V_{DD}=3.3V±10%, V_{DDO}=2.5V, Ambient Temperature –40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Clock Frequency	F_{IN}			25		MHz
Output Frequency Error				0		ppm
Output Rise Time	t_{OR}	At V_{DD}/2		0.5	1	ns
		0.7 V to 1.7V 125 MHz			0.4	
Output Fall Time	t_{OF}	At V_{DD}/2		0.5	1	
Output Clock Duty Cycle		Measured at V_{DD}/2, 125MHz	47	50	53	%
		Measured at V_{DD}/2, all other outputs	45	50	55	
Output High Voltage	V_{OH}	I_{OH} = -4mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -8mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Peak-to-Peak Jitter		66.$\overline{66}$MHz clock output		±150		ps
		125MHz clock output		±100		
		60MHz clock output			200	
Cycle-to-Cycle Jitter		125MHz clock output			±100	
		60M/66.$\overline{66}$M/80MHz clock output			±250	
Phase Noise		60M/66.$\overline{66}$ MHz, 500 kHz offset	-100			dB
Modulation Rate		80MHz clock output		32	60	kHz
Clock Stabilization Time from Power Up		$\overline{\text{PD\_RESET}}$ goes high to 1% of final frequency	3		10	ms

Note 1: CL = 15 pF
Note 2: Cycle-to-cycle jitter is measured at 25°C.
Note 3: Spread OFF.

Electrical Characteristics - 100MHz Differential HCSL Outputs

Unless otherwise specified, V_{DD}=3.3V±10%, Ambient Temperature –40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Frequency					100	MHz
Cycle-to-Cycle Jitter	$T_{CC/Jitter}$				150	ps
Peak-to-Peak Phase Jitter	$T_{Jø}$	PCIe Gen1 filter function			86	
Spread Range				-0.5	0	%
Spread Rate				32	0	kHz
Duty Cycle	T_{DC}		45	50	55	%
Clock Stabilization from Power Up				3.5		ms
Rising Edge Rate		Note3, 4	0.6		4.0	V/ns
Falling Edge Rate		Note3, 4	0.6		4.0	V/ns
Rise-Fall Matching		Note3, 11		20%		
Output Skew	T_{OSKEW}	V_T = 50%(measurement threshold), Intra-pair skew			50	ps
		V_T = 50%(measurement threshold), Inter-pair skew			200	ps
Clock Source DC Impedance(Zo)	Z_{C-DC}			17		Ω
High-Level Output Voltage	V_{OH}	Note2 (Rs = 33ohm)	0.65	0.71	0.85	V
Low-Level Output Voltage	V_{OL}		-0.20	0	0.05	V
Absolute Crossing Point Voltage	V_{CROSS}	Note2, 5, 6	0.25		0.55	V
Variation of V_{CROSS} over all rising clock edges	V_{CROSS} Delta	Note2, 5, 8			140	mV
Average Clock Period Accuracy	T_{PERIOD} AVG	Note3, 9, 10	-300		2800	ppm
Absolute Period (including jitter and spread spectrum)	T_{PERIOD} ABS	Note3, 7	9.847		10.203	ns

NOTE:1.Measured at the end of an 8-inch trace with a 5pF load.

2.Measurement taken from a single-ended waveform.

3.Measurement taken from a differential waveform.

4.Measured from -150 mV to +150 mV on the differential waveform. The signal is monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.

5.Measured at crossing point where the instantaneous voltage value of the rising edge of 100M+ equals the falling edge 100M-.

6.Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

7.Defines as the absolute minimum or maximum period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation.

8.Defined as the total variation of all crossing voltages of rising 100M+ and falling 100M-.

9.Refer to section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding PPM considerations.

10.PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100 MHz exactly or100 Hz. For 300 PPM there is an error budget of 100Hz/PPM * 300 PPM = 30 kHz. The period is measured with a frequency counter with measurement window set at 100 ms or greater. With spread spectrum turned off the error is less than ±300 ppm. With spread spectrum turned on there is an additional +2500 PPM nominal shift in maximum period resulting from the -0.5% down spread.

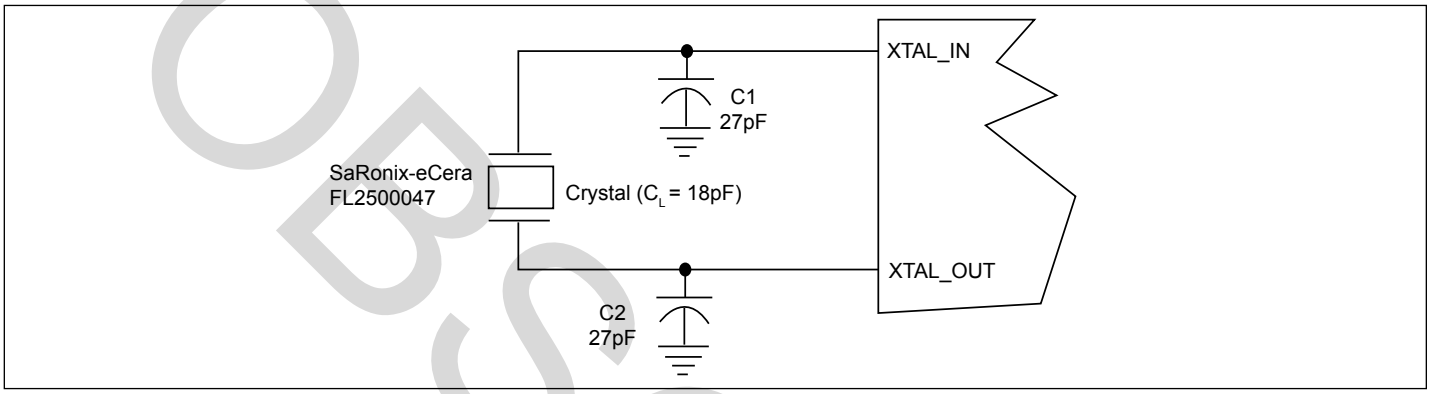
11.Matching applies to rising edge rate for PCIe and falling edge rate for PCIeN. It is measured using a ±75 mV window centered on the median cross point where

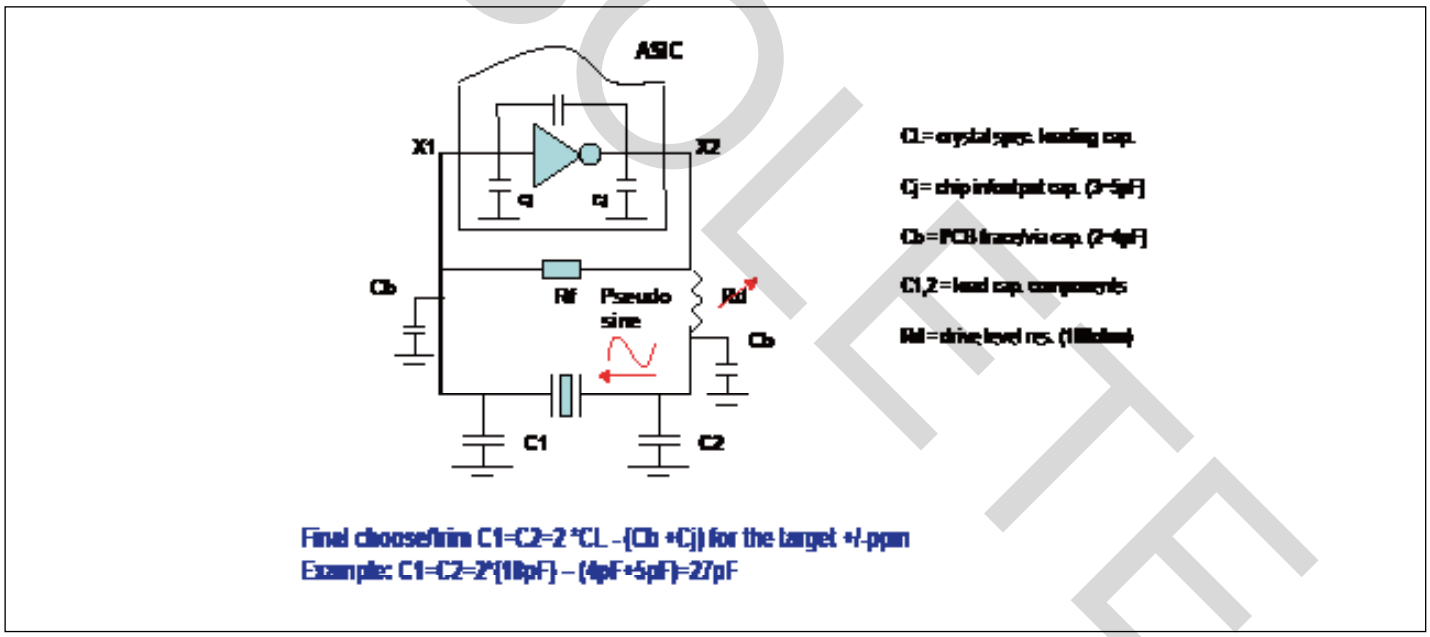
Application Notes

Crystal circuit connection

The following diagram shows PI6C49018 crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1= 27pF, C2= 27pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

Crystal Oscillator Circuit





Recommended Crystal Specification

Pericom recommends:

a) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

b) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

Configuration test load board termination for HCSL Outputs

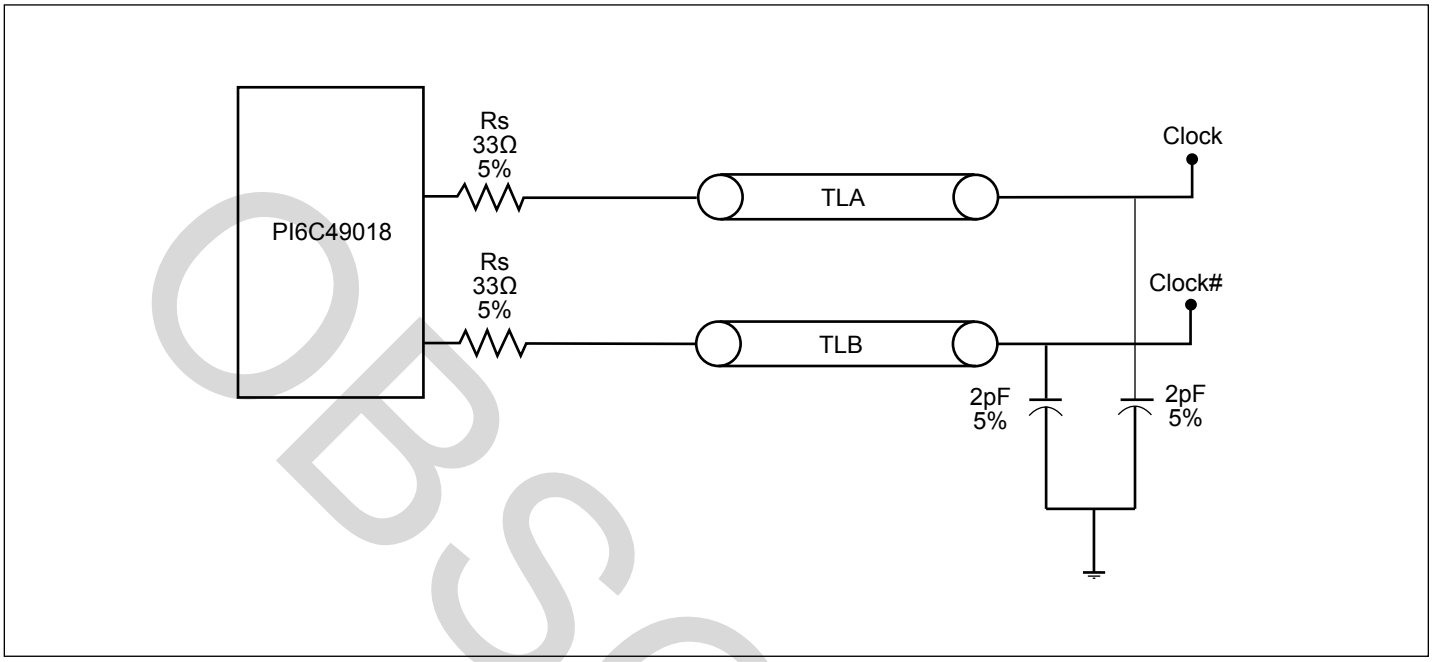
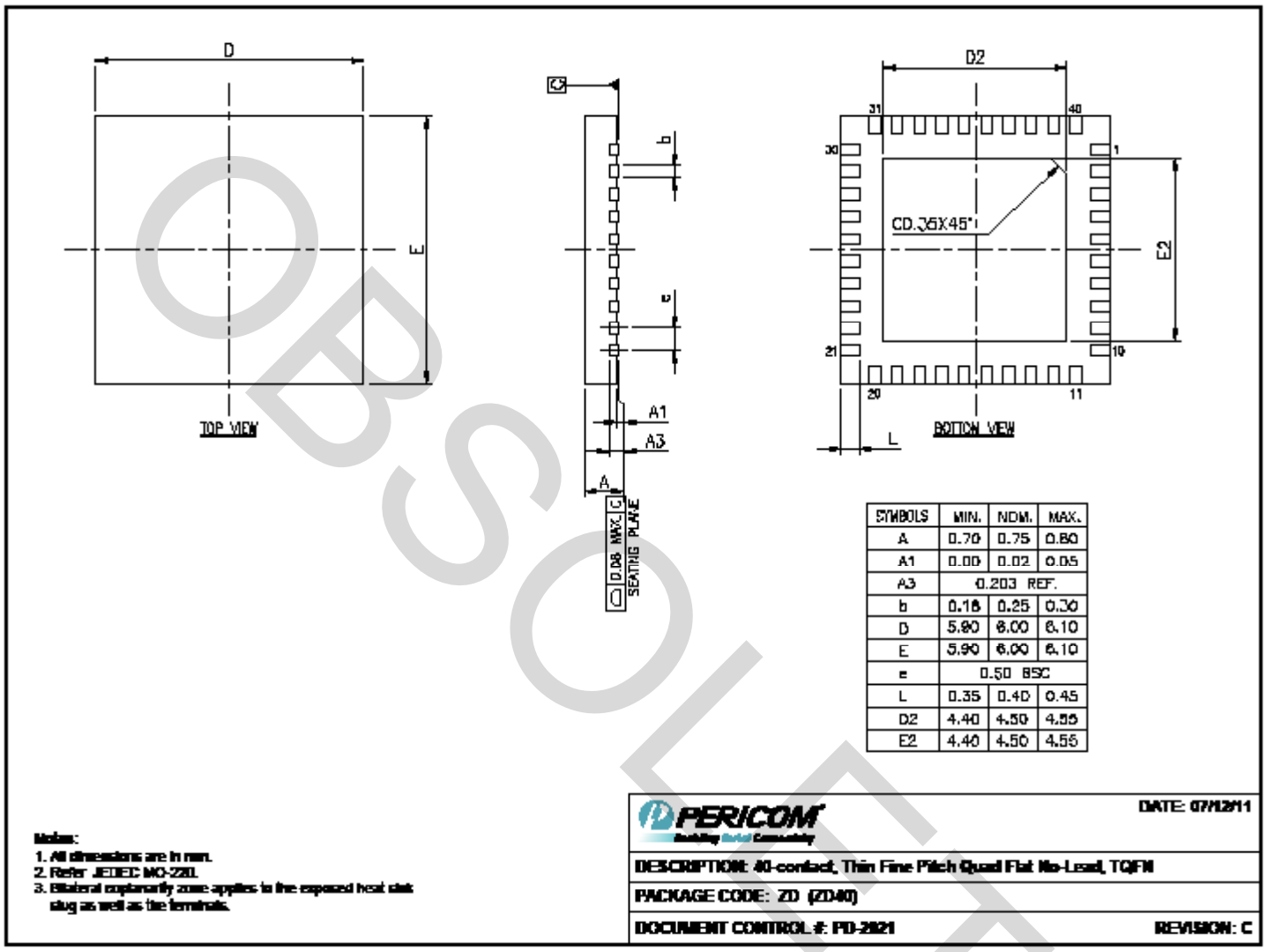


Figure 4. Configuration Test Load Board Termination

Packaging Mechanical: 40- TQFN (ZD)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.18	0.25	0.30
D	5.90	6.00	6.10
E	5.90	6.00	6.10
e		0.50 BSC	
L	0.35	0.40	0.45
D2	4.40	4.50	4.55
E2	4.40	4.50	4.55

Notes:
1. All dimensions are in mm.
2. Refer JEDEC MO-220.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

PERICOM Semiconductor Corporation
DATE: 07/12/11
DESCRIPTION: 40-contact, Thin Fine Pitch Quad Flat No-Lead, TQFN
PACKAGE CODE: ZD (ZD40)
DOCUMENT CONTROL #: PD-2021
REVISION: C

Note:
- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information(1-3)

Ordering Code	Package Code	Package Description
PI6C49018ZDIE	ZD	40-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel

单击下面可查看定价，库存，交付和生命周期等信息

>>Diodes Incorporated(达迩科技（美台）)