Crystal to LVDS/LVCMOS Frequency Synthesizer

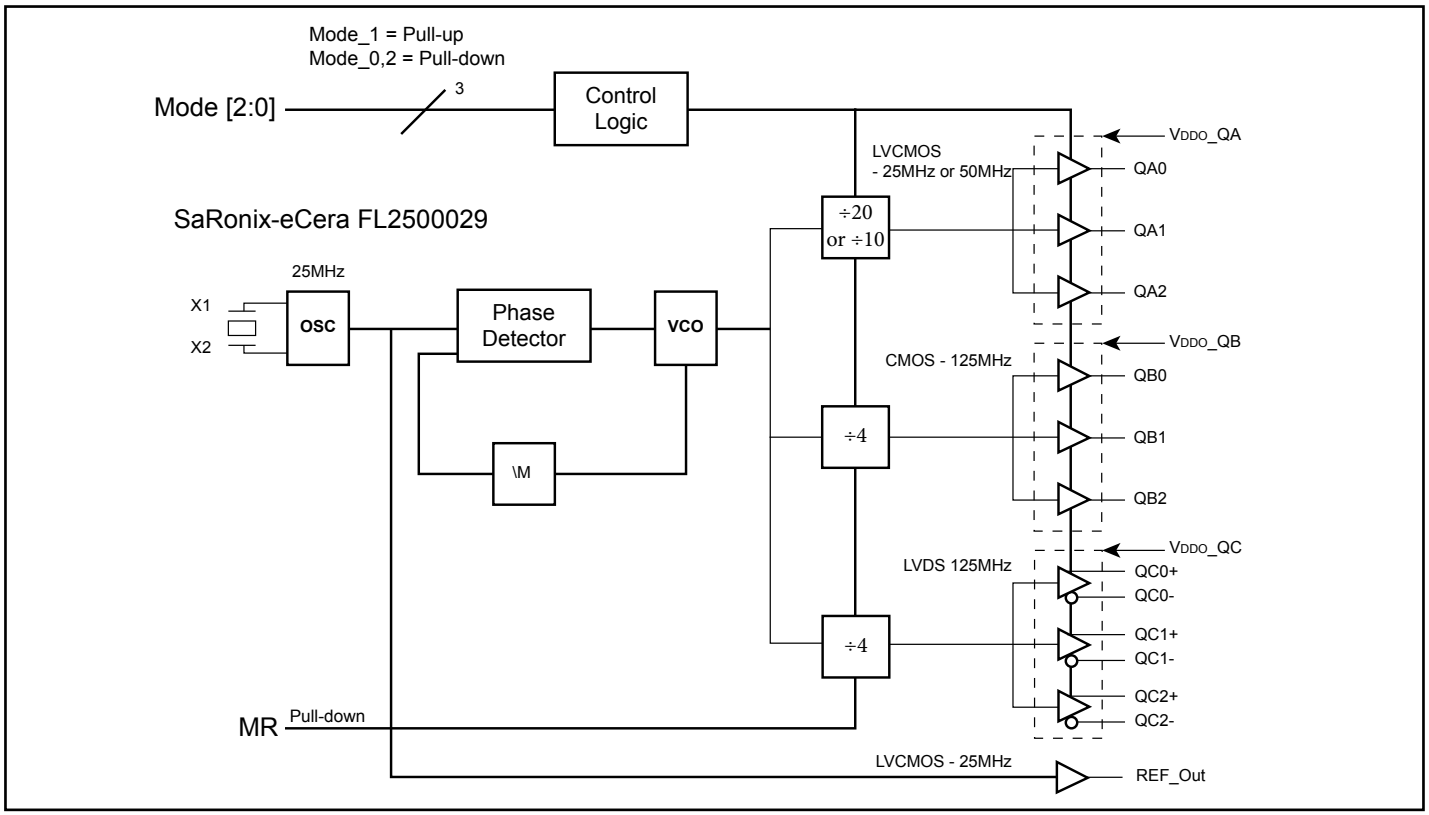
Features

- 3.3V supply voltage ± 5%
- Three banks of outputs:
  - Bank A: 3 25/50MHz pin selectable LVCMOS outputs
  - Bank B: 3 125MHz LVCMOS outputs
  - Bank C: 3 125MHz LVDS outputs
- 1 25MHz LVCMOS reference clock output (no PLL)
- 25MHz crystal input (SaRonix-eCera P/N FL2500029)
- Low 1ps max 12k-20MHz integrated phase noise design (for 125MHz CMOS and LVDS outputs)
- Industrial temperature -40°C to 85°C
- Package (Pb-free & Green)
  - 32-contact 5x5mm TQFN (ZH)

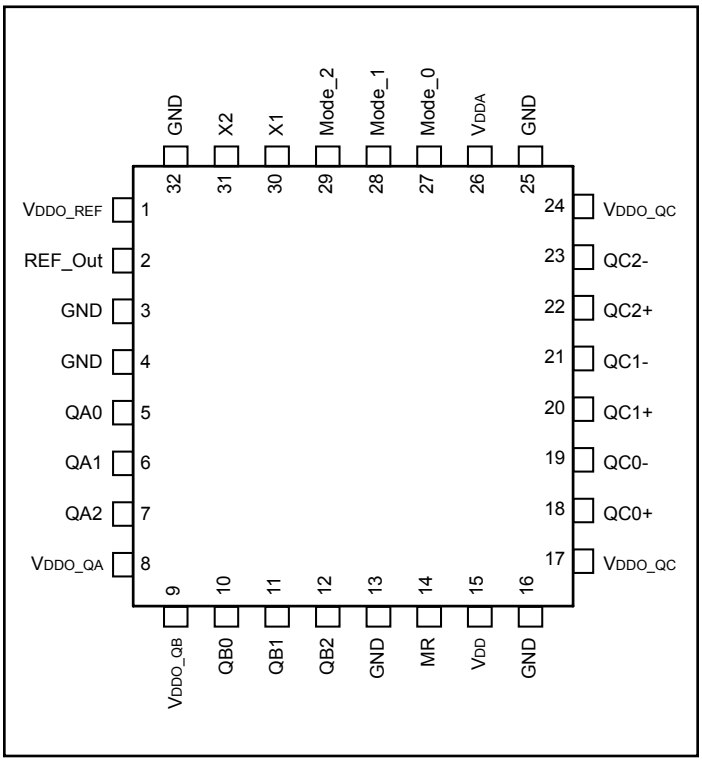
Description

The PI6LC4840 is an LC VCO based low phase noise design intended for the most demanding Ethernet applications. Common Ethernet frequencies of 25MHz and 125MHz are supported, with the 125Mhz having both LVDS and LVCMOS outputs for maximum flexibility. One 25Mhz LVCMOS non-PLL output is also available.

Block Diagram



Pin Configuration (32-contact TQFN)



Pinout Table

Pin Number	Pin Name	I/O Type	Description
1	V_{DDO_REF}	Power	Reference Clock Output Buffer V_{DD}
2	REF_Out	Output	25MHz LVCMOS output from fundamental oscillator core
3	GND	Power	Ground
4	GND	Power	Ground
5	QA0	Output	25 or 50MHz selectable LVCMOS output (see table 1)
6	QA1	Output	25 or 50MHz selectable LVCMOS output (see table 1)
7	QA2	Output	25 or 50MHz selectable LVCMOS output (see table 1)
8	V_{DDO_QA}	Power	V_{DD} Buffer Power for Bank A
9	V_{DDO_QB}	Power	V_{DD} Buffer Power for Bank B
10	QB0	Output	125MHz LVCMOS output
11	QB1	Output	125MHz LVCMOS output
12	QB2	Output	125MHz LVCMOS output
13	GND	Power	Ground

(Continued)

Pin Number	Pin Name	I/O Type	Description
14	MR	Input	Master Reset Pin. During Reset, LVCMOS outputs are pulled low, QCx+ outputs are pulled low, QCx- outputs are pulled high.
15	V_{DD}	Power	V_{DD} for core
16	GND	Power	Ground
17	V_{DDO_QC}	Power	V_{DD} Buffer Power for Bank C
18	QC0+	Output	125MHz LVDS Output
19	QC0-	Output	125MHz LVDS Output
20	QC1+	Output	125MHz LVDS Output
21	QC1-	Output	125MHz LVDS Output
22	QC2+	Output	125MHz LVDS Output
23	QC2-	Output	125MHz LVDS Output
24	V_{DDO_QC}	Power	V_{DD} Buffer Power for Bank C
25	GND	Power	GND
26	V_{DDA}	Power	V_{DD} for analog core
27	Mode_0	Input	Combination of output enable and frequency select functionality, see Table 1. Internal pull-down.
28	Mode_1	Input	Combination of output enable and frequency select functionality, see Table 1. Internal pull-up.
29	Mode_2	Input	Combination of output enable and frequency select functionality, see Table 1. Internal pull-down.
30	X1	Input	Crystal Input
31	X2	Output	Crystal Output
32	GND	Power	GND

Function Table (Mode Pin)

Inputs			Output Frequency (MHz)								
			Bank A			Bank B			Bank C		
Mode_2	Mode_1	Mode_0	QA0	QA1	QA2	QB0	QB1	QB2	QC0	QC1	QC2
0	0	0	25	-	-	-	-	-	125	-	-
0	0	1	25	-	-	125	-	-	125	-	-
0*	1*	0*	25	25	-	-	-	-	125	125	-
0	1	1	25	25	25	125	125	125	125	125	125
1	0	0	50	-	-	-	-	-	125	-	-
1	0	1	25	25	-	125	125	-	125	125	-
1	1	0	50	50	-	-	-	-	125	125	-
1	1	1	-	-	-	-	-	-	-	-	-

Notes:

- Outputs left in high impedance mode

* Default state

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature..... -65°C to +155°C
3.3V Analog Supply Voltage..... -0.5 to +4.6V
ESD Protection (HBM)..... 2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions (V_{DD} = V_{DDO_QA} = V_{DDO_QB} = V_{DDO_QC} = V_{DDO_REF} = 3.3V ±5%, T_A = -40°C to 85°C)

Symbol	Parameters	Conditions	Min.	Max.	Units
V_{DD}	3.3V Core Supply Voltage		3.135	3.465	V
V_{DDA}	3.3V for Analog		V_{DD} - 0.5	V_{DD}	
V_{DDO_REF}, V_{DDO_QA}, V_{DDO_QC}, V_{DDO_QB}	Output Supply Voltage		3.135	3.465	
T_A	Ambient Temperature		–40	85	°C
$I_{DD\ TOTAL}$	Sum of all I_{DD} currents flowing into IC	Outputs are unloaded		100	mA
I_{DD}	Power Supply Current for V_{DD} pin 15			15	
I_{DDA}	Analog Supply Current			50	
I_{DDO_QA}	Bank A LVCMOS Output Supply Current			5	
I_{DDO_QB}	Bank B LVCMOS Output Supply Current			10	
I_{DDO_QC}	LVDS Output Supply Current			25	
I_{DDO_REF}	Reference Supply Current			1	
P_{DISS}	Power Dissipation			0.35	W

LVCMOS DC Electrical Characteristics ($V_{DD} = V_{DDO\_QA} = V_{DDO\_QB} = V_{DDO\_QC} = V_{DDO\_REF}$ = 3.3V ±5%, T_A = -40°C to 85°C)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	
V_{OH}	Output High Voltage	I_{OH} = -12mA	2.6			
V_{OL}	Output Low Voltage	I_{OL} = 12mA			0.5	
I_{IH}	Input High Current	Mode_1, $V_{IN} = V_{DD}$ = 3.465V(1)			10	µA
		MR, Mode_2, Mode_0, $V_{IN} = V_{DD}$ = 3.465V			150	
I_{IL}	Input Low Current	MR, Mode_2, Mode_0, V_{DD} = 3.465V	-5			
		Mode_1, V_{DD} = 3.465V(1)	-150			µA
I_{OZ}	Tri-State output current				10	µA
R_{pu}	Internal pull up resistance			55		kΩ
R_{dn}	Internal pull down resistance			55		kΩ
Z_O	Output Impedance			38		Ω
C_{IN}	Input Capacitance	X1		5.5		pF
C_{OUT}	Output Capacitance	X2		1.5		

1. With condition in Fig 2.

LVCMOS AC Characteristics ($V_{DD} = V_{DDO\_QA} = V_{DDO\_QB} = V_{DDO\_QC} = V_{DDO\_REF}$ = 3.3V ±5%, T_A = -40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_r/T_f	Output Rise/Fall time	20% to 80%, C_L = 15pF			2	ns
		50Ω load			1.15	
T_{DC}	Output Duty Cycle	$t_{DC} = t_H/t_{CY}$, t_H = High Pulse Width, t_{CY} = Output Cycle Time, @ $V_{DD}/2$	48		52	%
J_{phase}	Integrated Phase Jitter	12kHz - 20MHz @125MHz		0.35	1	ps
		12kHz - 1MHz @25MHz		0.30	1	ps
		637kHz - 62.5MHz @125MHz		0.50	1	ps
$t_{SK(0)}$	Output-output skew	Within a bank at the same supply and with equal load			45	ps
t_j	Output period jitter	Output Freq = 25MHz AND 50MHz			30	ps
		Output Freq = 125MHz			70	

LVDS Output Characteristics (V_{DD} = V_{DDO_QA} = V_{DDO_QB} = V_{DDO_QC} = V_{DDO_REF} = 3.3V ±5%, T_A = -40°C to 85°C)

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
T_{rise} / T_{fall}	Rise and Fall Time	20% to 80%, single-ended	145		360	ps
T_{DC}	Duty Cycle	Differential	48		52	%
J_{phase}	Integrated phase jitter	12KHz-20MHz @ 125MHz		0.45	1	ps
		637kHz - 62.5MHz @125MHz(2)		0.45	1	
$T_{sk(o)}$	Output to Output skew	Within a bank at the same supply and with equal load			35	ps
I_{OZ}	Tri-state Output Current				10	µA
T_{DIS}	Output Disable Time				50	ns
T_{EN}	Output Enable Time				50	
V_{OD}	Differential Output Voltage		300		575	mV
V_{OS}	Offset Voltage		1.325		1.575	V
PSRR	Power Supply Rejection Ratio	Modulation Power = -30dBm from 10k to 15M modulation freq.		-50		dBc

2. Does not include 25MHz reference spur.

25MHz Crystal Characteristics (V_{DD} = V_{DDO_QA} = V_{DDO_QB} = V_{DDO_QC} = V_{DDO_REF} = 3.3V ±5%, T_A = -40°C to 85°C)

Parameters	Description	Min	Typ	Max.	Units
FREQ	Frequency		25		MHz
ESR	Equivalent Series Resistance			50	Ω
Cload	Load Capacitance		18		pF
Cshunt	Shunt Capacitance			7	
DRIVE	Drive Level			0.65	mW

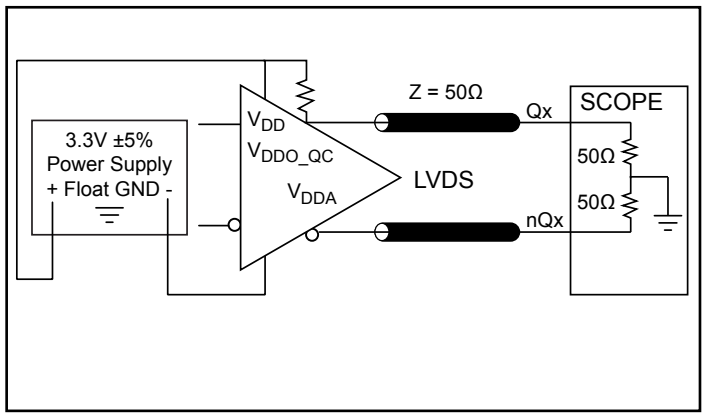


Figure 1. LVDS Output Load AC Test Circuit

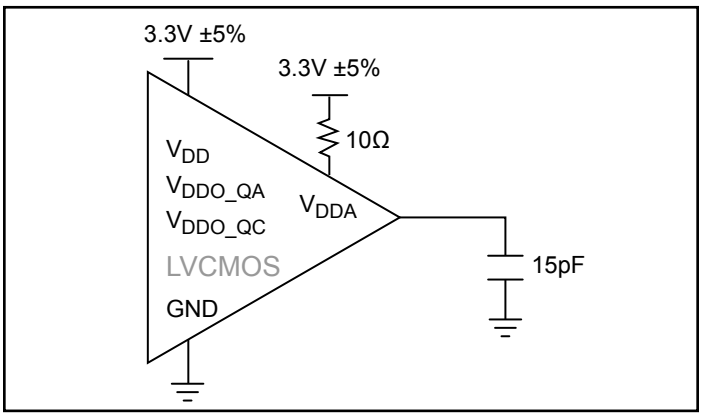


Figure 2. LVCMOS Output Load AC Test Circuit

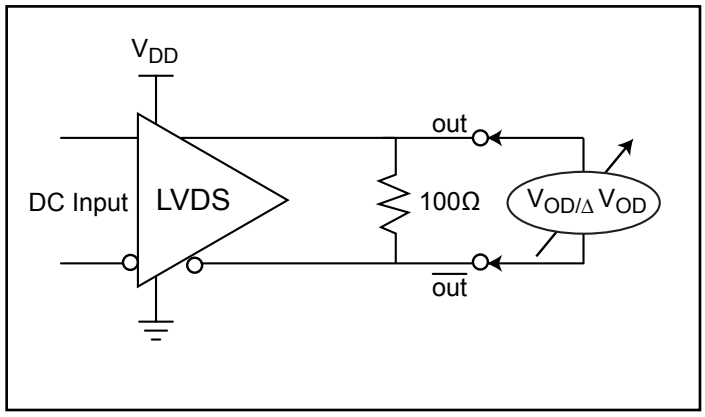


Figure 3. Differential Output Voltage Setup (V_{OD})

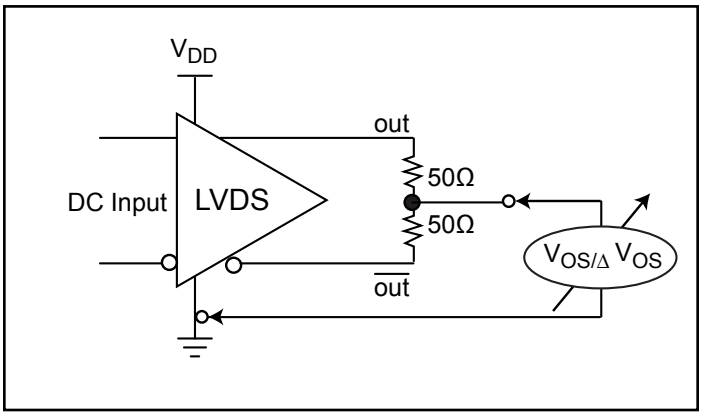


Figure 4. OffsetVoltage Setup (V_{OS})

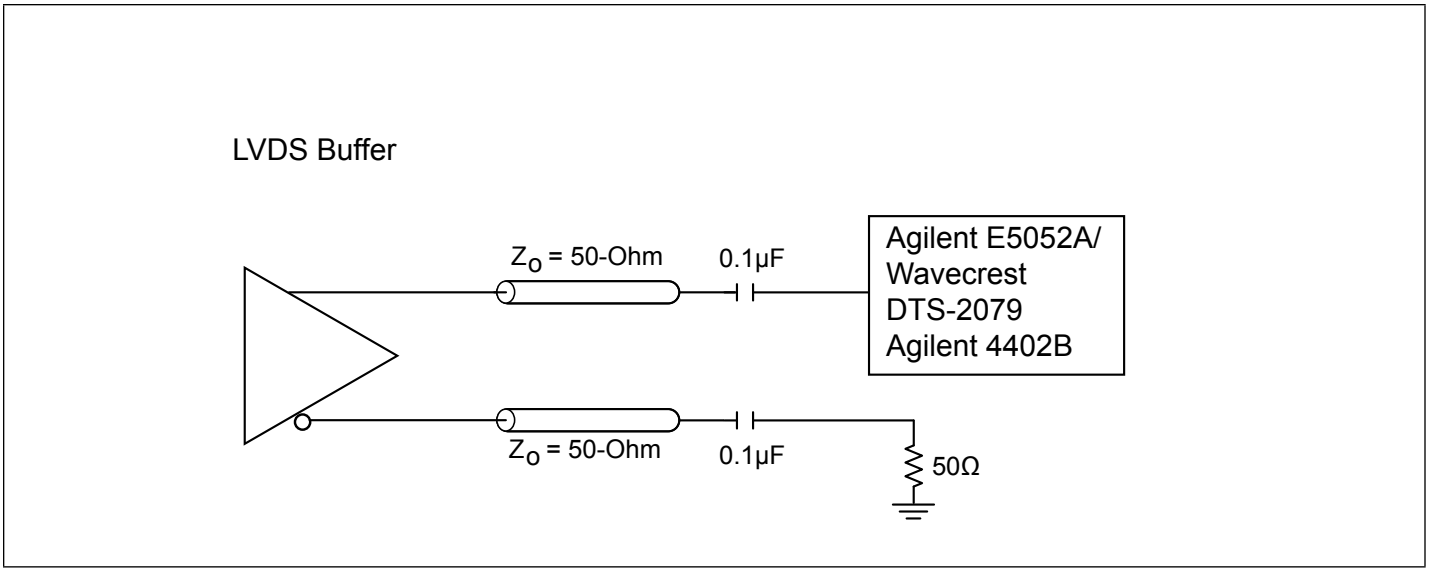


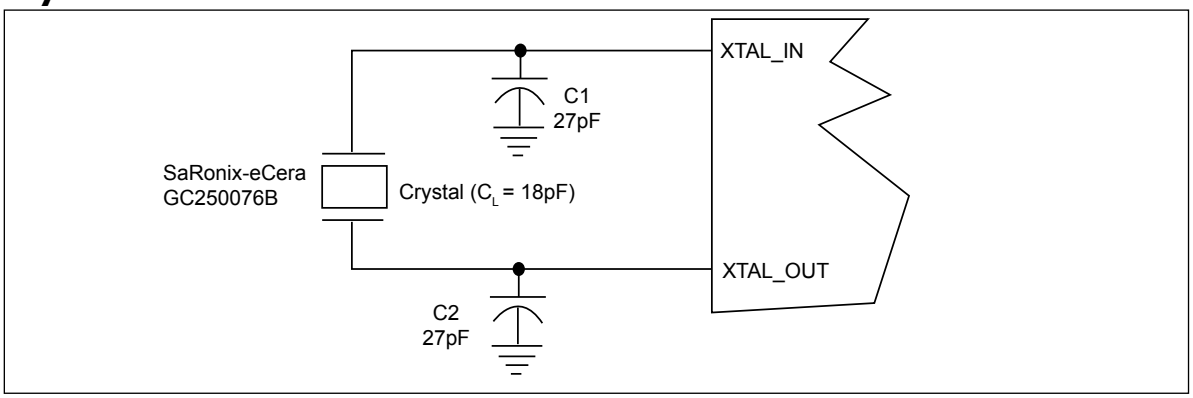
Figure 5. LVDS Test Circuit for Phase Noise, Period Jitter, and PSRR

Application Notes

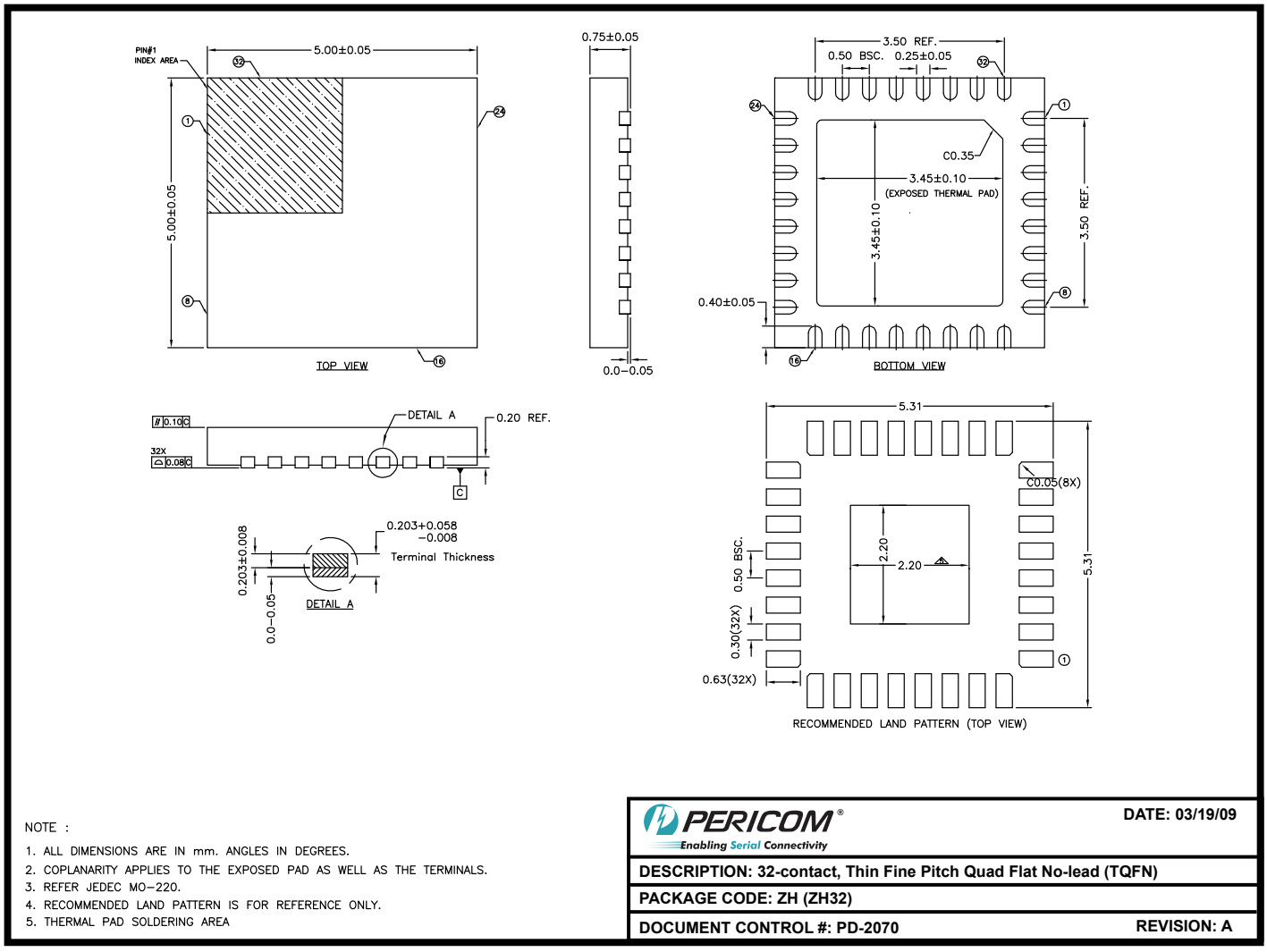
Crystal circuit connection

The following diagram shows PI6LC4840 crystal circuit connection with a parallel crystal. For the C_L=18pF crystal, it is suggested to use C1=27pF, C2=27pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

Crystal Oscillator Circuit



Packaging Mechanical: 32-Contact TQFN (ZH)



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For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Type
PI6LC4840ZHE	ZH	Pb-free & Green, (TQFN)

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel

单击下面可查看定价，库存，交付和生命周期等信息

>>Diodes Incorporated(达迩科技（美台）)