AP62600

4.5V TO 18V INPUT, 6A SYNCHRONOUS BUCK CONVERTER

Description

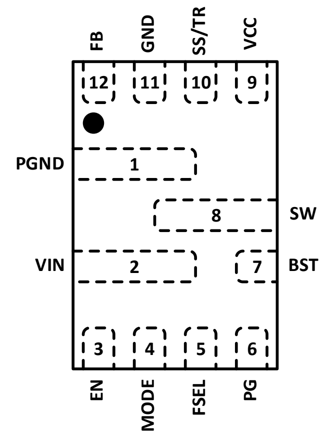
The AP62600 is a 6A, synchronous buck converter with a wide input voltage range of 4.5V to 18V. The device fully integrates a 36mΩ high-side power MOSFET and a 14mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

The AP62600 device is easily used by minimizing the external component count due to its adoption of Constant On-Time (COT) control to achieve fast transient response, easy loop stabilization, and low output voltage ripple.

The AP62600 design is optimized for Electromagnetic Interference (EMI) reduction. The device has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching.

The device is available in a V-QFN2030-12 (Type A) package.

Pin Assignments



V-QFN2030-12
(Type A)

Features

- VIN: 4.5V to 18V
- Output Voltage (VOUT): 0.6V to 7V
- 6A Continuous Output Current
- 0.6V ± 1% Reference Voltage
- 360μA Quiescent Current
- Selectable Switching Frequency
  - 400kHz
  - 800kHz
  - 1.2MHz
- Selectable Operation Modes
  - Pulse Frequency Modulation (PFM)
  - Ultrasonic Mode (USM)
  - Pulse Width Modulation (PWM)
- Programmable Soft-Start Time
- Proprietary Gate Driver Design for Best EMI Reduction
- Power-Good Indicator
- Precision Enable Threshold to Adjust UVLO
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Cycle-by-Cycle Valley Current Limit
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Applications

- 5V and 12V Distributed Power Bus Supplies
- Television Sets and Monitors
- White Goods and Small Home Appliances
- FPGA, DSP, and ASIC Supplies
- Home Audio
- Network Systems
- Gaming Consoles
- Consumer Electronics
- General Purpose Point of Load

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Application Circuit

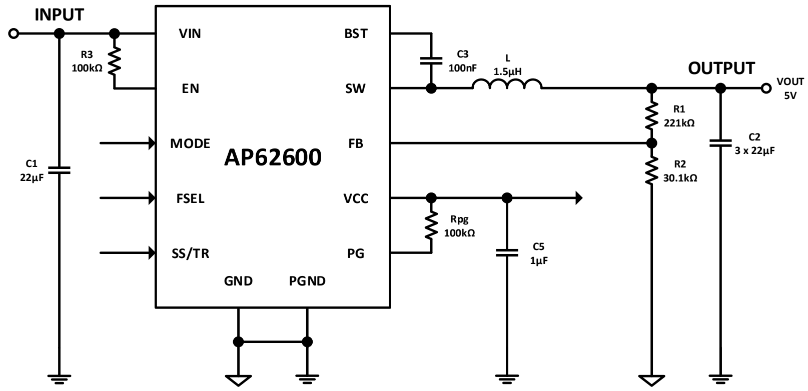


Figure 1. Typical Application Circuit

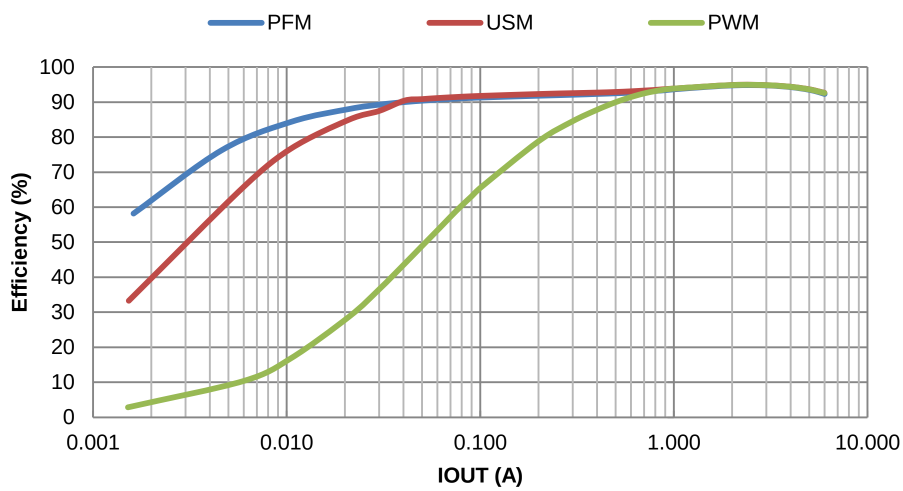


Figure 2. Efficiency vs. Output Current, VIN = 12V, VOUT = 5V, L = 1.5µH, f_{SW} = 800kHz

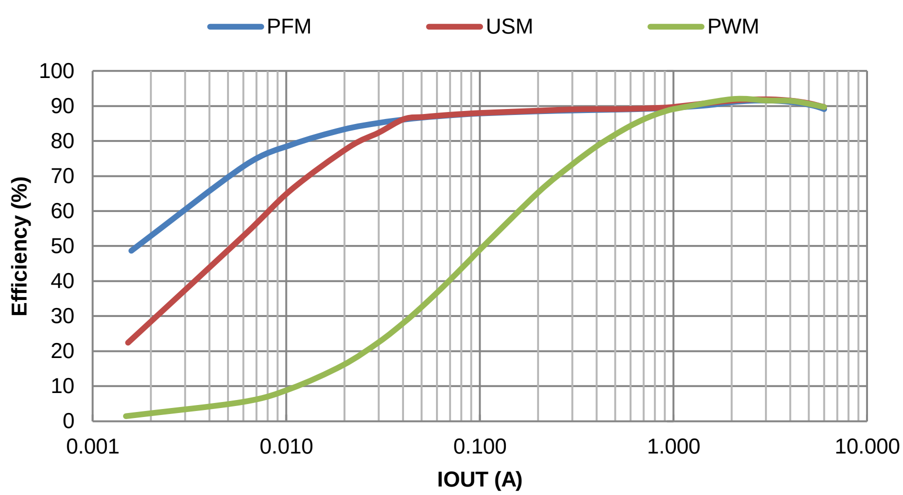


Figure 3. Efficiency vs. Output Current, VIN = 12V, VOUT = 3.3V, L = 1.2µH, f_{SW} = 800kHz

Pin Descriptions

Pin Name	Pin Number	Function
PGND	1	Power Ground. PGND must be connected to a single point ground and to as large a PGND plane as possible on the PCB for proper operation and optimized thermal performance.
VIN	2	Power Input. VIN supplies the power to the IC as well as the step-down converter power MOSFETs. Drive VIN with a 4.5V to 18V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. See **Input Capacitor** section for more details.
EN	3	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. It can be left open for automatic startup. The EN has a precision threshold of 1.18V for programing the UVLO. See **Enable** section for more details.
MODE	4	MODE Select. MODE is used to select the operation mode of the device. Connect MODE to GND to program the device to operate in PFM Mode. Leave MODE floating to program the device to operate in USM. Connect MODE to VCC to program the device to operate in PWM Only Mode.
FSEL	5	Frequency Select. FSEL is used to select the switching frequency of the device. Connect FSEL to GND to program the switching frequency to 400kHz. Leave FSEL floating to program the switching frequency to 800kHz. Connect FSEL to VCC to program the switching frequency to 1.2MHz.
PG	6	Power-Good. PG is an open-drain output that is pulled to GND when the output voltage is out of its regulation limits or during soft-start. Connect an external pull-up resistor from PG to VCC.
BST	7	High-Side Gate Drive Boost Input. BST supplies the drive voltage for the high-side N-Channel power MOSFET. A 100nF capacitor is recommended from BST to SW to power the high-side driver.
SW	8	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
VCC	9	Internal Power Supply. VCC supplies the internal logic circuitry as well as the gate drivers. Connect a 1µF capacitor as close as possible to VCC and PGND. This pin is not active when EN is low.
SS/TR	10	Soft-start and Tracking. SS/TR controls the soft-start, tracking, and sequencing of the output. Connect a ceramic capacitor from SS/TR to GND to program the soft-start time. Leave SS/TR floating to use the internal soft-start. See **Soft-Start, Tracking, and Sequencing** section for more details.
GND	11	Ground. GND is the main power ground for the control logic circuitry. It must have a Kelvin Connection to PGND.
FB	12	Feedback. FB is the sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See **Setting the Output Voltage** section for more details.

Functional Block Diagram

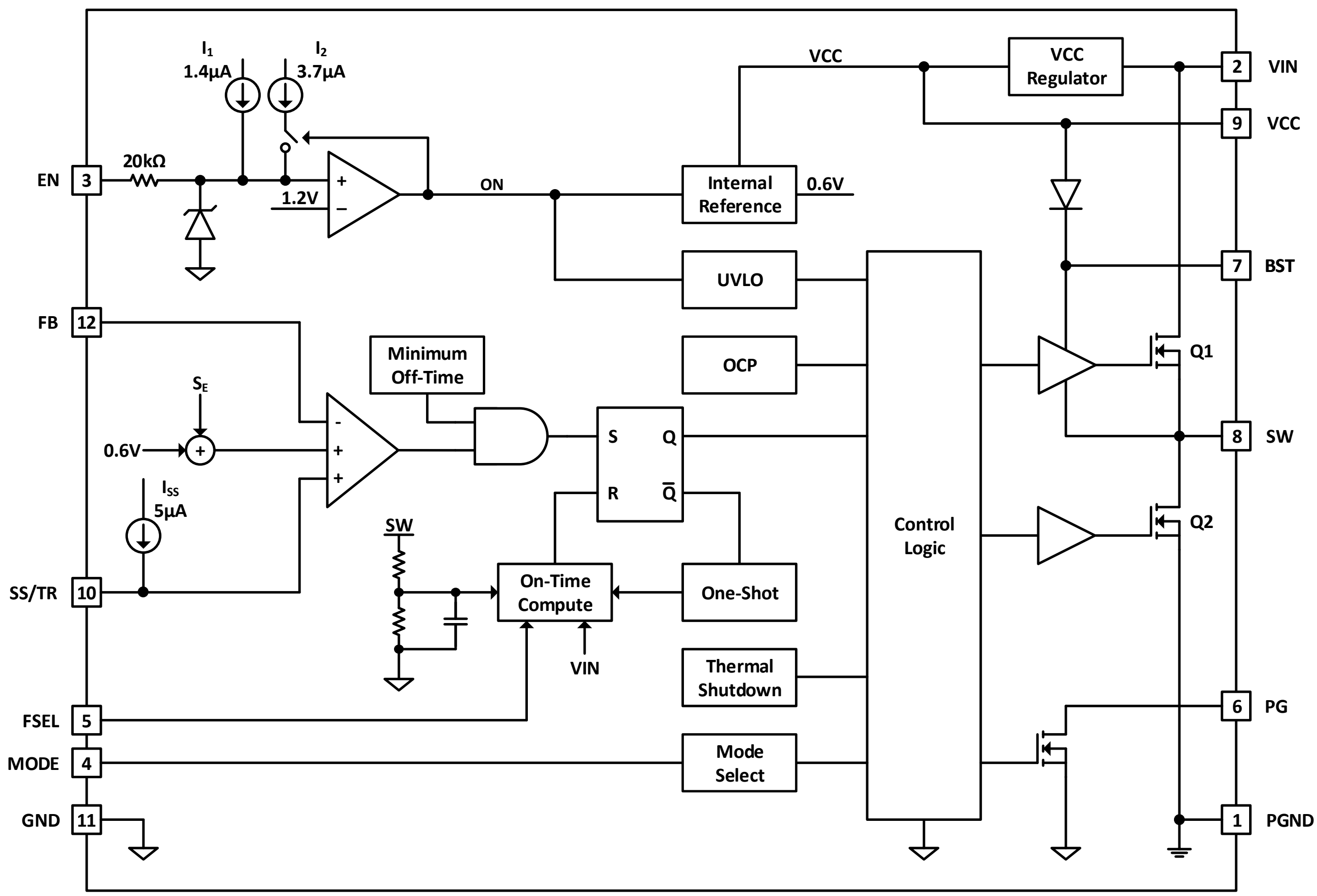


Figure 4. Functional Block Diagram

Absolute Maximum Ratings (Note 4) (At T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +20.0 (DC)	V
		-0.3 to 22.0 (400ms)	
VCC	VCC Pin Voltage	-0.3 to +6.0	V
V_{EN}	Enable/UVLO Pin Voltage	-0.3 to +6.0	V
V_{MODE}	MODE Select Pin Voltage	-0.3 to +6.0	V
V_{FSEL}	Frequency Select Pin Voltage	-0.3 to +6.0	V
V_{PG}	Power-Good Pin Voltage	-0.3 to +6.0	V
V_{BST}	Bootstrap Pin Voltage	V_{SW} - 0.3 to V_{SW} + 6.0	V
V_{SW}	Switch Pin Voltage	-1.0 to VIN + 0.3 (DC)	V
		-2.5 to VIN + 2.0 (20ns)	
$V_{SS/TR}$	Soft-Start/Tracking Pin Voltage	-0.3 to +6.0	V
V_{FB}	Feedback Pin Voltage	-0.3 to +6.0	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+150	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	±2000	V
CDM	Charged Device Model	±500	V

Notes: 4. Stresses greater than the **Absolute Maximum Ratings** specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	V-QFN2030-12 (Type A)	40	°C/W
θ_{JC}	Junction to Case	V-QFN2030-12 (Type A)	5.5	°C/W

Note: 6. Test condition for V-QFN2030-12: Device mounted on FR-4 substrate, four-layer PCB, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions (Note 7) (At T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	4.5	18.0	V
VOUT	Output Voltage	0.6	7.0	V
T_A	Operating Ambient Temperature	-40	+85	°C
T_J	Operating Junction Temperature	-40	+125	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (At T_J = +25°C, VIN = 12V, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +125°C, and input voltage range, 4.5V to 18V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V	—	1	3	µA
I_Q	Quiescent Supply Current	V_{FB} = 0.85V	—	360	—	µA
POR	VIN Power-on Reset Rising Threshold	—	4.0	4.25	4.45	V
UVLO	VIN Undervoltage Lockout Falling Threshold	—	—	3.95	—	V
VCC	VCC Output Voltage	6.0V < VIN < 18V, 0 < I_{VCC} < 5mA	4.75	5.0	5.25	V
I_{VCC}	VCC Current Source	VIN = 6V, VCC = 0V	—	—	20	mA
$R_{DS(ON)1}$	High-Side Power MOSFET On-Resistance (Note 8)	—	—	36	—	mΩ
$R_{DS(ON)2}$	Low-Side Power MOSFET On-Resistance (Note 8)	—	—	14	—	mΩ
I_{VALLEY_LIMIT}	LS Valley Current Limit (Note 8)	From source to drain	7.5	8.5	9.5	A
I_{NCL}	LS Negative Current Limit	From drain to source	—	2.0	—	A
f_{SW}	Oscillator Frequency	V_{FSEL} = GND, VOUT = 5V, CCM	—	400	—	kHz
		V_{FSEL} = Floating, VOUT = 5V, CCM	—	800	—	kHz
		V_{FSEL} = VCC, VOUT = 5V, CCM	—	1200	—	kHz
V_{MODE_PFM}	PFM Mode Logic Threshold	V_{MODE} = GND	—	—	0.9	V
V_{MODE_USM}	Ultrasonic Mode Logic Threshold	V_{MODE} = Floating	—	2.5	—	V
V_{MODE_PWM}	PWM Mode Logic Threshold	V_{MODE} = VCC	3.8	—	—	V
t_{ON_MIN}	Minimum On-Time	—	—	70	—	ns
t_{OFF_MIN}	Minimum Off-Time	—	—	255	—	ns
V_{FB}	Feedback Voltage	CCM	0.594	0.600	0.606	V
V_{EN_H}	EN Logic High Threshold	—	—	1.20	1.25	V
V_{EN_L}	EN Logic Low Threshold	—	1.03	1.12	—	V
I_{EN}	EN Input Current	V_{EN} = 1.5V	—	5.1	—	µA
		V_{EN} = 1V	1.0	1.4	2.0	µA
t_{SS}	Soft-Start Time	$V_{SS/TR}$ = Floating	—	1	—	ms
I_{SS}	Soft-Start Current Source	$V_{SS/TR}$ = 1.2V	—	5	—	µA
PG_{UV_FALL}	Undervoltage Falling Threshold	Percent of Output Regulation, Fault	—	85	—	%
PG_{UV_RISE}	Undervoltage Rising Threshold	Percent of Output Regulation, Good	—	95	—	%
PG_{OV_RISE}	Overvoltage Rising Threshold	Percent of Output Regulation, Fault	—	115	—	%
PG_{OV_FALL}	Overvoltage Falling Threshold	Percent of Output Regulation, Good	—	105	—	%
t_{PG_RD}	Power-Good Rise Delay Time	—	—	0.5	—	ms
V_{PG_OL}	Power-Good Output Logic Low	I_{PG} = -3mA	—	—	0.4	V
T_{SD}	Thermal Shutdown (Note 8)	—	—	160	—	°C
T_{HYS}	Thermal Shutdown Hysteresis (Note 8)	—	—	30	—	°C

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (AP62600 at T_A = +25°C, VIN = 12V, VOUT = 5V, FSEL = Floating (f_{SW} = 800kHz), SS/TR = Floating (t_{SS} = 1ms), unless otherwise specified.)

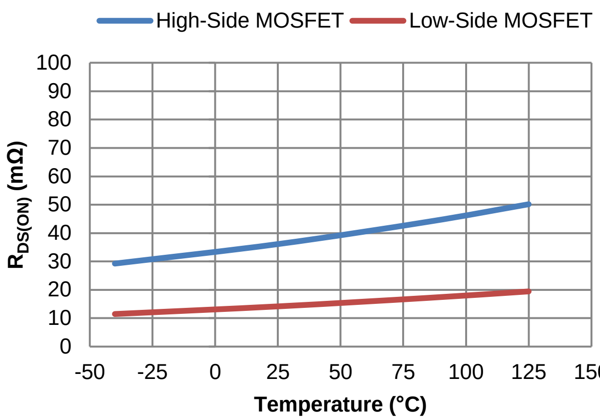


Figure 5. Power MOSFET $R_{DS(ON)}$ vs. Temperature

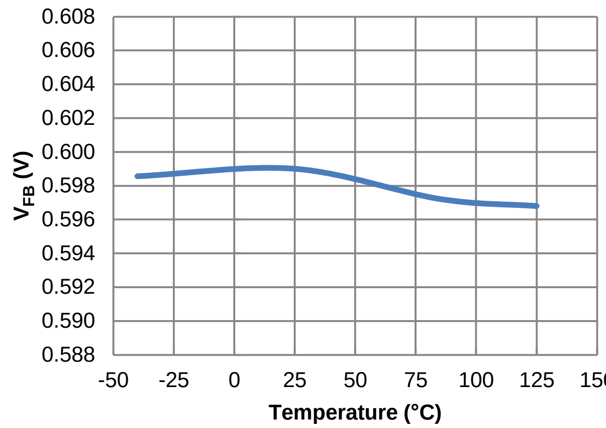


Figure 6. V_{FB} vs. Temperature

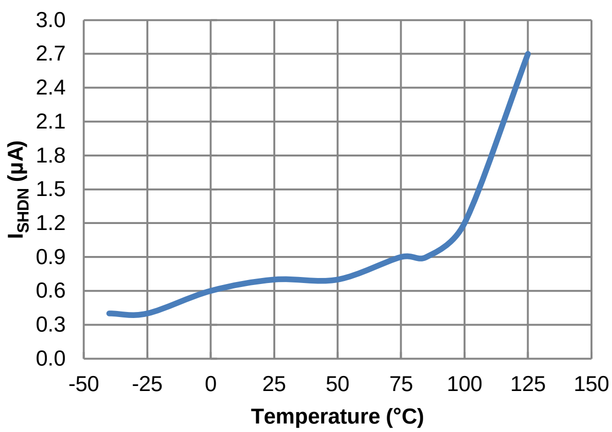


Figure 7. I_{SHDN} vs. Temperature

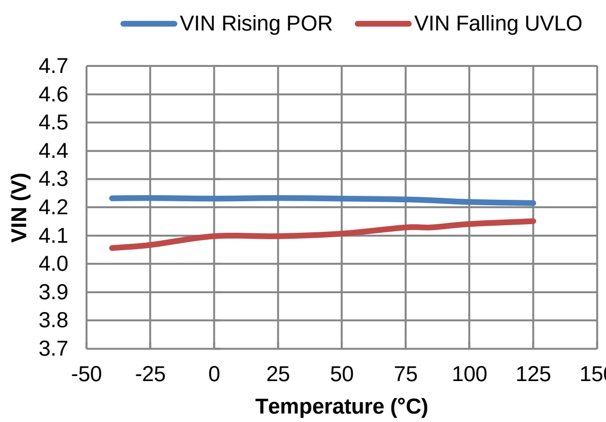


Figure 8. VIN Power-On Reset and UVLO vs. Temperature

Typical Performance Characteristics (AP62600 at T_A = +25°C, VIN = 12V, VOUT = 5V, FSEL = Floating (f_{SW} = 800kHz), SS/TR = Floating (t_{SS} = 1ms), unless otherwise specified.) (continued)

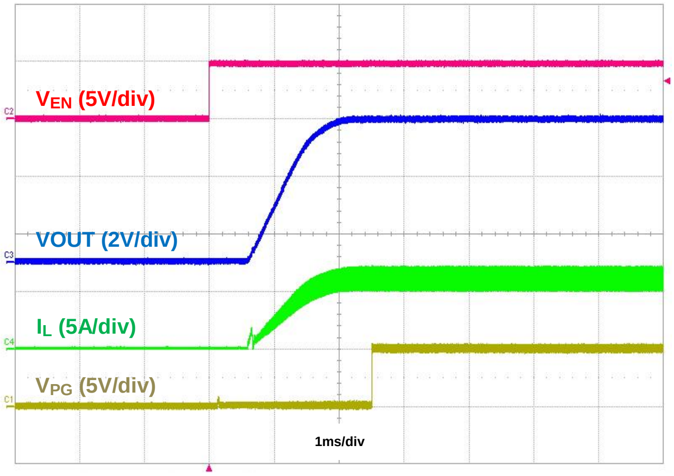


Figure 9. Startup Using EN, IOUT = 6A

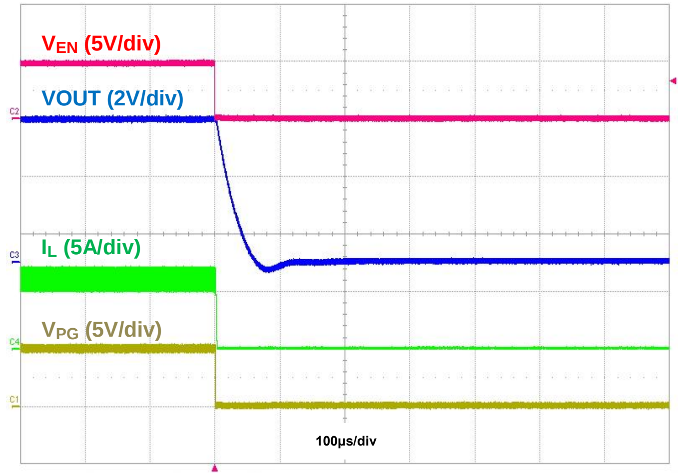


Figure 10. Shutdown Using EN, IOUT = 6A

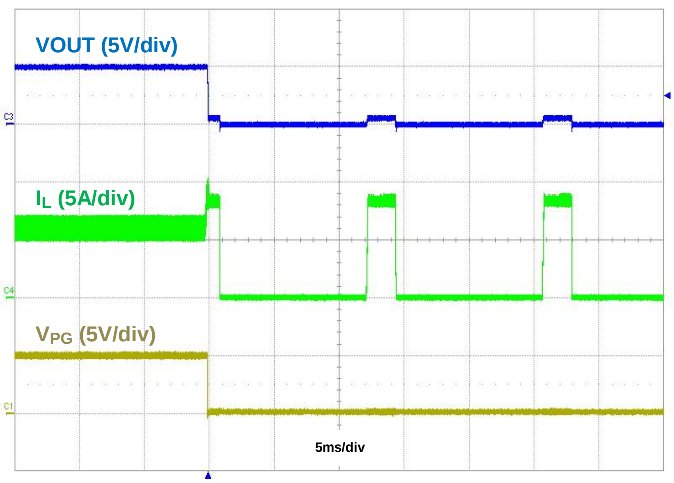


Figure 11. Output Short Protection, IOUT = 6A

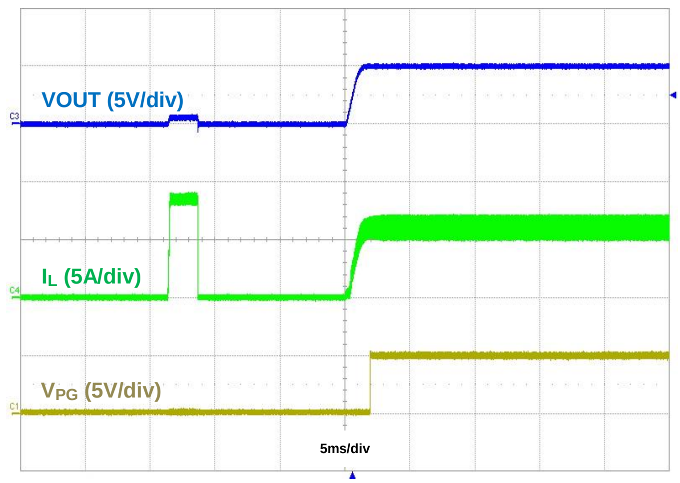


Figure 12. Output Short Recovery, IOUT = 6A

Typical Performance Characteristics (AP62600 at T_A = +25°C, VIN = 12V, VOUT = 5V, MODE = GND (PFM), FSEL = Floating (f_{SW} = 800kHz), SS/TR = Floating (t_{SS} = 1ms), unless otherwise specified.)

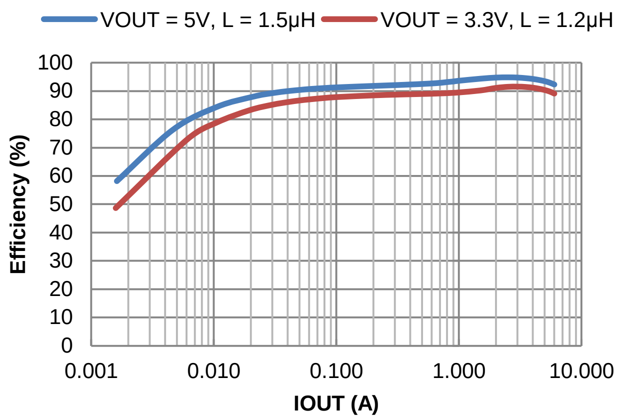


Figure 13. Efficiency vs. Output Current, VIN = 12V

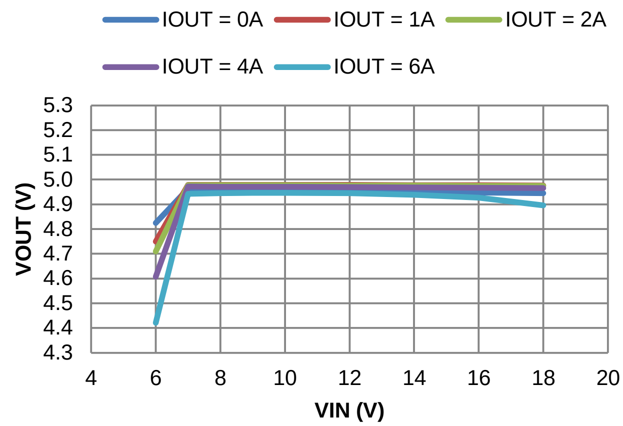


Figure 14. Line Regulation

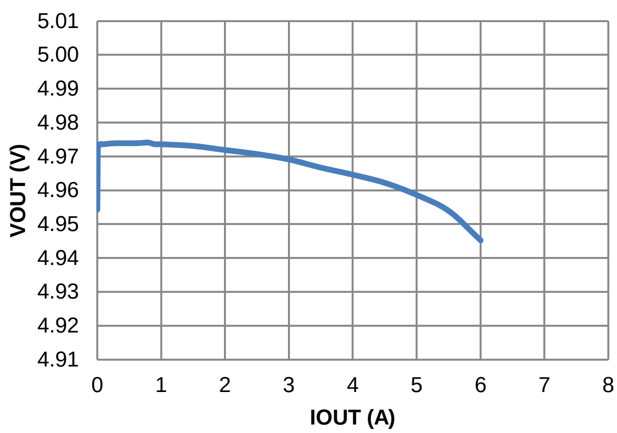


Figure 15. Load Regulation

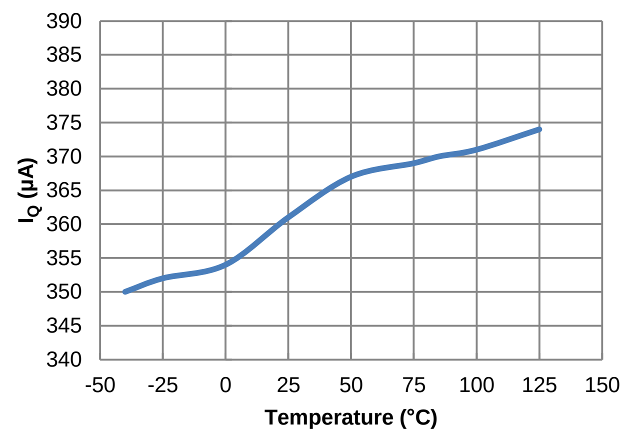


Figure 16. I_Q vs. Temperature

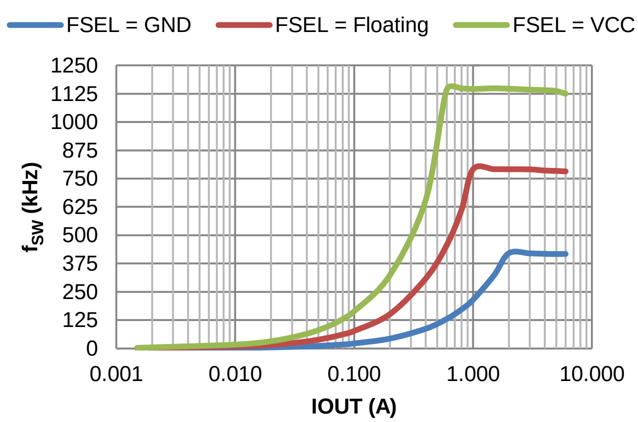


Figure 17. f_{SW} vs. Load

Typical Performance Characteristics (AP62600 at T_A = +25°C, VIN = 12V, VOUT = 5V, MODE = GND (PFM), FSEL = Floating (f_{SW} = 800kHz), SS/TR = Floating (t_{SS} = 1ms), unless otherwise specified.) (continued)

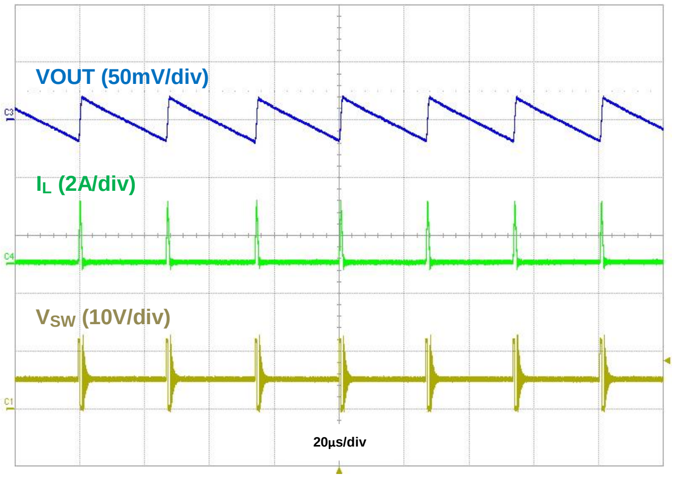


Figure 18. Output Voltage Ripple, IOUT = 50mA

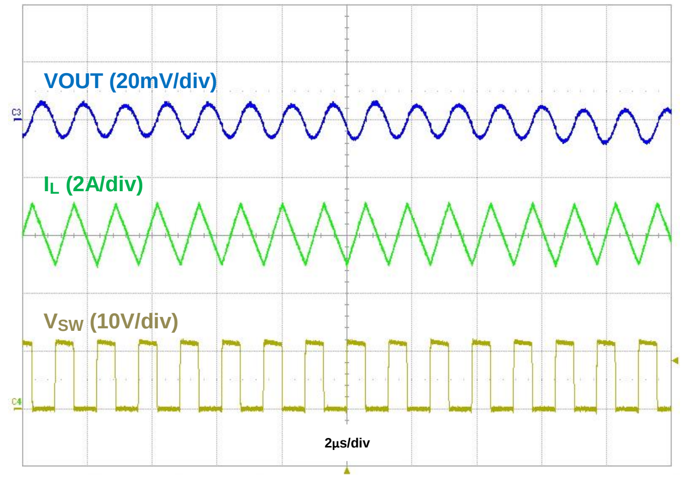


Figure 19. Output Voltage Ripple, IOUT = 6A

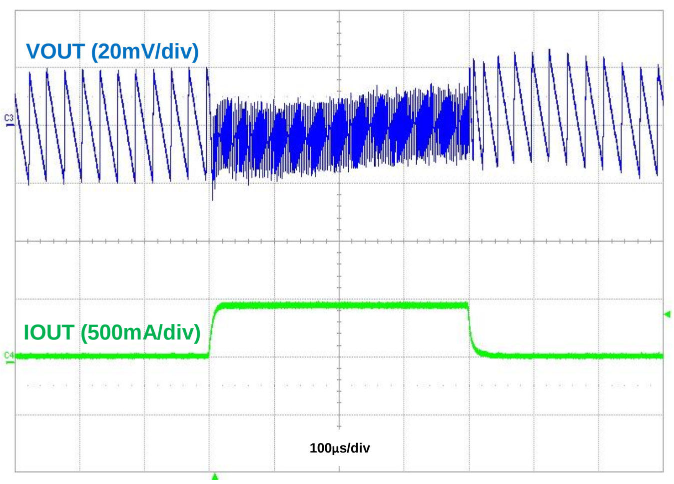


Figure 20. Load Transient, IOUT = 50mA to 500mA to 50mA

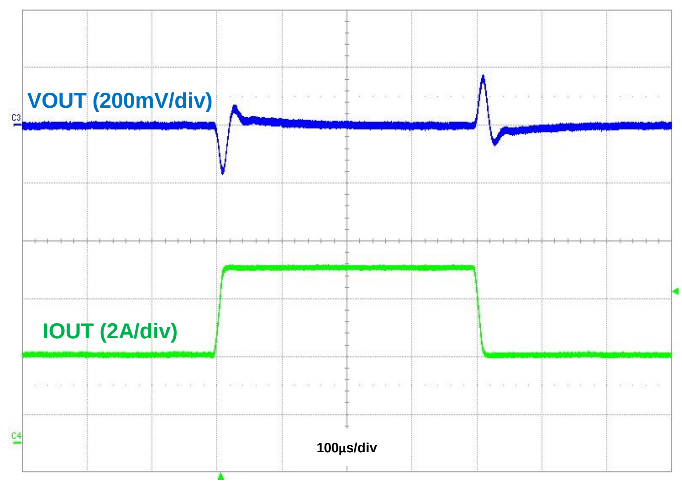


Figure 21. Load Transient, IOUT = 3A to 6A to 3A

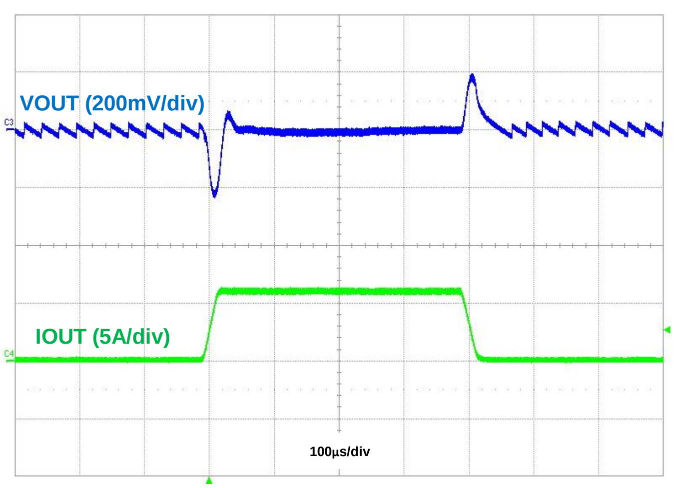


Figure 22. Load Transient, IOUT = 50mA to 6A to 50mA

Typical Performance Characteristics (AP62600 at T_A = +25°C, VIN = 12V, VOUT = 5V, MODE = Floating (USM), FSEL = Floating (f_{SW} = 800kHz), SS/TR = Floating (t_{SS} = 1ms), unless otherwise specified.)

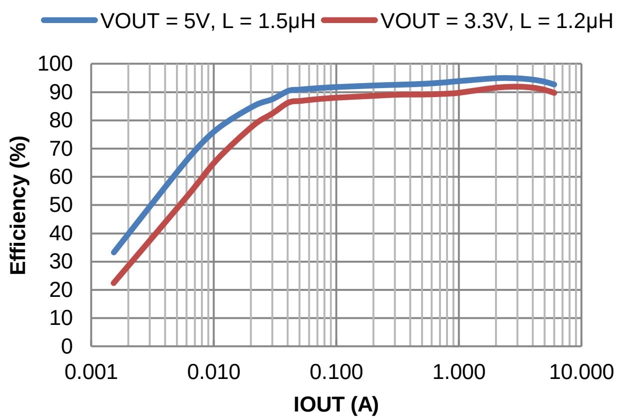


Figure 23. Efficiency vs. Output Current, VIN = 12V

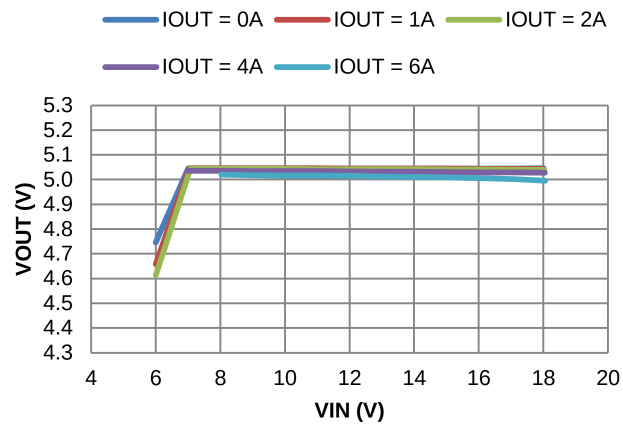


Figure 24. Line Regulation

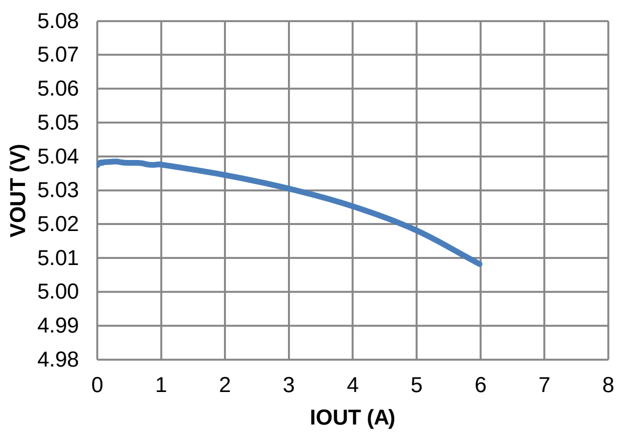


Figure 25. Load Regulation

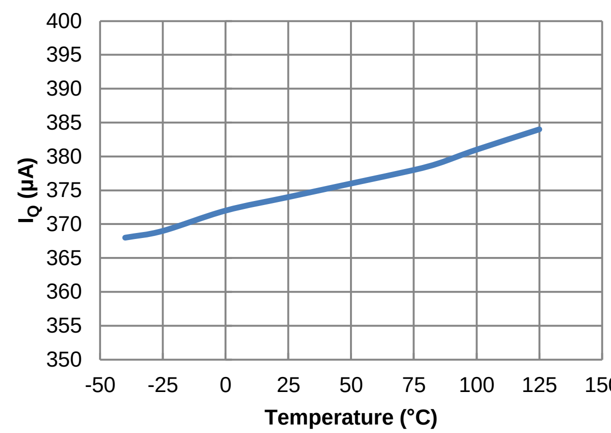


Figure 26. I_Q vs. Temperature

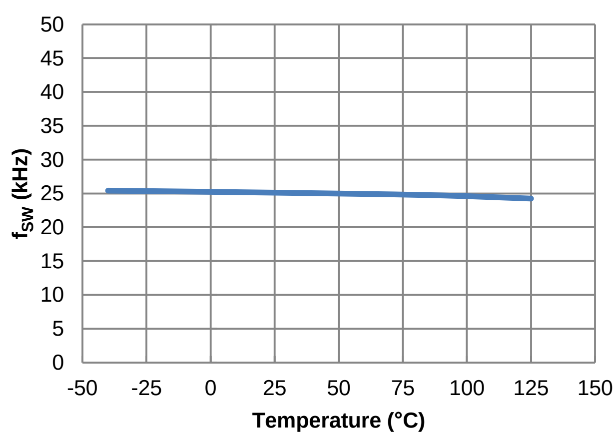


Figure 27. f_{SW} vs. Temperature, IOUT = 0A

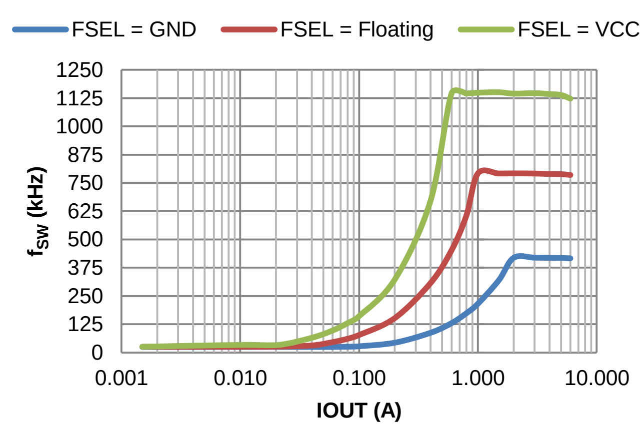


Figure 28. f_{SW} vs. Load

Typical Performance Characteristics (AP62600 at T_A = +25°C, VIN = 12V, VOUT = 5V, MODE = Floating (USM), FSEL = Floating (f_{SW} = 800kHz), SS/TR = Floating (t_{SS} = 1ms), unless otherwise specified.) (continued)

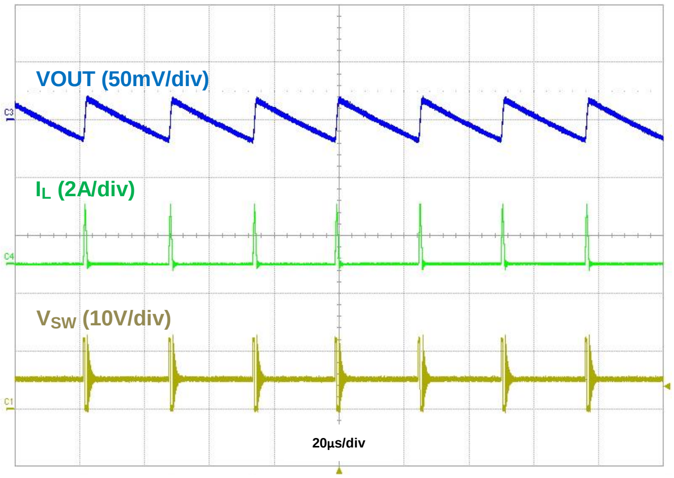


Figure 29. Output Voltage Ripple, IOUT = 50mA

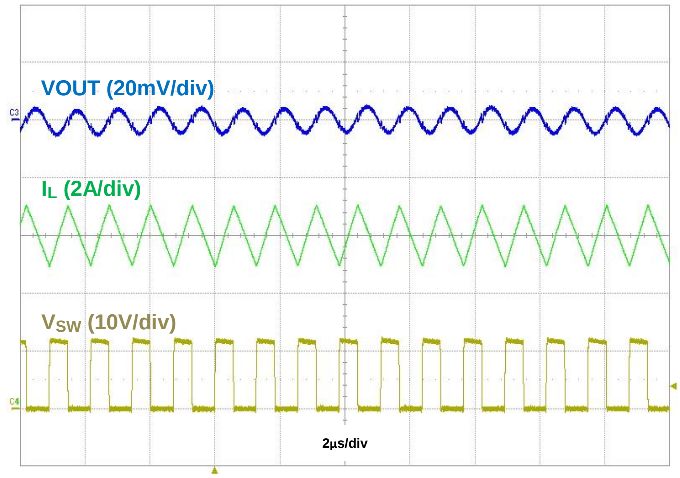


Figure 30. Output Voltage Ripple, IOUT = 6A

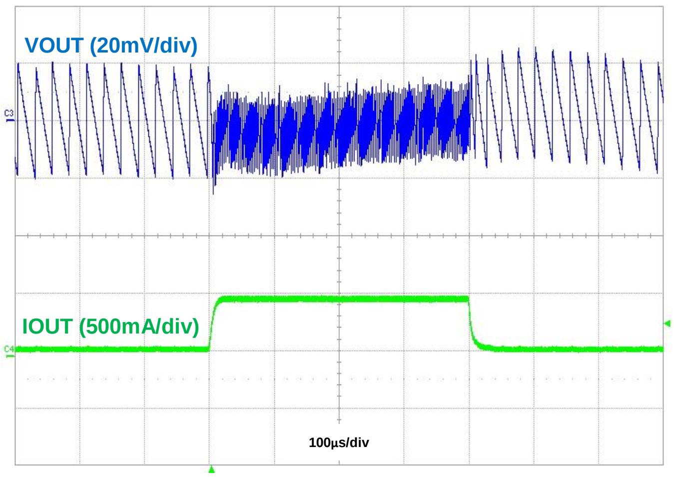


Figure 31. Load Transient, IOUT = 50mA to 500mA to 50mA

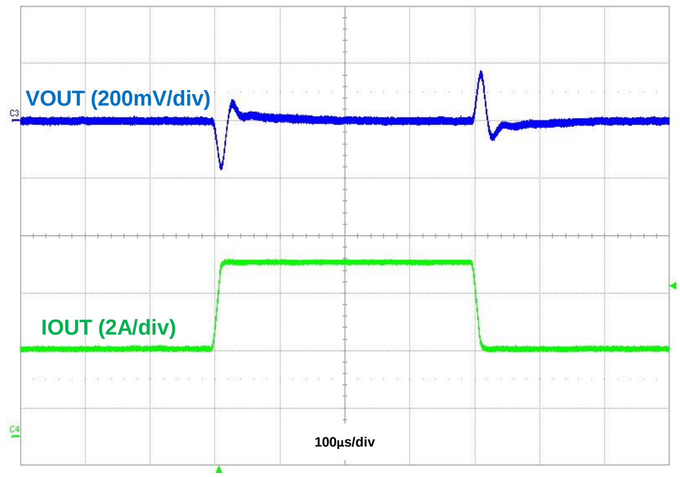


Figure 32. Load Transient, IOUT = 3A to 6A to 3A

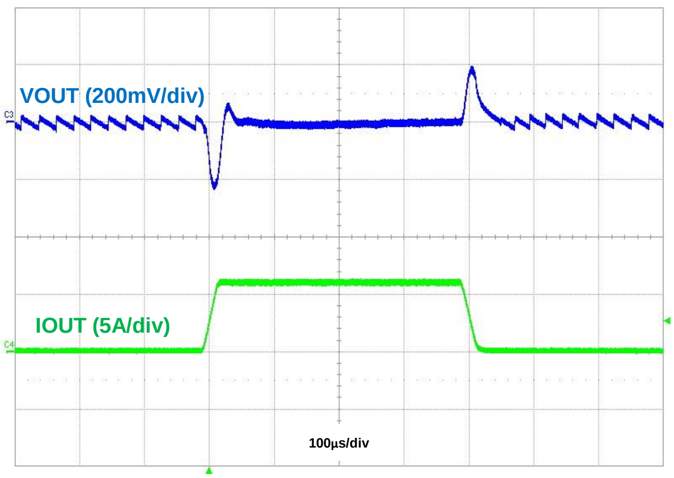


Figure 33. Load Transient, IOUT = 50mA to 6A to 50mA

Typical Performance Characteristics (AP62600 at T_A = +25°C, VIN = 12V, VOUT = 5V, MODE = VCC (PWM), FSEL = Floating (f_{SW} = 800kHz), SS/TR = Floating (t_{SS} = 1ms), unless otherwise specified.)

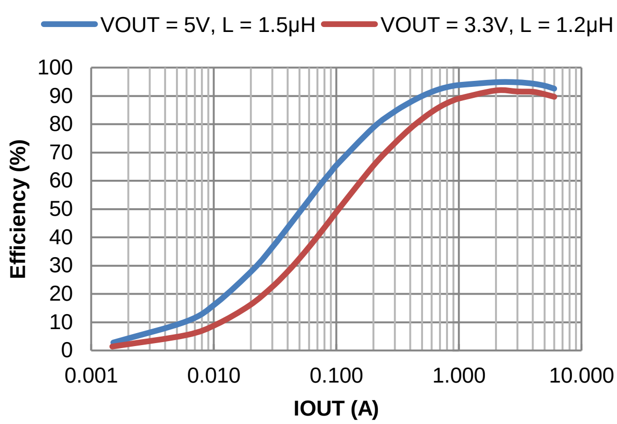


Figure 34. Efficiency vs. Output Current, VIN = 12V

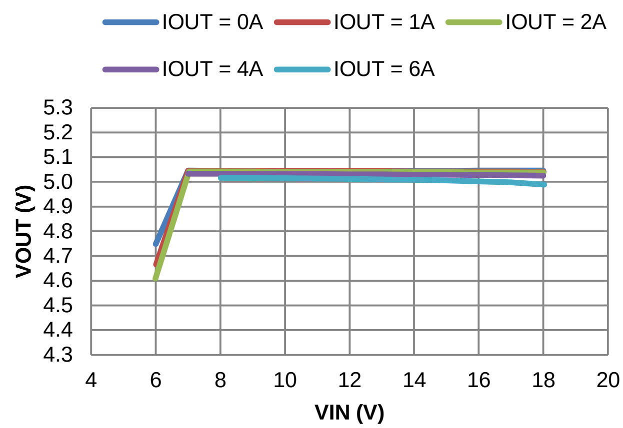


Figure 35. Line Regulation

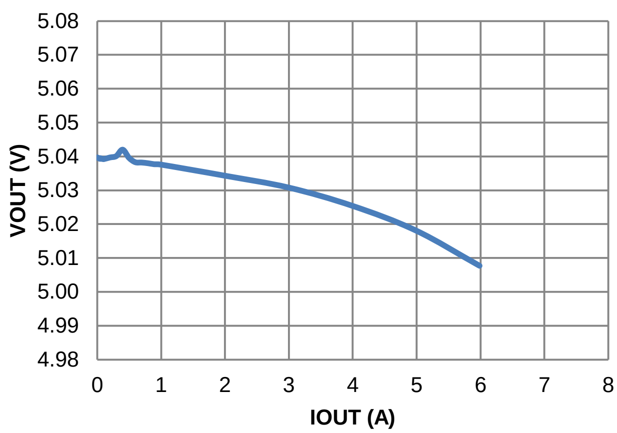


Figure 36. Load Regulation

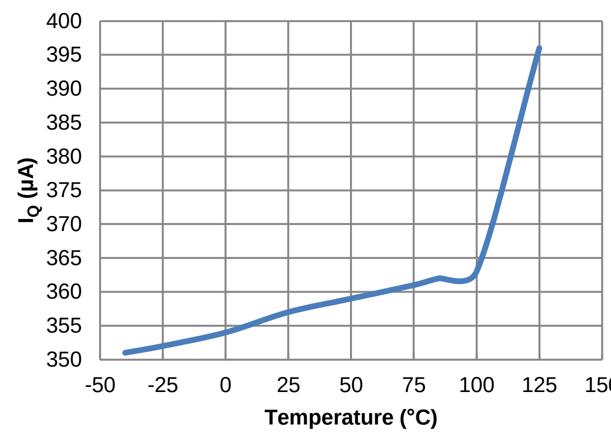


Figure 37. I_Q vs. Temperature

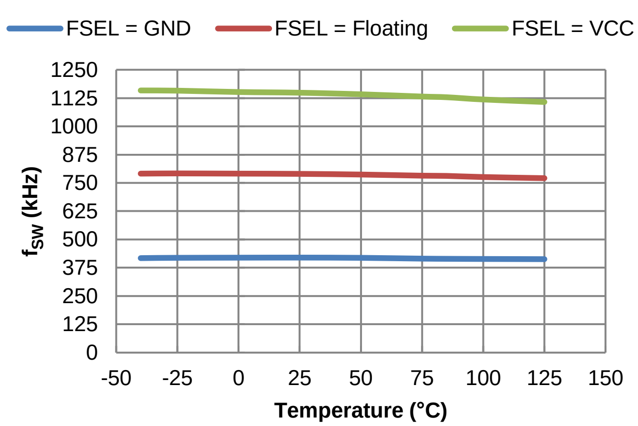


Figure 38. f_{SW} vs. Temperature, IOUT = 0A

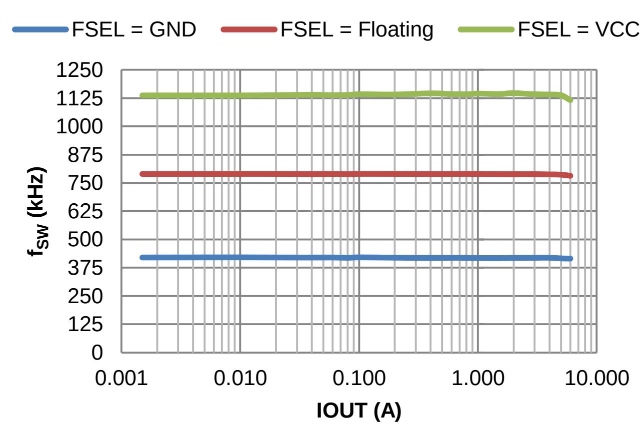


Figure 39. f_{SW} vs. Load

Typical Performance Characteristics (AP62600 at T_A = +25°C, VIN = 12V, VOUT = 5V, MODE = VCC (PWM), FSEL = Floating (f_{SW} = 800kHz), SS/TR = Floating (t_{SS} = 1ms), unless otherwise specified.) (continued)

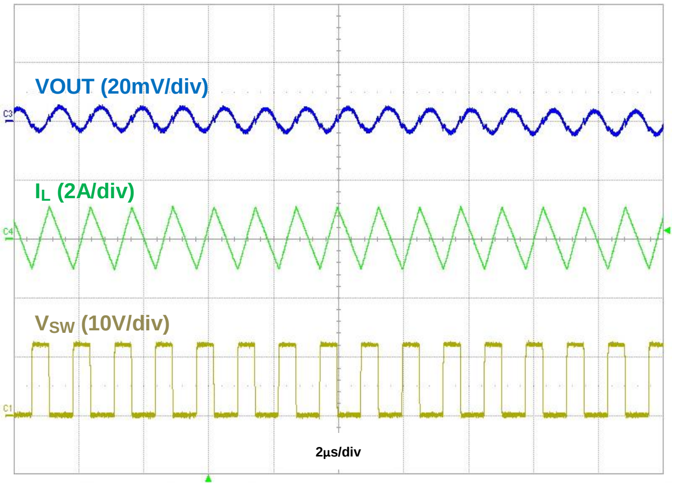


Figure 40. Output Voltage Ripple, IOUT = 50mA

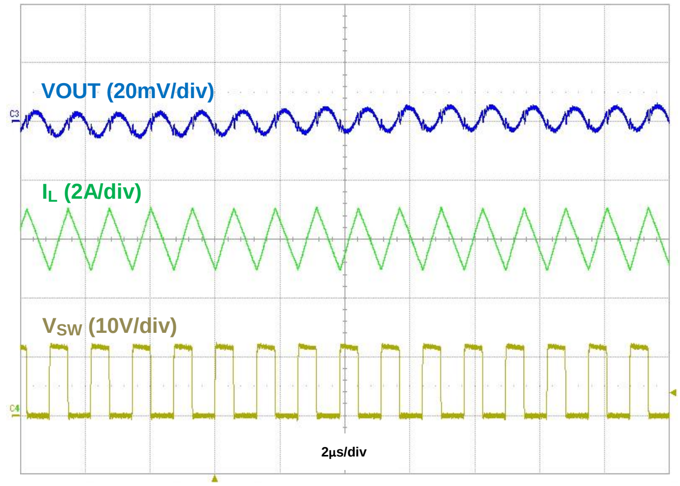


Figure 41. Output Voltage Ripple, IOUT = 6A

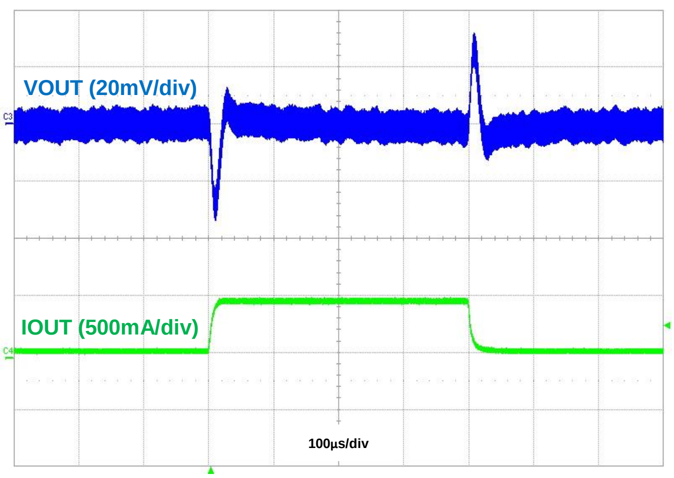


Figure 42. Load Transient, IOUT = 50mA to 500mA to 50mA

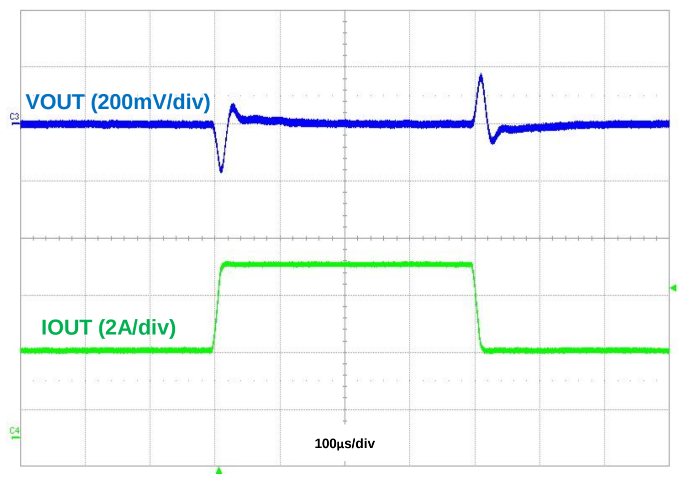


Figure 43. Load Transient, IOUT = 3A to 6A to 3A

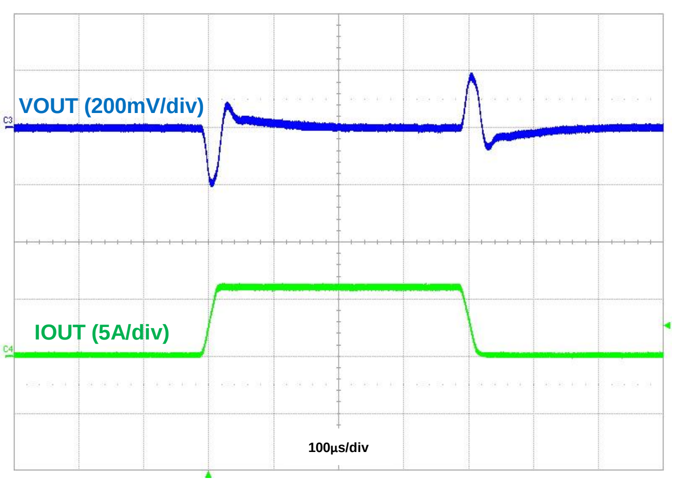


Figure 44. Load Transient, IOUT = 50mA to 6A to 50mA

Application Information

1 Pulse Width Modulation (PWM) Operation

The AP62600 device is a 4.5V-to-18V input, 6A output, EMI friendly, fully integrated synchronous buck converter. Refer to the block diagram in Figure 4. The device employs constant on-time control to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the one-shot pulse turns on the high-side power MOSFET, Q1, for a fixed on-time, t_{ON}. This one-shot on-pulse timing is calculated by the converter's input voltage and output voltage to maintain a pseudo-fixed frequency over the input voltage range. When Q1 is on, the inductor current rises linearly and the device charges the output capacitor. Q1 turns off after the fixed on-time expires, and the low-side power MOSFET, Q2, turns on. Once the output voltage drops below the output regulation, Q2 turns off. The one-shot timer is then reset and Q1 turns on again. The on-time is inversely proportional to the input voltage and directly proportional to the output voltage. It is calculated by the following equation:

$$\mathbf{t_{ON}} = \frac{\mathbf{VOUT}}{\mathbf{VIN \cdot f_{SW}}} \quad \text{Eq. 1}$$

Where:

- VIN is the input voltage
- VOUT is the output voltage
- f_{SW} is the switching frequency

The off-time duration is t_{OFF} and starts after the on-time expires. The off-time expires when the feedback voltage decreases below the reference voltage, which then triggers the on-time duration to start again. The minimum off-time is 255ns typical.

Connecting the MODE pin to VCC programs the device to operate in PWM Mode regardless of output load.

2 Pulse Frequency Modulation (PFM) and Ultrasonic Mode (USM) Operation

AP62600 enters PFM operation at light load conditions for high efficiency when the MODE pin is tied to GND. During light load conditions, the regulator automatically reduces the switching frequency. As the output current decreases, so too does the inductor current. The inductor current, I_L, eventually reaches 0A, marking the boundary between Continuous Conduction Mode (CCM) and Discontinuous Condition Mode (DCM). During this time, both Q1 and Q2 are off, and the load current is provided only by the output capacitor. When V_{FB} becomes lower than 0.6V, the next cycle begins, and Q1 turns on.

Likewise, as the output load increases from light load to heavy load, the switching frequency increases to maintain the regulation of the output voltage. The transition point between light and heavy load conditions can be calculated using the following equation:

$$\mathbf{I_{LOAD}} = \left(\frac{\mathbf{VIN - VOUT}}{\mathbf{2L}}\right) \cdot \mathbf{t_{ON}} \quad \text{Eq. 2}$$

Where:

- L is the inductor value

AP62600 enters USM during light load conditions when the MODE pin is left floating. USM is similar to PFM Mode but with one key difference. Unlike in PFM Mode, operating in USM limits the switching frequency of the device from going below 22kHz. This prevents the device from switching in the audible frequency range. When the regulator detects that no switching has occurred within the last 35us, it turns on Q2 for a fixed amount of time to force switching action on SW.

The quiescent current of AP62600 is 360µA typical under a no-load, non-switching condition.

Application Information (continued)

3 Enable

When disabled, the device shutdown supply current is only 1µA. When applying a voltage greater than the EN logic high threshold (typical 1.2V, rising), the AP62600 enables all functions and the device initiates the soft-start phase. An internal 1.4µA pull-up current source connected from the internal LDO-regulated VCC to the EN pin guarantees that if EN is left floating, the device still automatically enables once the voltage reaches the EN logic high threshold. The AP62600 has a built-in 1ms soft-start time to prevent output voltage overshoot and inrush current. The soft-start time is also programmable by connecting an external capacitor from SS/TR to GND. See **Soft-start, Tracking, and Sequencing** section for more details. When the EN voltage falls below its logic low threshold (typical 1.12V, falling), the internal SS voltage discharges to ground and device operation disables.

The EN pin can also be used to program the undervoltage lockout thresholds. See **Adjusting Undervoltage Lockout (UVLO)** section for more details.

4 Soft-Start, Tracking, and Sequencing

When the SS/TR pin is left floating, the AP62600 uses its built-in soft-start time, t_{SS}, of 1ms. The soft-start time can be extended by connecting an external capacitor from SS/TR to GND. The capacitor, along with the internal I_{SS} of 5µA, determines the new soft-start time. The capacitance required for a given programmed soft-start time is calculated by:

$$C_{SS}[nF] = 8.33 \cdot t_{SS}[ms] \quad \text{Eq. 3}$$

Where:

- C_{SS} is the soft-start capacitance in nF
- t_{SS} is the soft-start time in ms

Two AP62600 devices, IC#1 and IC#2, can be used in a ratiometric tracking configuration. Each AP62600 device shares the same C_{SS} capacitance, which programs the same soft-start time for each device. See Figure 45 and Figure 46 for more details.

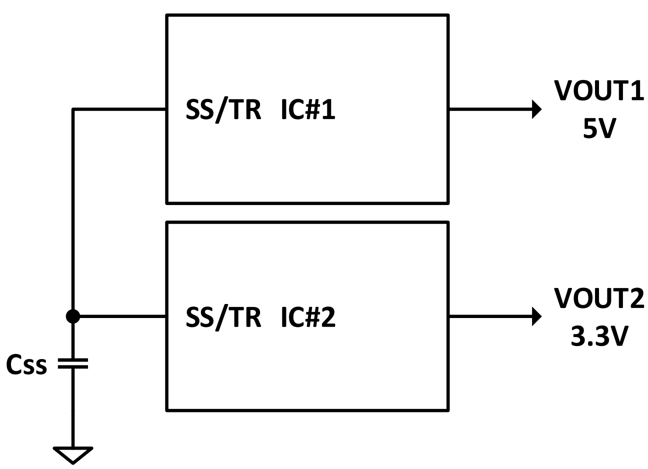


Figure 45. Ratiometric Tracking Configuration

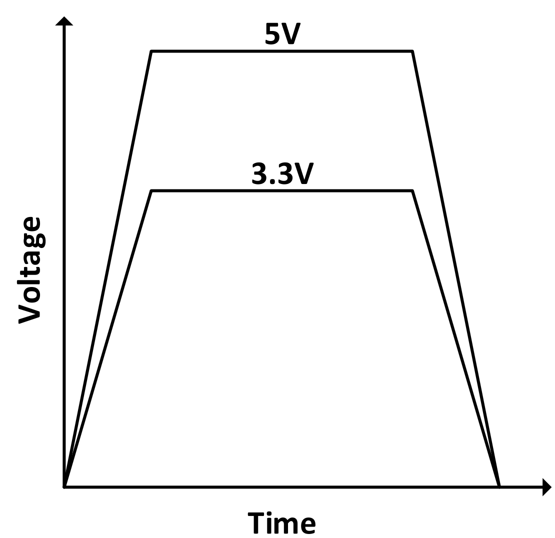


Figure 46. Ratiometric Tracking Function

Application Information (cont.)

4 Soft-start, Tracking, and Sequencing (continued)

Two AP62600 devices can be used in a coincidental tracking configuration. The higher voltage output of IC#1 is divided down to connect to the input of IC#2's SS/TR pin, which overrides IC#2's internal 0.6V reference voltage during start-up. Each AP62600 device has the same output voltage rising and falling slew rates. The resistive divider (R5 and R6) should have a ratio that matches the ratio of the feedback resistive divider of IC#2. See Figure 47 and Figure 48 for more details.

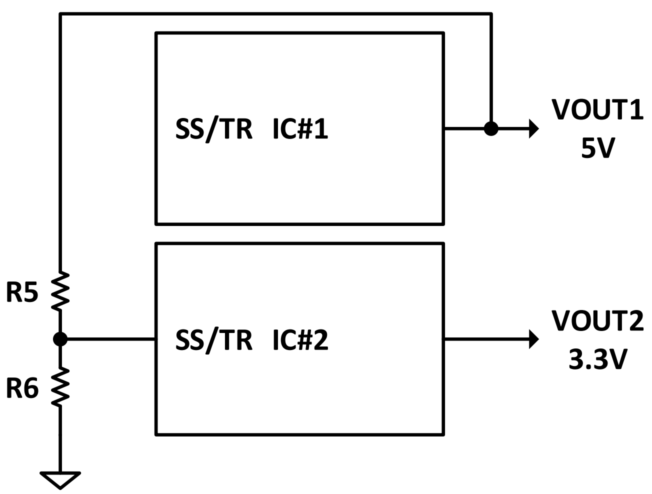


Figure 47. Coincidental Tracking Configuration

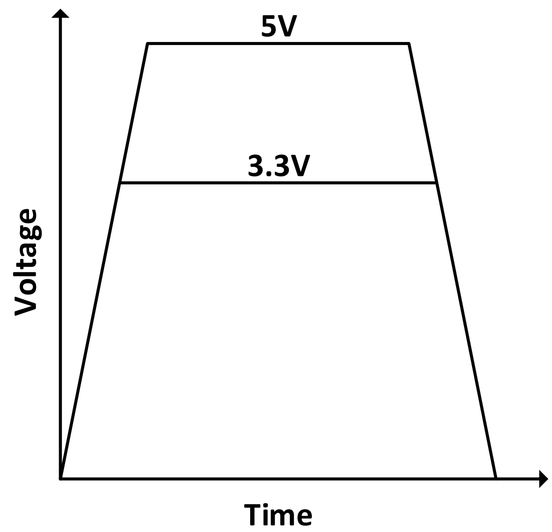


Figure 48. Coincidental Tracking Function

Two AP62600 devices can be used in an output sequencing configuration. Once the output voltage of IC#1 is within regulation, its PG signal goes from low to high and enables the start-up sequence of IC#2. See Figure 49 and Figure 50 for more details.

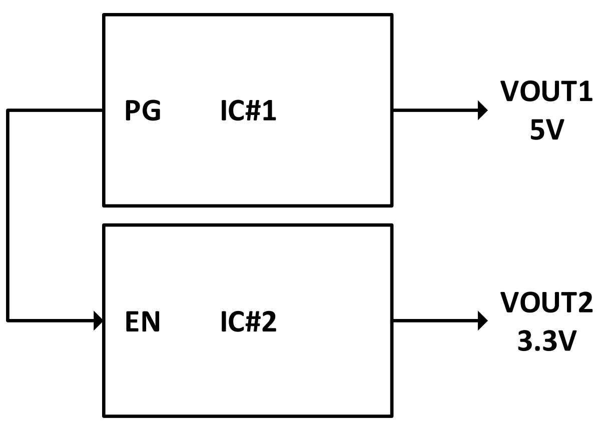


Figure 49. Output Sequencing Configuration

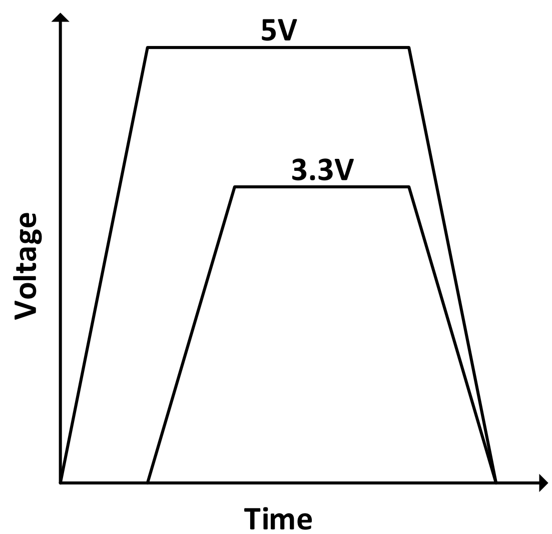


Figure 50. Output Sequencing Function

5 Electromagnetic Interference (EMI) Reduction with Ringing-Free Switching Node

In some applications, the system must meet EMI standards. In relation to high frequency radiation EMI noise, the switching node's (SW's) ringing amplitude is especially critical. To dampen high frequency radiated EMI noise, the AP62600 device implements a proprietary, multi-level gate driver scheme that achieves a ringing-free switching node without sacrificing the switching node's rise and fall slew rates as well as the converter's power efficiency.

Application Information (cont.)

6 Power-Good (PG) Indicator

The PG pin of AP62600 is an open-drain output that is actively held low during the soft-start period until the output voltage reaches 95% of its target value. When the output voltage is outside of its regulation by ±15%, PG pulls low until the output returns within 5% of its set value. The PG rising edge transition is delayed by 0.5ms. Connect an external pull-up resistor of 100kΩ from PG to VCC.

7 Adjusting Undervoltage Lockout (UVLO)

Undervoltage lockout is implemented to prevent the IC from insufficient input voltages. The AP62600 device has a UVLO comparator that monitors the input voltage and the internal bandgap reference. The AP62600 disables if the input voltage falls below 3.95V. In this UVLO event, both the high-side and low-side power MOSFETs turn off.

Some applications may desire higher VIN UVLO threshold voltages than is provided by the default setup. A 3.7µA hysteresis pull-up current source on the EN pin along with an external resistive divider (R3 and R4) configures the VIN UVLO threshold voltages as shown in Figure 51.

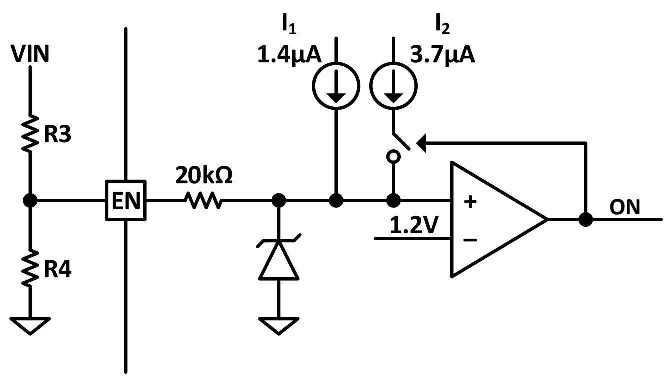


Figure 51. Programming UVLO

The resistive divider resistor values are calculated by:

$$\mathbf{R3} = \frac{\mathbf{0.933 \cdot V_{ON} - V_{OFF}}}{\mathbf{3.793\mu A}} \qquad \text{Eq. 4}$$

$$\mathbf{R4} = \frac{\mathbf{1.12 \cdot R3}}{\mathbf{V_{OFF} - 1.12V + 5.1\mu A \cdot R3}} \qquad \text{Eq. 5}$$

Where:

- V_{ON} is the rising edge VIN voltage to enable the regulator and is greater than 4.45V
- V_{OFF} is the falling edge VIN voltage to disable the regulator and is greater than 4.15V

8 Overcurrent Protection (OCP)

The AP62600 has cycle-by-cycle valley current limit protection by sensing the current through the internal low-side power MOSFET, Q2. While Q2 is on, the internal sensing circuitry monitors its conduction current. The overcurrent limit has a corresponding voltage limit, V_{LIMIT}. When the voltage between GND and SW is lower than V_{LIMIT} due to excessive current through Q2, the OCP triggers, and the controller turns off Q2. During this time, both Q1 and Q2 remain off. A new switching cycle begins only when the voltage between GND and SW rises above V_{LIMIT}. If Q2 consistently hits the valley current limit for $1 \cdot t_{SS}$, the buck converter enters hiccup mode and shuts down. After $7 \cdot t_{SS}$ of down time, the buck converter restarts powering up. Hiccup mode reduces the power dissipation in the overcurrent condition.

Because the $R_{DS(ON)}$ values of the power MOSFETs increase with temperature, V_{LIMIT} has a temperature coefficient of 0.4%/°C to compensate for the temperature dependency of $R_{DS(ON)}$.

Application Information (cont.)

9 Thermal Shutdown (TSD)

If the junction temperature of the device reaches the thermal shutdown limit of 160°C, the AP62600 shuts down both its high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (130°C typical), the device initiates a normal power-up cycle with soft-start.

10 Power Derating Characteristics

To prevent the regulator from exceeding the maximum recommended operating junction temperature, some thermal analysis is required. The regulator's temperature rise is given by:

$$\mathbf{T_{RISE} = PD \cdot (\theta_{JA})} \qquad \textbf{Eq. 6}$$

Where:

- PD is the power dissipated by the regulator
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature

The junction temperature, T_J, is given by:

$$\mathbf{T_J = T_A + T_{RISE}} \qquad \textbf{Eq. 7}$$

Where:

- T_A is the ambient temperature of the environment

For the V-QFN2030-12 (Type A) package, the θ_{JA} is 40°C/W. The actual junction temperature should not exceed the maximum recommended operating junction temperature of 125°C when considering the thermal design. Figure 52 shows a typical derating curve versus ambient temperature.

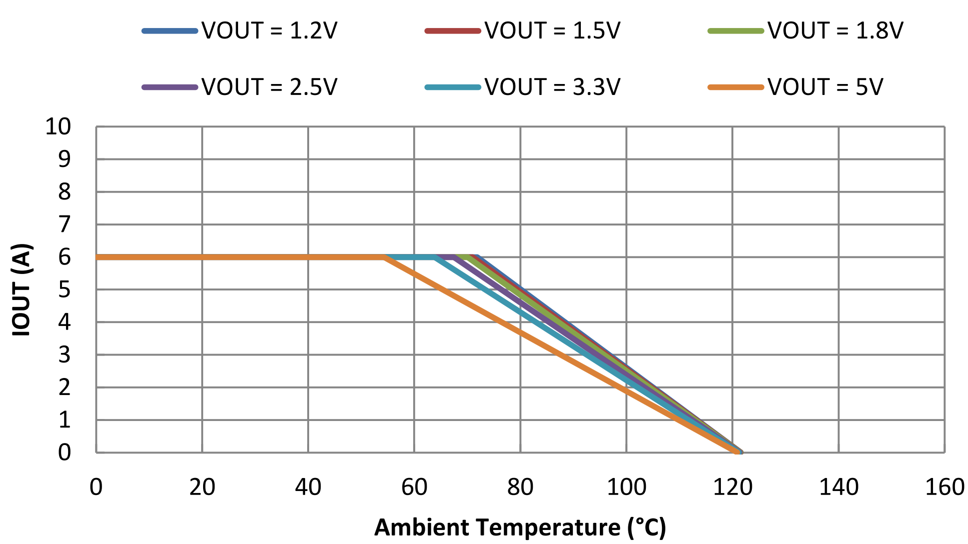


Figure 52. Output Current Derating Curve vs. Ambient Temperature, VIN = 12V, f_{SW} = 800kHz

Application Information (cont.)

11 Setting the Output Voltage

The AP62600 has an adjustable output voltage, starting from 0.6V, using an external resistive divider. The resistor values of the feedback network are selected based on a design trade-off between efficiency and output voltage accuracy. There is less current consumption in the feedback network for high resistor values, which improves efficiency at light loads. However, values too high cause the device to be more susceptible to noise affecting its output voltage accuracy. R1 can be determined by the following equation:

$$\mathbf{R1} = \mathbf{R2} \cdot \left(\frac{\mathbf{VOUT}}{\mathbf{0.6V}} - \mathbf{1}\right) \quad \textbf{Eq. 8}$$

Table 1 shows a list of recommended component selections for common AP62600 output voltages referencing Figure 1. The AP62600 is capable of delivering output voltages greater than the listed maximum recommended output voltage of 7.0V by modifying the typical application circuit with additional external components. Consult Diodes Incorporated for more information if such output voltages are required.

Table 1. Recommended Component Selections

AP62600							
Output Voltage (V)	**Frequency (kHz)**	**R1 (kΩ)**	**R2 (kΩ)**	**L (µH)**	**C1 (µF)**	**C2 (µF)**	**C3 (nF)**
1.2	400	30.1	30.1	1.5	22	3 x 22	100
	800			0.68			
	1200			0.47			
1.5	400	45.3	30.1	2.2	22	3 x 22	100
	800			0.68			
	1200			0.47			
1.8	400	60.4	30.1	2.2	22	3 x 22	100
	800			0.82			
	1200			0.68			
2.5	400	95.3	30.1	2.2	22	3 x 22	100
	800			1.0			
	1200			0.68			
3.3	400	137.0	30.1	4.7	22	3 x 22	100
	800			1.2			
	1200			0.82			
5.0	400	221.0	30.1	4.7	22	3 x 22	100
	800			1.5			
	1200			1.0			

Application Information (cont.)

12 Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$\mathbf{L = \frac{VOUT \cdot (VIN - VOUT)}{VIN \cdot \Delta I_L \cdot f_{SW}}} \quad \textbf{Eq. 9}$$

Where:

- ΔI_L is the inductor current ripple
- f_{SW} is the buck converter switching frequency

For AP62600, choose ΔI_L to be 30% to 50% of the maximum load current of 6A.

The inductor peak current is calculated by:

$$\mathbf{I_{L_{PEAK}} = I_{LOAD} + \frac{\Delta I_L}{2}} \quad \textbf{Eq. 10}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal power MOSFETs. Therefore, choosing an inductor with the appropriate saturation current rating is important. For most applications, it is recommended to select an inductor of approximately 0.47µH to 4.7µH with a DC current rating of at least 35% higher than the maximum load current. For highest efficiency, the inductor's DC resistance should be less than 10mΩ. Use a larger inductance for improved efficiency under light load conditions.

Application Information (cont.)

13 Input Capacitor

The input capacitor reduces both the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor must sustain the ripple current produced during the on-time of Q1. It must have a low ESR to minimize power dissipation due to the RMS input current.

The RMS current rating of the input capacitor is a critical parameter and must be higher than the RMS input current. As a rule of thumb, select an input capacitor with an RMS current rating greater than half of the maximum load current.

Due to large dI/dt through the input capacitor, electrolytic or ceramic capacitors with low ESR should be used. If using a tantalum capacitor, it must be surge protected or else capacitor failure could occur. Using a ceramic capacitor of 22µF or greater is sufficient for most applications.

14 Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces both the overshoots and undershoots of the output voltage during load transients. During the first few microseconds of an increasing load transient, the converter recognizes the change from steady-state and sets the off-time to minimum to supply more current to the load. However, the inductor limits the change to increasing current depending on its inductance. Therefore, the output capacitor supplies the difference in current to the load during this time. Likewise, during the first few microseconds of a decreasing load transient, the converter recognizes the change from steady-state and increases the off-time to reduce the current supplied to the load. However, the inductor limits the change in decreasing current as well. Therefore, the output capacitor absorbs the excess current from the inductor during this time.

The effective output capacitance, COUT, requirements can be calculated from the equations below.

The ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated by:

$$\mathbf{VOUT_{Ripple}} = \Delta \mathbf{I_L} \cdot \left(\mathbf{ESR} + \frac{\mathbf{1}}{\mathbf{8} \cdot \mathbf{f_{SW}} \cdot \mathbf{COUT}}\right) \quad \text{Eq. 11}$$

An output capacitor with large capacitance and low ESR is the best option. For most applications, a 22µF to 68µF ceramic capacitor is sufficient. To meet the load transient requirements, the calculated COUT should satisfy the following inequality:

$$\mathbf{COUT} > \mathbf{max}\left(\frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Overshoot}} \cdot \mathbf{VOUT}}, \frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Undershoot}} \cdot (\mathbf{VIN} - \mathbf{VOUT})}\right) \quad \text{Eq. 12}$$

Where:

- I_{Trans} is the load transient
- $\Delta V_{Overshoot}$ is the maximum output overshoot voltage
- $\Delta V_{Undershoot}$ is the maximum output undershoot voltage

13 Bootstrap Capacitor

To ensure proper operation, a ceramic capacitor must be connected between the BST and SW pins to supply the drive voltage for the high-side power MOSFET. A 100nF ceramic capacitor is sufficient.

Layout

PCB Layout

1. The AP62600 works at 6A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and PGND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to PGND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as PGND to maximize thermal performance.
7. Add as many vias as possible around both the PGND pin and under the PGND plane for heat dissipation to all the PGND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 53 for more details.

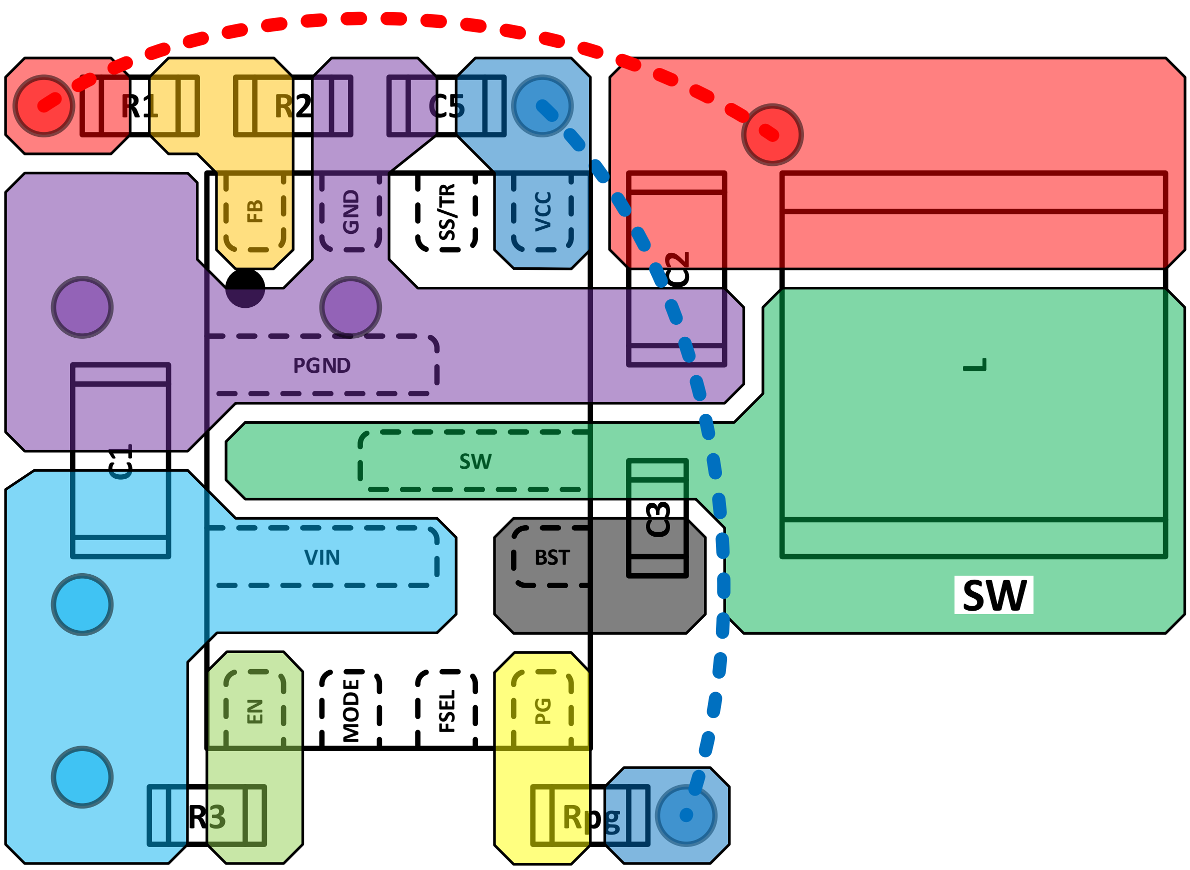
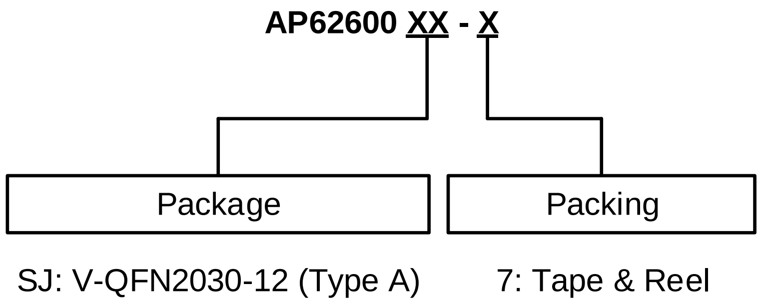


Figure 53. Recommended PCB Layout

Ordering Information

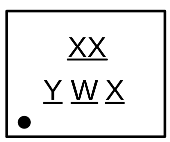


Orderable Device	Package Code	Tape and Reel	
		Quantity	Part Number Suffix
AP62600SJ-7	SJ	3000	-7

Marking Information

V-QFN2030-12 (Type A)

(Top View)



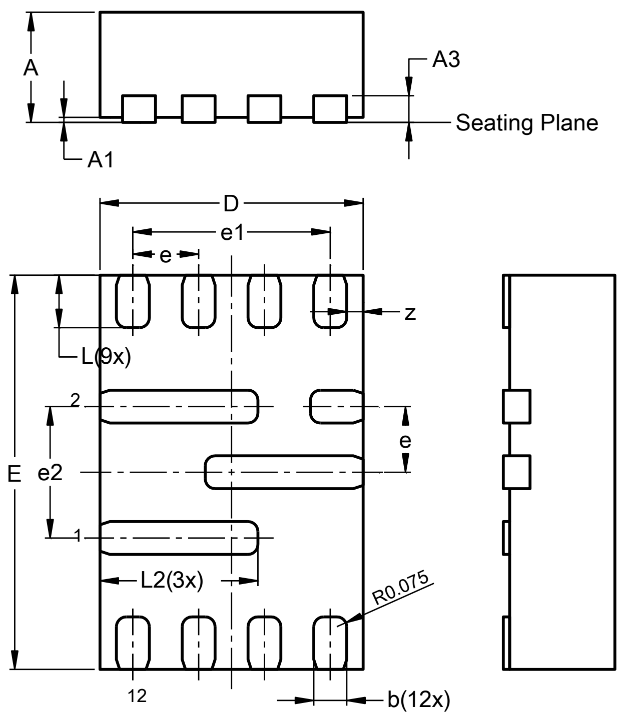
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Orderable Device	Package	Identification Code
AP62600SJ-7	V-QFN2030-12 (Type A)	K2

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-QFN2030-12 (Type A)

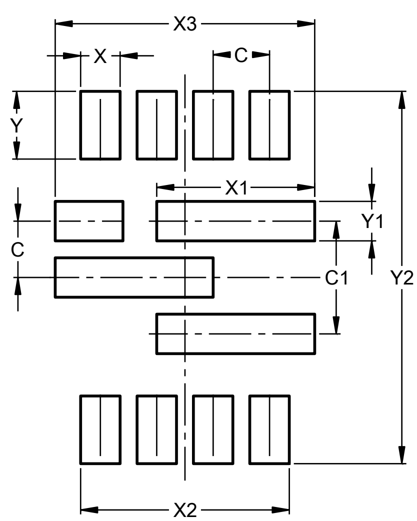


V-QFN2030-12 (Type A)			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	—	—	0.203
b	0.20	0.30	0.25
D	1.95	2.05	2.00
E	2.95	3.05	3.00
e	0.50 BSC		
e1	1.50 BSC		
e2	1.00 BSC		
L	0.35	0.45	0.40
L2	1.15	1.25	1.20
z	—	—	0.125
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-QFN2030-12 (Type A)



Dimensions	Value (in mm)
C	0.500
C1	1.000
X	0.350
X1	1.400
X2	1.850
X3	2.300
Y	0.600
Y1	0.350
Y2	3.300