



20V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

V _{(BR)DSS}	R _{DS(ON) max}	I _{D max} T _A = +25°C
20V	$9.5 \text{m}\Omega @ V_{GS} = 4.5 \text{V}$	11.7A
	$11m\Omega$ @ $V_{GS} = 2.5V$	10.8A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- · General Purpose Interfacing Switch
- Power Management Functions

Features

- 0.6mm Profile Ideal for Low Profile Applications
- PCB Footprint of 4mm²
- Low Gate Threshold Voltage
- Low On-Resistance
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

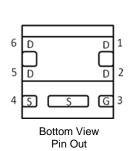
Mechanical Data

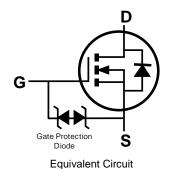
- Case: U-DFN2020-6
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (e4)
- Weight: 0.0065 grams (Approximate)





Bottom View





Ordering Information (Note 4)

Part Number	Marking	Reel size (inches)	Quantity per reel
DMN2011UFDE-7	N3	7	3,000
DMN2011UFDE-13	N3	13	10,000

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



N3 = Product Type Marking Code YM = Date Code Marking Y = Year (ex: A = 2013) M = Month (ex: 9 = September)

Date Code Key

Year	201	1	2012		2013	20	14	2015		2016		2017
Code	Υ		Z		Α	E	3	С		D		Е
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units		
Drain-Source Voltage	V_{DSS}	20	V		
Gate-Source Voltage			V_{GSS}	±12	V
Continuous Drain Current (Note 6) V 4.5V	Steady State	$T_A = +25$ °C $T_A = +70$ °C	ID	11.7 9.3	А
Continuous Drain Current (Note 6) V _{GS} = 4.5V	t<10s	$T_A = +25$ °C $T_A = +70$ °C	ΙD	14.2 11.4	А
$\begin{array}{cccc} & & & & & & \\ & & & & & \\ & & & & \\ & & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & \\ & & & \\ & \\ & & \\ & & \\ & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & $			ΙD	10.8 8.7	А
Continuous Drain Current (Note 6) V _{GS} = 2.5V	t<10s	$T_A = +25$ °C $T_A = +70$ °C	Ι _D	13.2 10.6	А
Pulsed Drain Current (10µs pulse, duty cycle = 1%)	I _{DM}	80	Α		
Maximum Body Diode Continuous Current	Is	2.5	Α		
Avalanche Current (Note 7) L = 0.1mH	I _{AS}	18	A		
Avalanche Energy (Note 7) L = 0.1mH	E _{AS}	17	mJ		

Thermal Characteristics

Characteristic	Characteristic			
Total Davier Dissination (Nata 5)	T _A = +25°C	<u> </u>	0.61	W
Total Power Dissipation (Note 5)	T _A = +70°C	P_{D}	0.39	
Thermal Desistance Junction to Ambient (Note 5)	Steady state	Б	209	°C/W
Thermal Resistance, Junction to Ambient (Note 5)	t<10s	$R_{ heta JA}$	142	
Total Dawar Dissination (Note C)	$T_A = +25$ °C	6	1.97	W
Total Power Dissipation (Note 6)	T _A = +70°C	P_{D}	1.27	
Thermal Registence, Junction to Ambient (Note 6)	Steady state	D	64	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	t<10s	$R_{ hetaJA}$	43	
Thermal Resistance, Junction to Case (Note 6)	R ₀ JC	9.8		
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C	

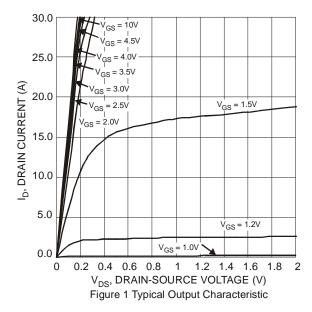


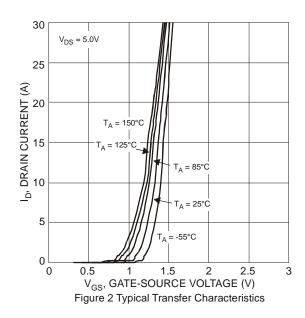
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						•
Drain-Source Breakdown Voltage	BV _{DSS}	20	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}		_	1	μA	$V_{DS} = 16V, V_{GS} = 0V$
Zero Gate Voltage Drain Current T _J = +150°C (Note 9)	I _{DSS}		_	100	μA	$V_{DS} = 16V, V_{GS} = 0V$
Gate-Source Leakage	I _{GSS}		_	±10	μΑ	$V_{GS} = \pm 10V$, $V_{DS} = 0V$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(th)}	0.4	_	1.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
			6.5	9.5		$V_{GS} = 4.5V, I_D = 7A$
Static Drain-Source On-Resistance	D		7.5	11	mΩ	$V_{GS} = 2.5V, I_D = 7A$
Static Dialii-Source Oil-Resistance	R _{DS(ON)}	_	10	20	11122	$V_{GS} = 1.8V, I_D = 5A$
			15	35		$V_{GS} = 1.5V, I_D = 3A$
Diode Forward Voltage	V_{SD}	_	0.7	1.2	V	$V_{GS} = 0V, I_{S} = 8.5A$
On State Drain Current (Note 9)	ID(ON)	20	_	_	Α	$V_{DS} \leq 5V$, $V_{GS} = 4.5V$
DYNAMIC CHARACTERISTICS (Note 9)	•		•		•	•
Input Capacitance	C _{iss}	_	2248	3372	pF	
Output Capacitance	Coss	_	295	443	pF	$V_{DS} = 10V, V_{GS} = 0V,$ - f = 1.0MHz
Reverse Transfer Capacitance	C _{rss}	_	265	398	pF	1 - 1.000112
Gate Resistance	Rg	_	1.5	3	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	24	36	nC	
Total Gate Charge (V _{GS} = 10V)	Qg		56	84	nC	
Gate-Source Charge	Qgs		3.5	6	nC	$V_{DS} = 10V, I_D = 8.5A$
Gate-Drain Charge	Q _{gd}	_	5.1	8	nC	
Turn-On Delay Time	t _{D(on)}	_	3.6	6	ns	
Turn-On Rise Time	tr	_	2.6	4	ns	$V_{DS} = 10V, I_{D} = 8.5A$
Turn-Off Delay Time	t _{D(off)}	_	21.6	33	ns	$V_{GS} = 4.5V, R_G = 1.8\Omega$
Turn-Off Fall Time	t _f	_	13.5	21	ns	
Reverse Recovery Time	T _{rr}	_	12.8	20	ns	L 0.5A 411/41 040A/
Reverse Recovery Charge	Q _{rr}	_	6.9	11	nC	I _F = 8.5A, di/dt = 210A/μs

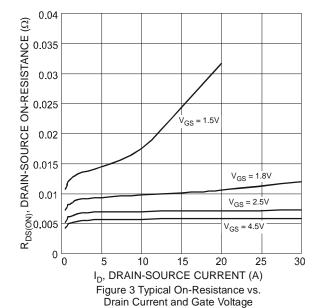
Notes:

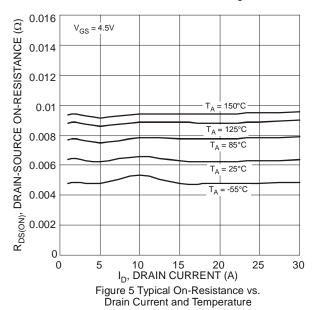
- 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
- 7. I_{AS} and E_{AS} rating are based on low frequency and duty cycles to keep T_J = +25°C
- 8. Short duration pulse test used to minimize self-heating effect.
 9. Guaranteed by design. Not subject to product testing.











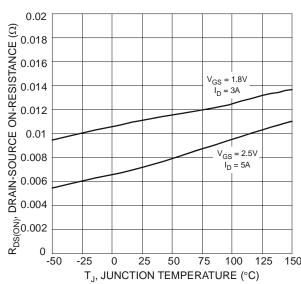
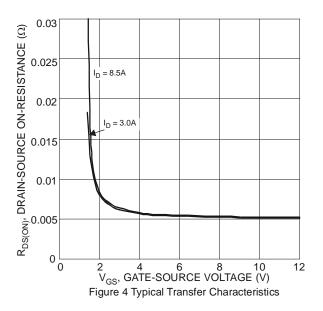


Figure 7 On-Resistance Variation with Temperature



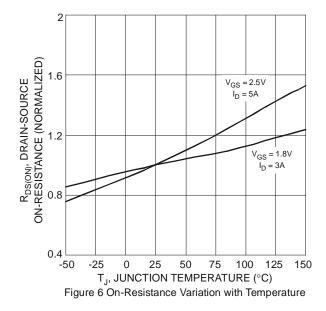
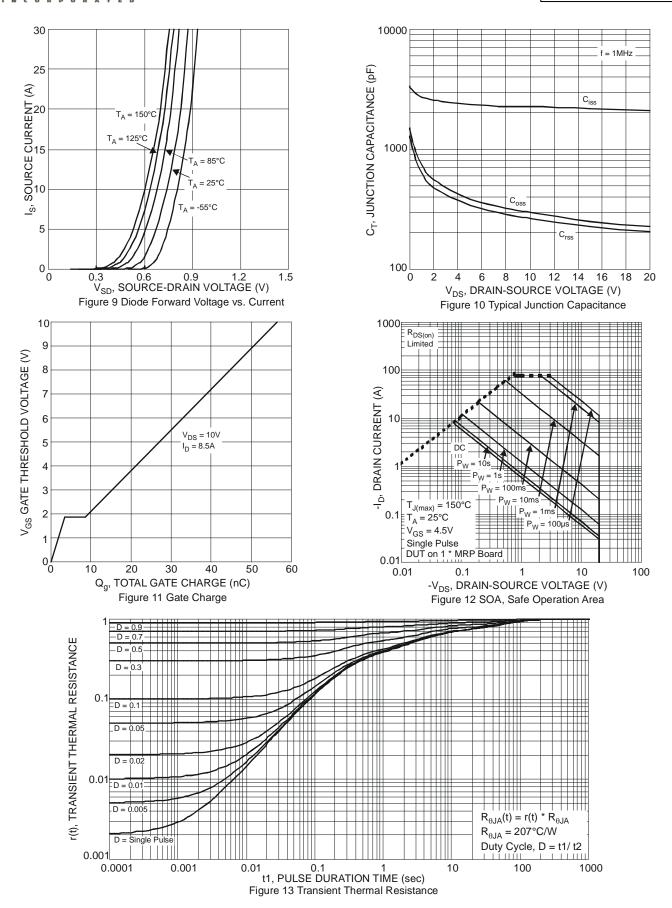


Figure 8 Gate Threshold Variation vs. Ambient Temperature

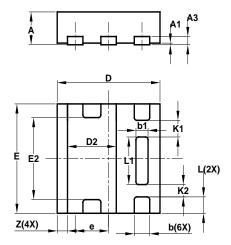






Package Outline Dimensions

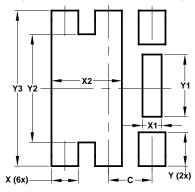
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



U-DFN2020-6								
Type E								
Dim	Dim Min Max Typ							
Α	0.57	0.63	0.60					
A1	0	0.05	0.03					
А3	_	_	0.15					
b	0.25	0.35	0.30					
b1	0.185	0.285	0.235					
D	1.95	2.05	2.00					
D2	0.85 1.05 0.9		0.95					
Е	1.95 2.05 2.0		2.00					
E2	1.40 1.60 1.50		1.50					
е	— — 0.65							
L	0.25 0.35 0.3		0.30					
L1	0.82 0.92 0.87		0.87					
K1	0		0.305					
K2	_	_	0.225					
Z		_	0.20					
All Dimensions in mm								

Suggested Pad Layout

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



Dimensions	Value (in mm)
С	0.650
Х	0.400
X1	0.285
X2	1.050
Υ	0.500
Y1	0.920
Y2	1.600
Y3	2.300



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