

## Description

The AP2401A and AP2411A are single-channel, current-limited, integrated high-side power switches optimized for Universal Serial Bus (USB) and other hot-swap applications. The family of devices complies with USB standards and is available with both polarities of enable input.

The devices have fast short-circuit response time for improved overall system robustness, and have integrated output discharge function to ensure completely controlled discharging of the output voltage capacitor. They provide a complete protection solution for applications subject to heavy capacitive loads and the prospect of short circuit, and offer reverse current blocking, overcurrent, over-temperature and short-circuit protection, as well as controlled rise time and undervoltage lockout functionality. A 7ms deglitch capability on the open-drain Flag output prevents false overcurrent reporting and does not require any external components. AP2401A and AP2411A will be latched off after a 7ms deglitch.

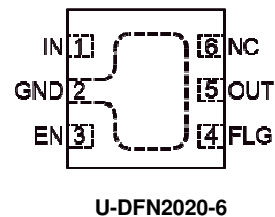
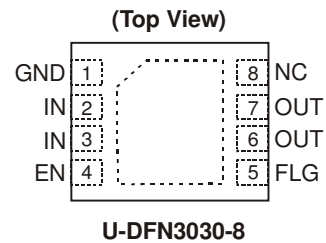
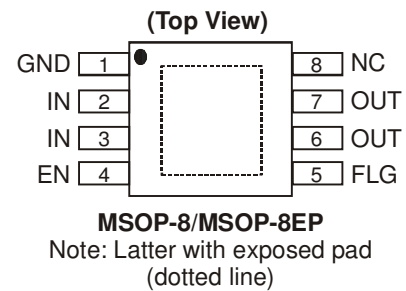
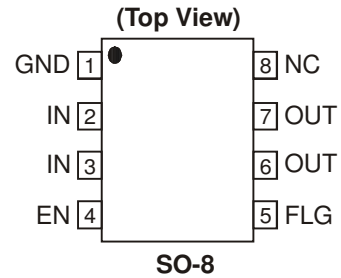
All devices are available in SO-8, MSOP-8, MSOP-8EP, U-DFN3030-8 and U-DFN2020-6 packages.

## Features

- Single Channel Current-Limited Power Switch
- Output Discharge Function
- Output Current Latch-Off when OCP Triggered
- Fast Short-Circuit Response Time: 2 $\mu$ s
- 2.5A Accurate Current Limiting
- Reverse Current Blocking
- 70m $\Omega$  On-Resistance
- Input Voltage Range: 2.7V - 5.5V
- Built-In Soft-Start with 0.6ms Typical Rise Time
- Overcurrent and Thermal Protection
- Fault Report (FLG) with Blanking Time (7ms typ)
- ESD Protection: 2kV HBM, 200V MM
- Active Low (AP2401A) or Active High (AP2411A) Enable
- Ambient Temperature Range: -40 $^{\circ}$ C to +85 $^{\circ}$ C
- SO-8, MSOP-8, MSOP-8EP, U-DFN3030-8 and U-DFN2020-6: Available in "Green" Molding Compound (No Br, Sb)
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- UL Recognized, File Number E322375
- IEC60950-1 CB Scheme Certified

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

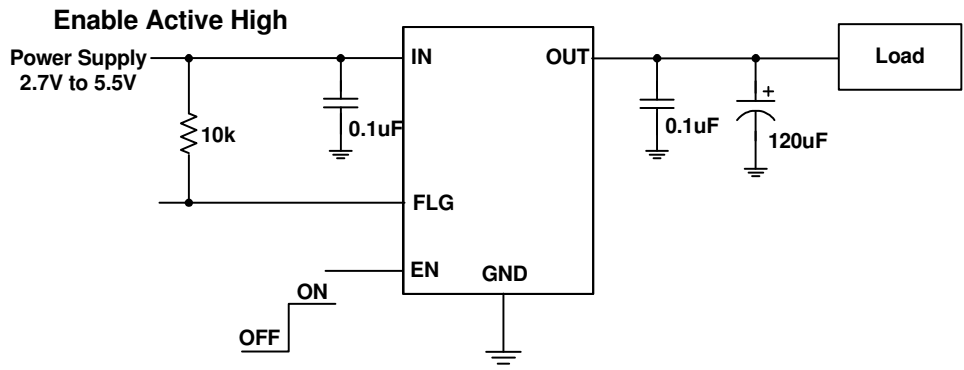
## Pin Assignments



## Applications

- LCD TVs & Monitors
- Set-Top-Boxes, Residential Gateways
- Laptops, Desktops, Servers, E-Readers
- Printers, Docking Stations, HUBs

### Typical Applications Circuit

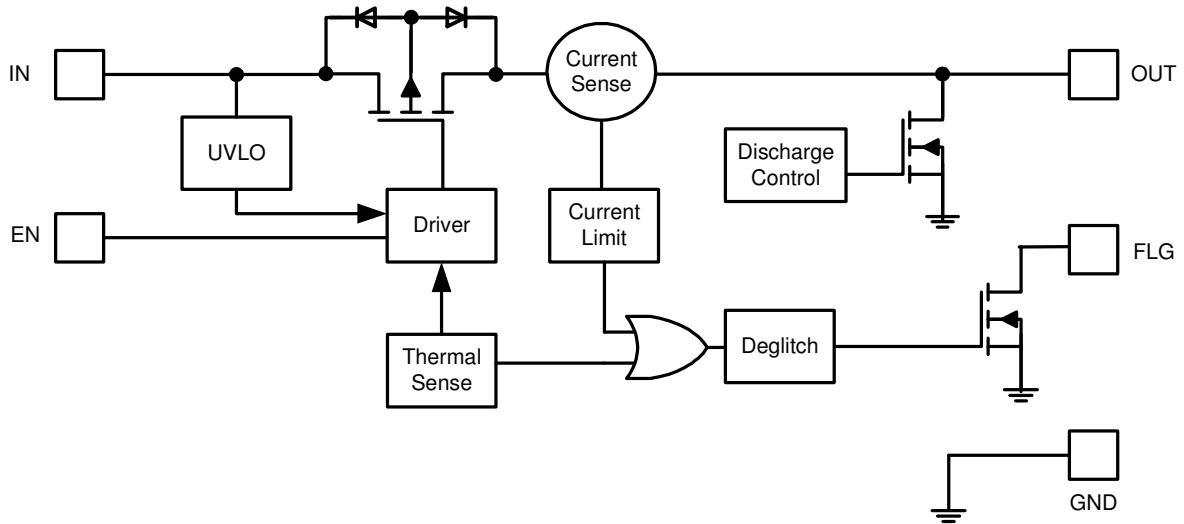


### Available Options

Part Number	Channel	Enable Pin (EN)	Recommended Maximum Continuous Load Current (A)	Typical Output Latch-Off Current Limit (A)	Package
AP2401A	1	Active Low	2	2.5	SO-8 MSOP-8 MSOP-8EP U-DFN3030-8 U-DFN2020-6
AP2411A	1	Active High			

### Pin Descriptions

Pin Name	Pin Number			Function
	SO-8, MSOP-8	MSOP-8EP, U-DFN3030-8	U-DFN2020-6	
GND	1	1	2	Ground
IN	2, 3	2, 3	1	Voltage Input Pin. Connect a 0.1µF or larger ceramic capacitor from IN to GND as close as possible. (all IN pins must be tied together externally)
EN	4	4	3	Enable Input. Active low (AP2401A) or active high (AP2411A).
FLG	5	5	4	Over-temperature and overcurrent fault reporting with 7ms deglitch; active low open-drain output. FLG is disabled for 7ms after turn-on.
OUT	6, 7	6, 7	5	Voltage Output Pin (all OUT pins must be tied together externally)
NC	8	8	6	No Internal Connection. Recommend tie to OUT pins.
Exposed Pad	—	Exposed Pad	Exposed Pad	Exposed pad. <b>It should be externally connected to GND plane and thermal mass for enhanced thermal impedance.</b> Exposed pad should not be used as electrical ground conduction path.

**Functional Block Diagram**

**Absolute Maximum Ratings** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body Model ESD Protection	4	kV
ESD MM	Machine Model ESD Protection	300	V
$V_{IN}$	Input Voltage (Note 4)	-0.3 to 6.5	V
$V_{OUT}$	Output Voltage (Note 4)	-0.3 to $V_{IN} + 0.3$ or 6.5	V
$V_{EN}, V_{FLG}$	Enable Voltage (Note 4)	-0.3 to $V_{IN} + 0.3$ or 6.5	V
$I_{LOAD}$	Maximum Continuous Load Current	Internal Limited	A
$T_{J(MAX)}$	Maximum Junction Temperature	150	$^\circ\text{C}$
$T_{ST}$	Storage Temperature Range (Note 4)	-65 to +150	$^\circ\text{C}$

- Notes:
4. All voltages referred to GND pin. Maximums are the lower of  $V_{IN} + 0.3$  and 6.5V.
  5. UL Recognized Rating from  $-30^\circ\text{C}$  to  $+70^\circ\text{C}$  (Diodes qualified  $T_{ST}$  from  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$ ).

Caution: Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

**Recommended Operating Conditions** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
$V_{IN}$	Input Voltage	2.7	5.5	V
$I_{OUT}$	Output Current	0	2	A
$V_{IL}$	EN Input Logic Low Voltage	0	0.8	V
$V_{IH}$	EN Input Logic High Voltage	2	$V_{IN}$	V
$T_A$	Operating Ambient Temperature	-40	+85	$^\circ\text{C}$

**Electrical Characteristics** (@ $T_A = +25^\circ\text{C}$ ,  $V_{IN} = +5.0\text{V}$ ,  $C_{IN} = 0.1\mu\text{F}$ ,  $C_L = 1\mu\text{F}$ , unless otherwise specified.)

Symbol	Parameter	Test Conditions (Note 5)	Min	Typ	Max	Unit	
$V_{UVLO}$	Input UVLO	$V_{IN}$ rising	1.6	2.0	2.4	V	
$\Delta V_{UVLO}$	Input UVLO Hysteresis	$V_{IN}$ decreasing	-	50	-	mV	
$I_{SHDN}$	Input Shutdown Current	Disabled, OUT = open	-	0.1	1	$\mu\text{A}$	
$I_Q$	Input Quiescent Current	Enabled, OUT = open	-	60	100	$\mu\text{A}$	
$I_{LEAK}$	Input Leakage Current	Disabled, OUT grounded	-	0.1	1	$\mu\text{A}$	
$I_{REV}$	Reverse Leakage Current	Disabled, $V_{IN} = 0\text{V}$ , $V_{OUT} = 5\text{V}$ , $I_{REV}$ at $V_{IN}$	-	0.01	1	$\mu\text{A}$	
$R_{DS(ON)}$	Switch on-Resistance	$V_{IN} = 5\text{V}$ , $I_{OUT} = 2.0\text{A}$	$T_A = +25^\circ\text{C}$	-	70	84	m $\Omega$
			$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	-	-	105	
		$V_{IN} = 3.3\text{V}$ , $I_{OUT} = 2.0\text{A}$	$T_A = +25^\circ\text{C}$	-	90	108	
			$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	-	-	135	
$I_{LIMIT}$	Over-Load Current Limit (Note 6)	$V_{IN} = 5\text{V}$ , $V_{OUT} = 4.5\text{V}$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	2.05	2.5	2.85	A
$I_{TRIG}$	Current Limiting Trigger Threshold	Output Current Slew rate (< 100A/s)	-	2.5	-	A	
$I_{SHORT}$	Short-Circuit Current Limit	Enabled into short circuit	1.8	2.75	3.3	A	
$T_{SHORT}$	Short-Circuit Response Time	$V_{OUT} = 0\text{V}$ to $I_{OUT} = I_{LIMIT}$ (OUT shorted to ground)	-	2	-	$\mu\text{s}$	
$V_{IL}$	EN Input Logic Low Voltage	$V_{IN} = 2.7\text{V}$ to $5.5\text{V}$	-	-	0.8	V	
$V_{IH}$	EN Input Logic High Voltage	$V_{IN} = 2.7\text{V}$ to $5.5\text{V}$	2	-	-	V	
$I_{LEAK-EN}$	EN Input Leakage	$V_{IN} = 5\text{V}$ , $V_{EN} = 0\text{V}$ and $5.5\text{V}$	-	0.01	1	$\mu\text{A}$	
$I_{LEAK-O}$	Output Leakage Current	Disabled, $V_{OUT} = 0\text{V}$	-	0.5	1	$\mu\text{A}$	
$T_{D(ON)}$	Output Turn-on Delay Time	$C_L = 1\mu\text{F}$ , $R_{LOAD} = 5\Omega$	-	0.1	-	ms	
$T_R$	Output Turn-on Rise Time	$C_L = 1\mu\text{F}$ , $R_{LOAD} = 5\Omega$	-	0.6	1.5	ms	
$T_{D(OFF)}$	Output Turn-off Delay Time	$C_L = 1\mu\text{F}$ , $R_{LOAD} = 5\Omega$	-	0.1	-	ms	
$T_F$	Output Turn-off Fall Time	$C_L = 1\mu\text{F}$ , $R_{LOAD} = 5\Omega$	-	0.05	0.1	ms	
$R_{FLG}$	FLG Output FET on-Resistance	$I_{FLG} = 10\text{mA}$	-	25	40	$\Omega$	
$I_{FOH}$	FLG Off Current	$V_{FLG} = 5\text{V}$	-	0.01	1	$\mu\text{A}$	
$T_{BLANK}$	FLG Blanking and Latch-off Time	Assertion or deassertion due to overcurrent and over-temperature condition	4	7	15	ms	
$T_{DIS}$	Discharge Time	$C_L = 1\mu\text{F}$ , $V_{IN} = 5\text{V}$ , disabled to $V_{OUT} < 0.5\text{V}$	-	0.6	-	ms	
$R_{DIS}$	Discharge Resistance (Note 7)	$V_{IN} = 5\text{V}$ , disabled, $I_{OUT} = 1\text{mA}$	-	105	-	$\Omega$	
$T_{SHDN}$	Thermal Shutdown Threshold	Enabled	-	140	-	$^\circ\text{C}$	
$T_{HYS}$	Thermal Shutdown Hysteresis	-	-	20	-	$^\circ\text{C}$	
$\theta_{JA}$	Thermal Resistance Junction-to-Ambient	SO-8 (Note 8)	-	96	-	$^\circ\text{C/W}$	
		MSOP-8 (Note 8)	-	130	-	$^\circ\text{C/W}$	
		MSOP-8EP (Note 9)	-	92	-	$^\circ\text{C/W}$	
		U-DFN3030-8 (Note 9)	-	84	-	$^\circ\text{C/W}$	
		U-DFN2020-6 (Note 10)	-	90	-	$^\circ\text{C/W}$	

- Notes:
- Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
  - The discharge function is active when the device is disabled (when enable is de-asserted or during power-up power-down when  $V_{IN} < V_{UVLO}$ ). The discharge function offers a resistive discharge path for the external storage capacitor for limited time.
  - Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad layout.
  - Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.
  - Device mounted on 1"x1" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground.

**Typical Performance Characteristics**

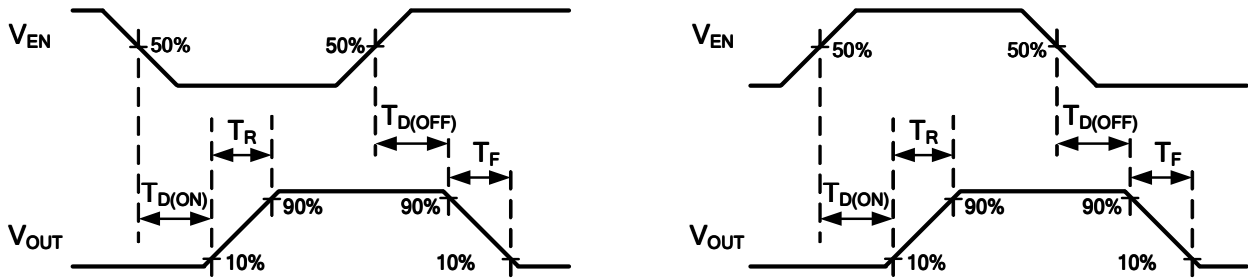
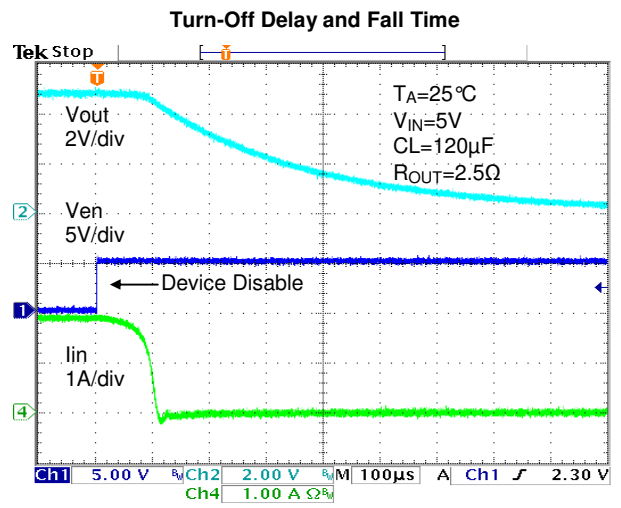
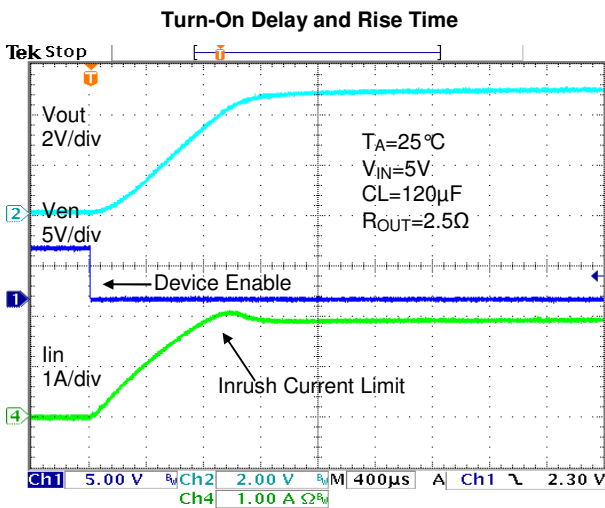
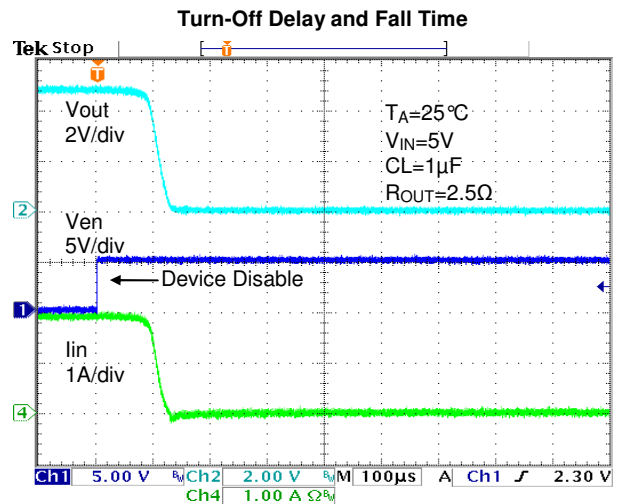
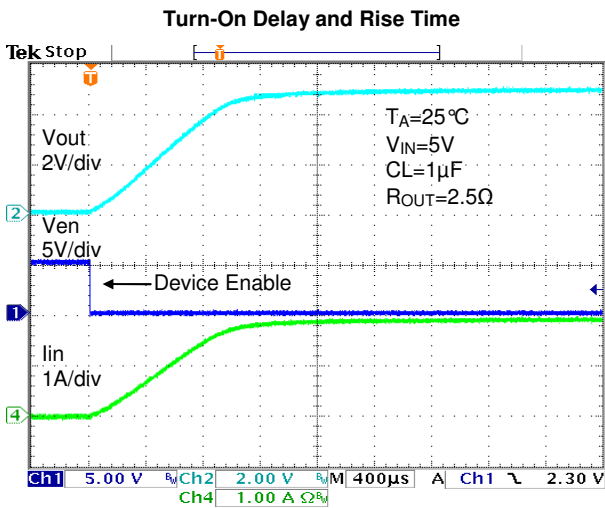


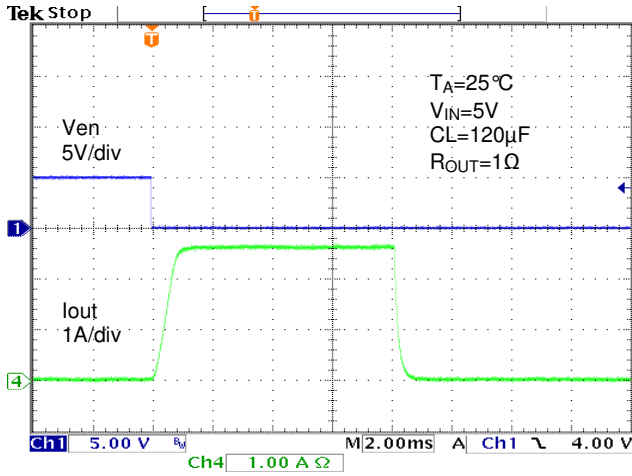
Figure 1 Voltage Waveforms: AP2401A (left), AP2411A (right)

All Enable Plots are for Enable Active Low

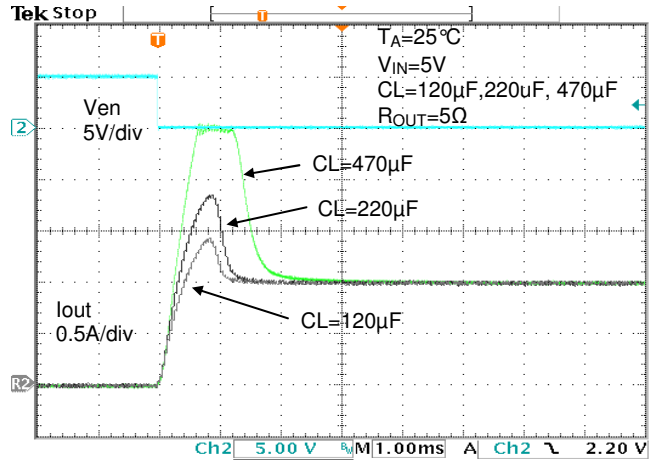


**Typical Performance Characteristics** (continued)

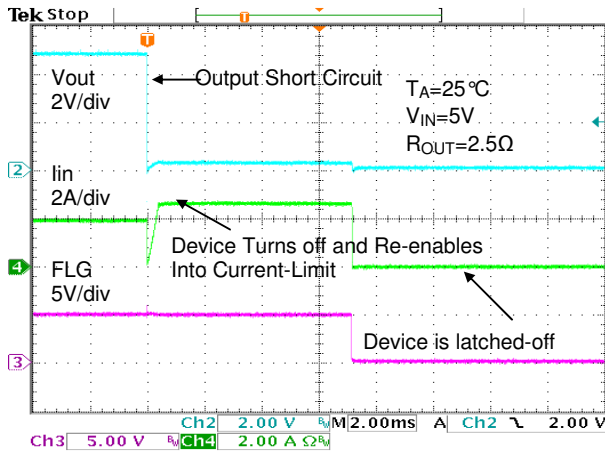
**Device Enabled Into Short-Circuit**



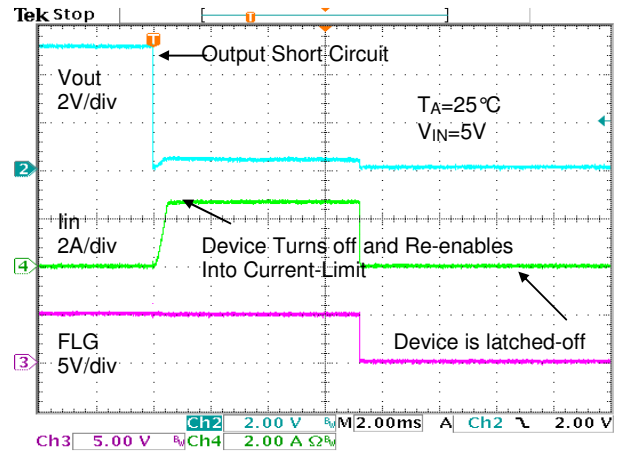
**Inrush Current**



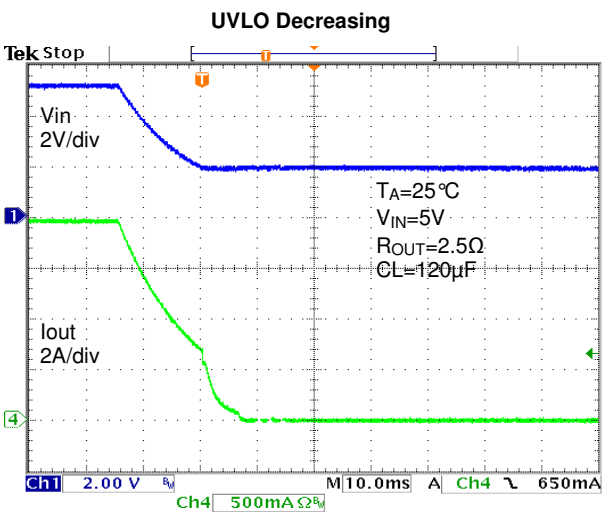
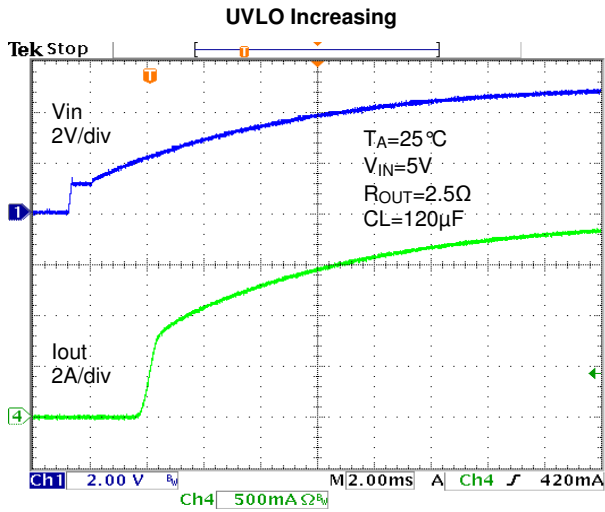
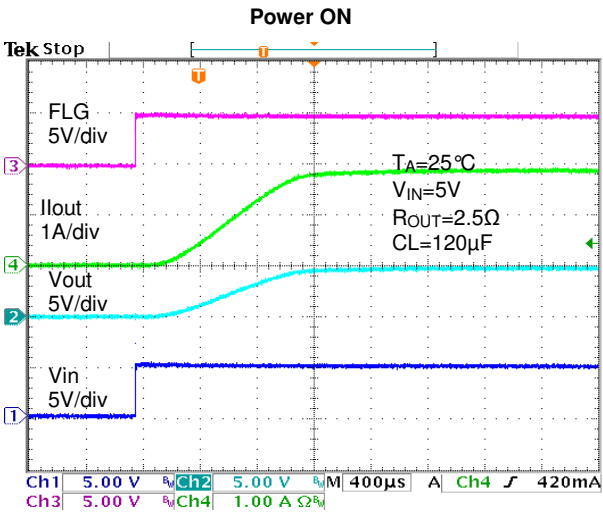
**Full-Load to Short-Circuit Transient Response**



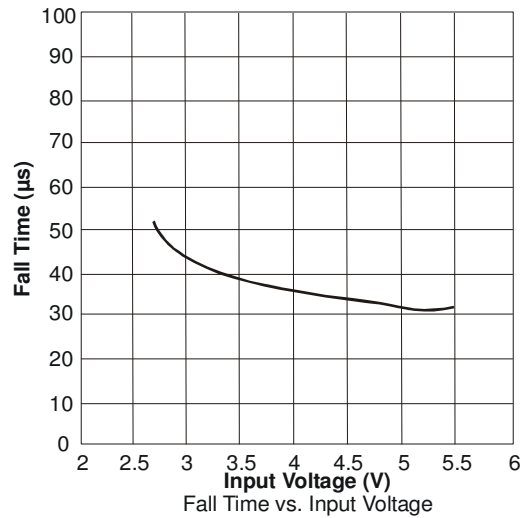
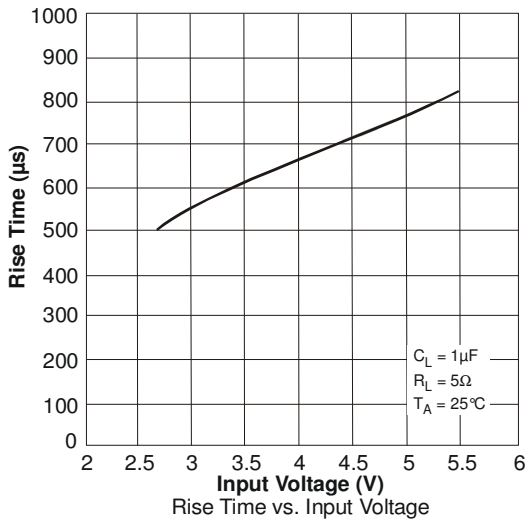
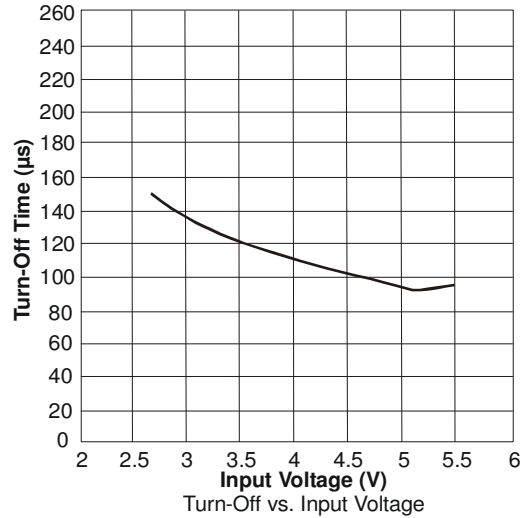
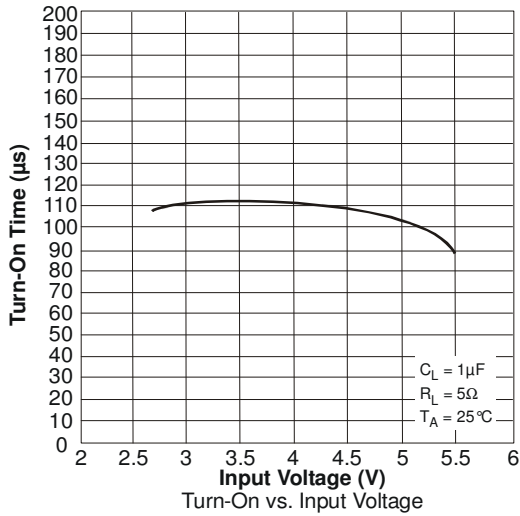
**No-Load to Short-Circuit Transient Response**



**Typical Performance Characteristics (cont.)**

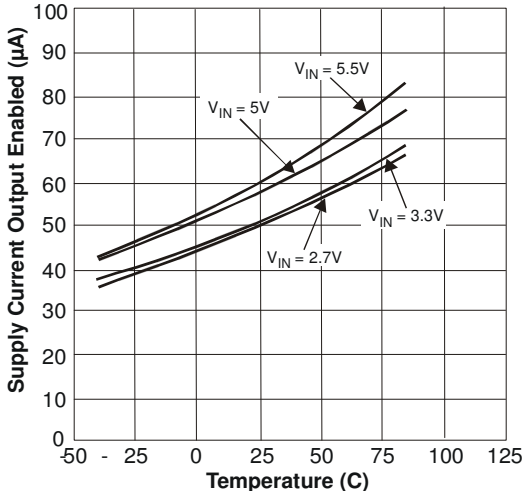


**Typical Performance Characteristics (cont.)**

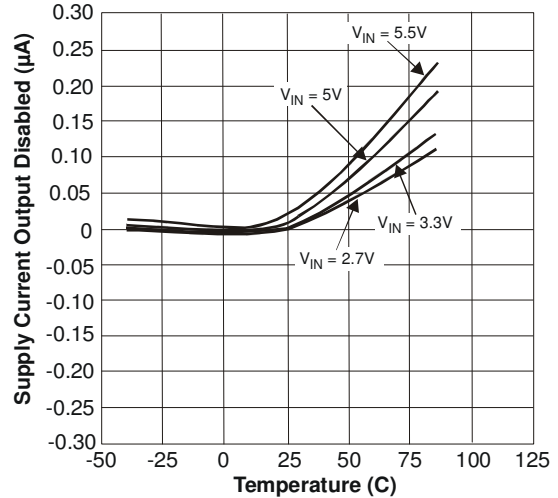




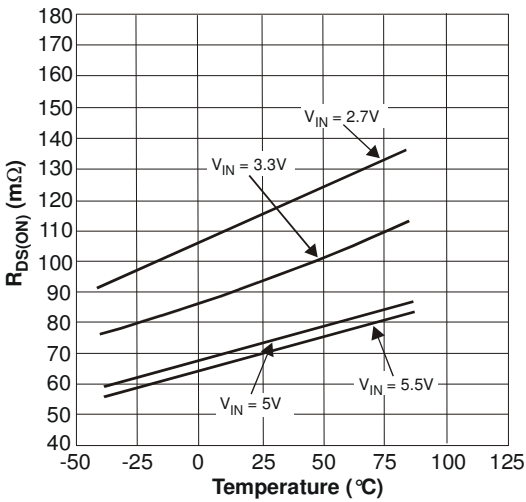
**Typical Performance Characteristics (cont.)**



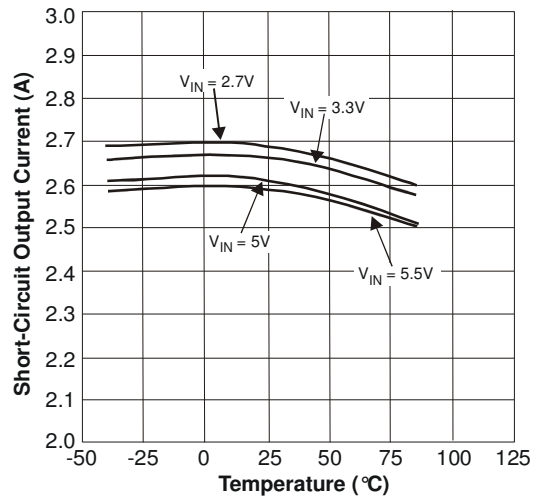
Supply Current, Output Enabled vs. Temperature



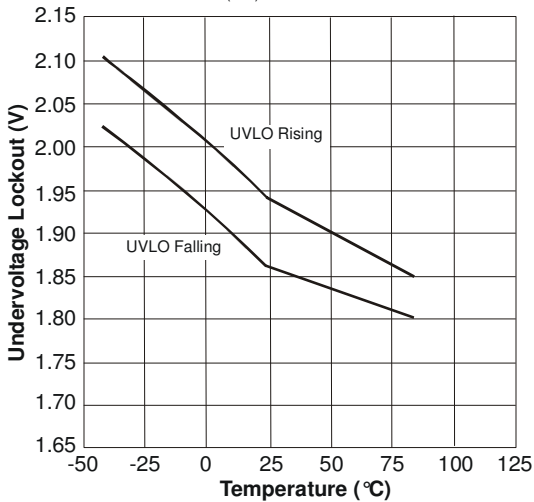
Supply Current, Output Disabled vs. Temperature



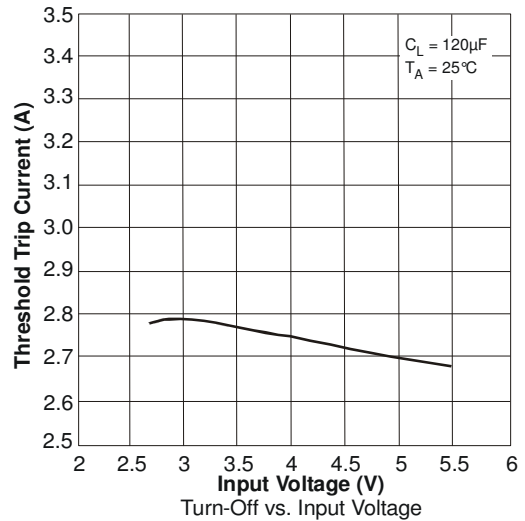
$R_{DS(ON)}$  vs. Temperature



Short-Circuit, Output Current vs. Temperature



Undervoltage Lockout vs. Temperature



Turn-Off vs. Input Voltage

## Application Information

### Power Supply Considerations

A 0.1µF to 2.2µF X7R or X5R ceramic bypass capacitor placed between IN and GND, close to the device, is recommended. When an external power supply is used, or an additional ferrite bead is added to the input, high inrush current may cause voltage spikes higher than the device maximum input rating during short circuit condition. In this case a 2.2µF or bigger capacitor is recommended. Placing a high-value electrolytic capacitor on the input and output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.1µF to 1.0µF ceramic capacitor improves the immunity of the device to short-circuit transients.

### Overcurrent and Short Circuit Protection

An internal sensing FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the devices will limit the current until the overload condition is removed or the internal deglitch time (7ms typical) is reached and the device is turned off. The device will remain latched off even the overload condition is removed until power is cycled or the device enable is toggled.

Three possible overload conditions can occur. In the first condition, the output has been shorted to GND before the device is enabled or before VIN has been applied. The AP2401A/AP2411A senses the short circuit and immediately clamps output current to a certain safe level namely  $I_{LIMIT}$ , and turns off after deglitch time (7ms typical).

In the second condition, an output short or an overload occurs while the device is enabled. At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. After the current limit function has tripped (reached the overcurrent trip threshold), the device switches into current limiting mode and the current is clamped at  $I_{LIMIT}$  current for deglitch time period (7ms typical), and then turned off.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold ( $I_{TRIP}$ ) is reached or until the thermal limit of the device is exceeded. The AP2401A/AP2411A is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its current limiting mode and output current is clamped at  $I_{LIMIT}$  for deglitch time period (7ms typical), and then turned off.

### FLG Response

When an overcurrent or over-temperature shutdown condition is encountered, the FLG open-drain output goes active low after a nominal 7ms deglitch timeout.

When that happens, the FLG will remain low and the switch will be latched off until the fault condition is removed. Connecting a heavy capacitive load to the output of the device can cause a momentary overcurrent condition, which does not trigger the FLG due to the 7ms deglitch timeout. The AP2401A/AP2411A is designed to eliminate false, overcurrent reporting without the need of external components to remove unwanted pulses.

### Power Dissipation and Junction Temperature

The low, on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature ( $T_A$ ) and  $R_{DS(ON)}$ , the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

$T_A$  = Ambient Temperature °C

$R_{\theta JA}$  = Thermal Resistance

$P_D$  = Total Power Dissipation

### Thermal Protection

Thermal protection prevents the IC from damage when heavy-overload or short-circuit faults are present for extended periods of time. The AP2401A/AP2411A implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately 140°C due to excessive power dissipation in an overcurrent condition, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit allowing the device to cool down approximately 25°C before the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The FLG open-drain output is asserted when an over-temperature shutdown occurs with 7ms deglitch.

When the FLG is asserted, the switch will be latched off until the temperature drops to 20°C below the thermal shutdown threshold and the power or EN pin is cycled.

**Application Information** (continued)

**Undervoltage Lockout (UVLO)**

Undervoltage lockout function (UVLO) keeps the internal power switch from being turned on until the power supply has reached at least 2V, even if the switch is enabled. Whenever the input voltage falls below approximately 2V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

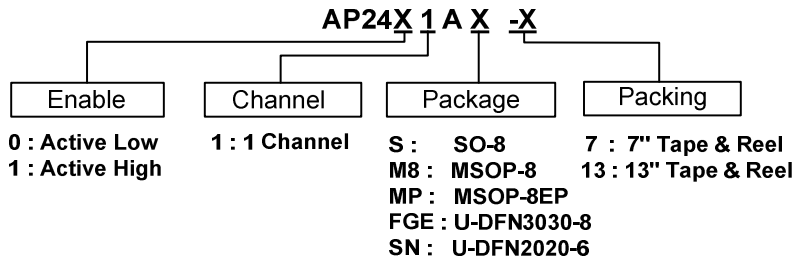
**Discharge Function**

The discharge function of the device is active when enable is disabled or de-asserted. The discharge function with the N-MOS power switch implementation is activated and offers a resistive discharge path for the external storage capacitor. This is designed for discharging any residue of the output voltage when either no external output resistance or load resistance is present at the output.

**Dual-Purpose Port Applications**

AP2401A/AP2411A is suitable for use in dual-purpose port applications in which a single port is used for data communication between the host and peripheral devices while simultaneously maintaining a charge to the battery of the peripheral device. An example of this is a shared HDMI/MHL (Mobile High-definition Link) port that allows streaming video between an HDTV or set-top box and a smartphone or tablet while maintaining a charge to the smartphone or tablet battery. In such dual-purpose port applications, it is important to insure Vin of the AP2401A/AP2411A is ramped to its operating voltage prior to enabling the output. Since the AP2401A/AP2411A includes an embedded discharge feature that discharges the output load of the device when the device is disabled, the batteries of the connected peripheral device will be subject to continual discharge whenever the AP2401A/AP2411A is disabled. An overstress condition to the device's discharge MOS transistor may result.

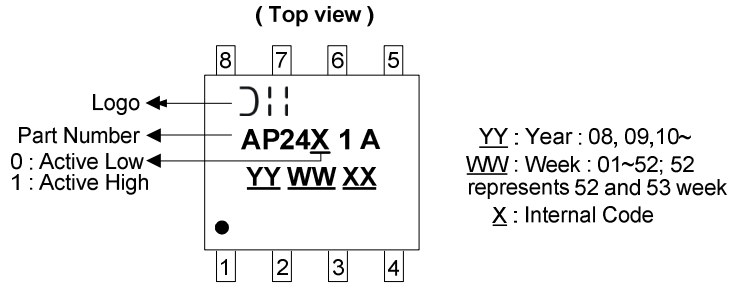
**Ordering Information**



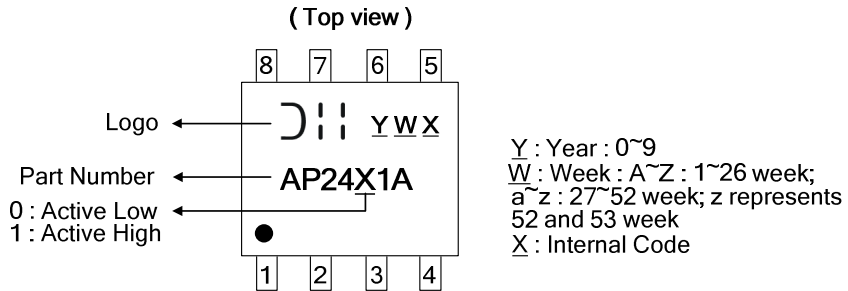
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				Quantity	Part Number Suffix
AP24X1AS-13	New Product	S	SO-8	2,500/Tape & Reel	-13
AP24X1AM8-13	New Product	M8	MSOP-8	2,500/Tape & Reel	-13
AP24X1AMP-13	New Product	MP	MSOP-8EP	2,500/Tape & Reel	-13
AP24X1AFGE-7	New Product	FGE	U-DFN3030-8	3,000/Tape & Reel	-7
AP24X1ASN-7	Preview	SN	U-DFN2020-6	3,000/Tape & Reel	-7

**Marking Information**

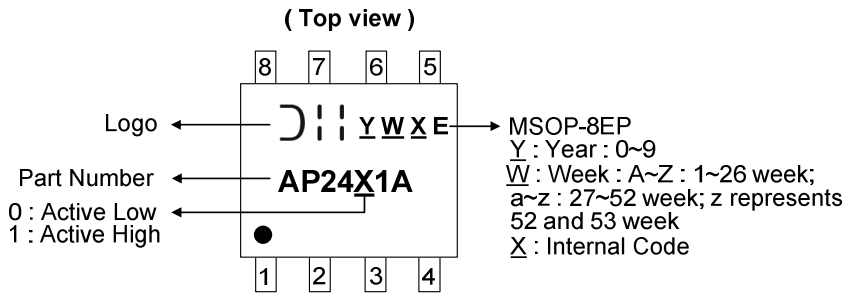
(1) SO-8



(2) MSOP-8



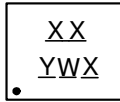
(3) MSOP-8EP



**Marking Information** (continued)

(4) U-DFN3030-8

( Top View )

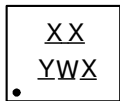


XX : Identification Code  
Y : Year : 0~9  
W : Week : A~Z : 1~26 week;  
a~z : 27~52 week; z represents  
52 and 53 week  
X : A~Z : Internal Code

Part Number	Package	Identification Code
AP2401AFGE-7	U-DFN3030-8	4W
AP2411AFGE-7	U-DFN3030-8	4X

(5) U-DFN2020-6

( Top View )



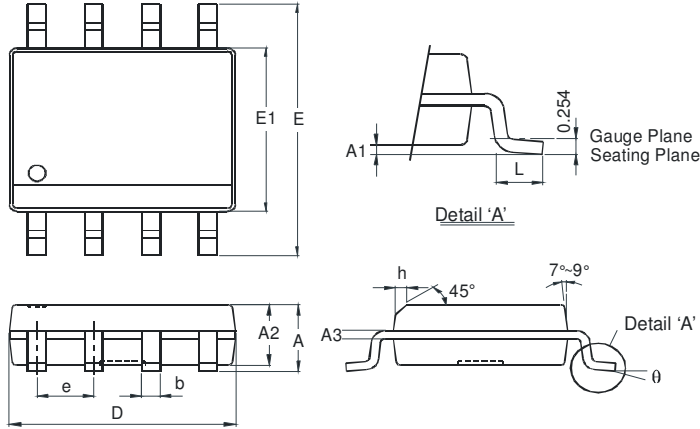
XX : Identification Code  
Y : Year : 0~9  
W : Week : A~Z : 1~26 week;  
a~z : 27~52 week; z represents  
52 and 53 week  
X : A~Z : Internal Code

Part Number	Package	Identification Code
AP2401ASN-7	U-DFN2020-6	4Y
AP2411ASN-7	U-DFN2020-6	4Z

**Package Outline Dimensions** (All dimensions in mm.)

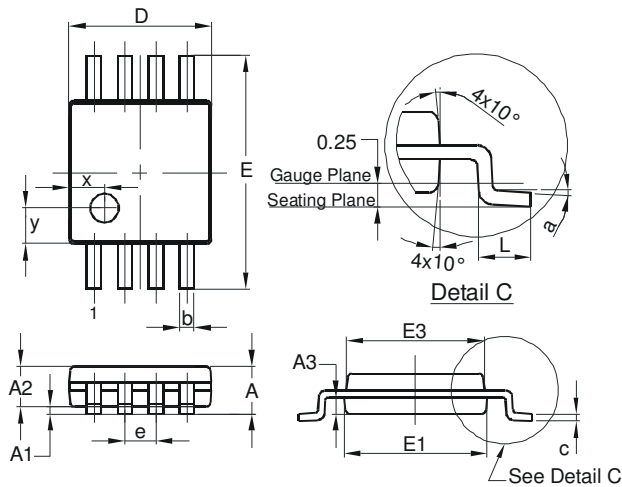
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

**1. Package type: SO-8**



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

**2. Package type: MSOP-8**

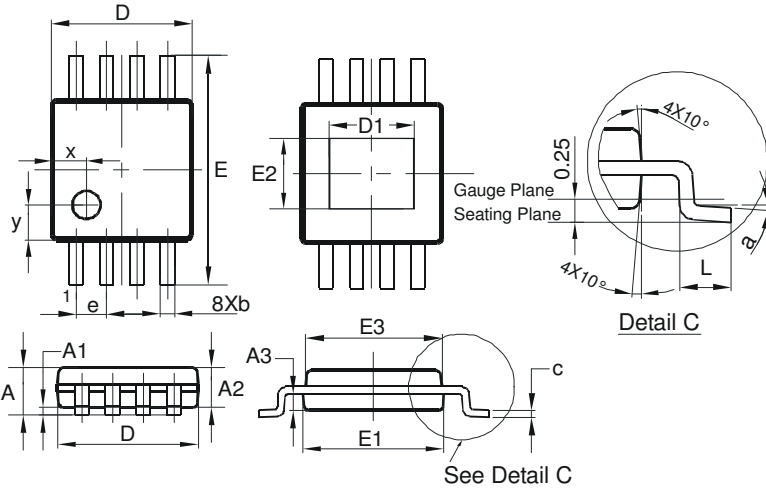


MSOP-8			
Dim	Min	Max	Typ
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

**Package Outline Dimensions** (cont.) (All dimensions in mm.)

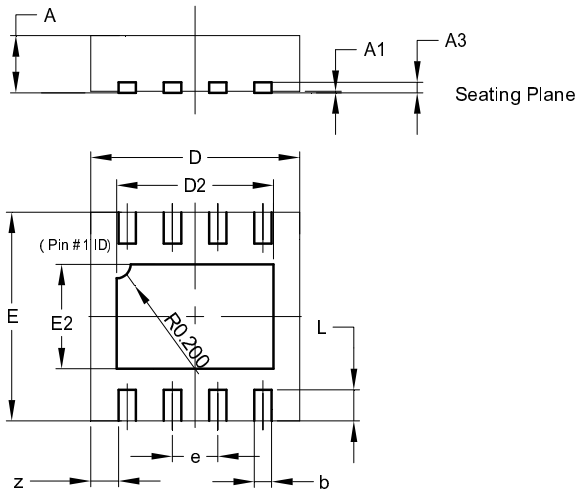
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

**3. Package type: MSOP-8EP**



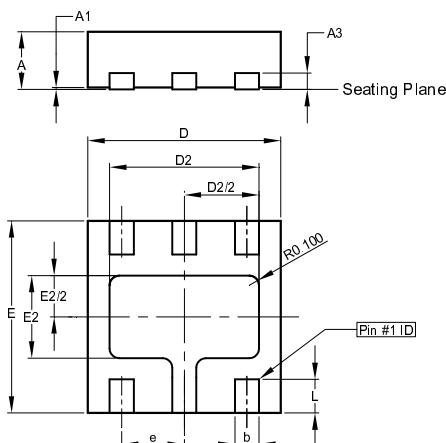
MSOP-8EP			
Dim	Min	Max	Typ
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
D1	1.60	2.00	1.80
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E2	1.30	1.70	1.50
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

**4. Package type: U-DFN3030-8 Type E**



U-DFN3030-8 (TYPE E)			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0.00	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	2.95	3.05	3.00
D2	2.15	2.35	2.25
E	2.95	3.05	3.00
E2	1.40	1.60	1.50
e	-	-	0.65
L	0.30	0.60	0.45
z	-	-	0.40
All Dimensions in mm			

**5. Package type: U-DFN2020-6**

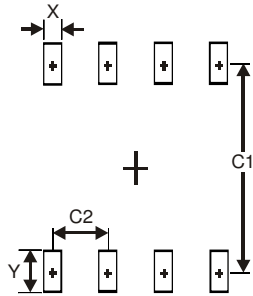


U-DFN2020-6			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0	0.05	0.03
A3	—	—	0.15
b	0.20	0.30	0.25
D	1.95	2.075	2.00
D2	1.45	1.65	1.55
e	—	—	0.65
E	1.95	2.075	2.00
E2	0.76	0.96	0.86
L	0.30	0.40	0.35
All Dimensions in mm			

## Suggested Pad Layout

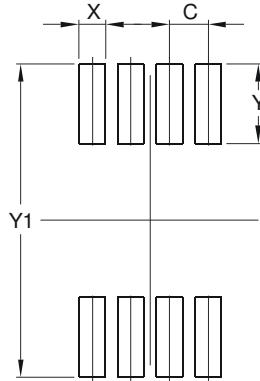
Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

(1) Package type: SO-8



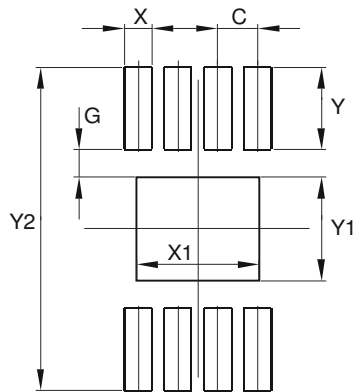
Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

(2) Package type: MSOP-8



Dimensions	Value (in mm)
C	0.650
X	0.450
Y	1.350
Y1	5.300

(3) Package type: MSOP-8EP



Dimensions	Value (in mm)
C	0.650
G	0.450
X	0.450
X1	2.000
Y	1.350
Y1	1.700
Y2	5.300





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