Description

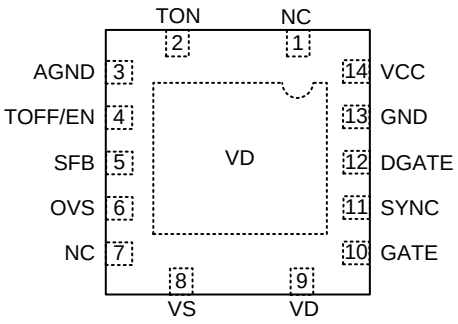
The AR2003FV is Active/Synchronous Rectification Controller, providing output voltage from 4.5V to 21V. Using internal drain-to-source voltage sensing, the AR2003FV is ideal for Fly-back, LLC-resonant and other power supply architectures. It has SFB pin that can eliminate the external feedback resistor when target output voltage is 5V or 12V.

The small footprint of the AR2003FV makes it ideal for space constrained applications.

Intelligent features of this IC are the Minimum Off Time (TOFF) and Minimum on Time (TON), these features blank the noise generated during the turn on and turn off instances of the power FET. Light load detection for improved efficiency at light and no load is implemented. Other features include Under Voltage Lock Out (UVLO), SYNC feature for CCM operation and low turn off threshold voltage for improved efficiency.

Pin Assignments

(Top View)



V-DFN3535-14

Features

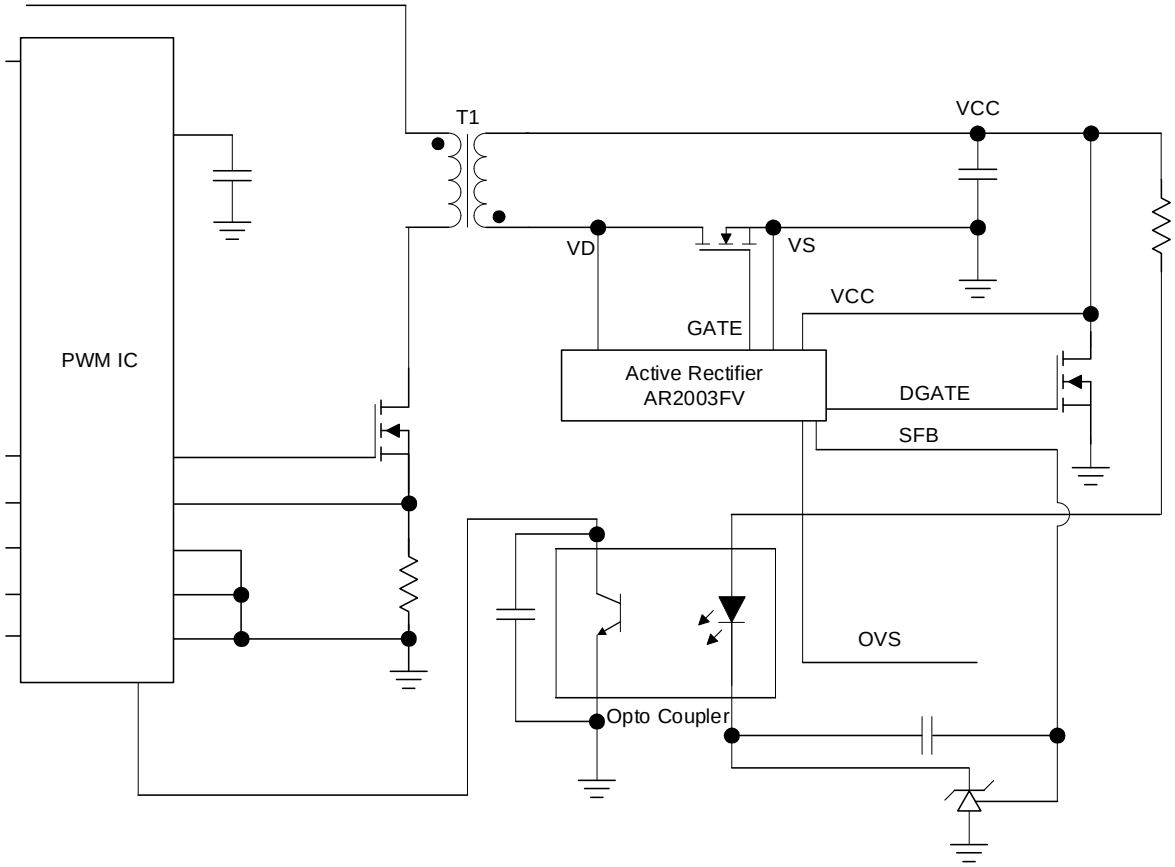
- Primary-Side or Secondary-side Active/Synchronous Rectification, Optimized for Systems with Dynamic Voltage Scaling Capabilities
- Frequency of Operation up to 600kHz
- Suitable for Discontinuous (DCM), Continuous (CCM) and Critical (CrCM) Conduction Mode
- Minimum On-time and Off-time to Blanking Turn-on/off Oscillations
- Light Load Detection and Sleep Mode
- Drain Voltage Rating of 200V
- Recommended Operating Voltage from 4.5V up to 21V
- Low Component Count.
- Low Under Voltage Lockout
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

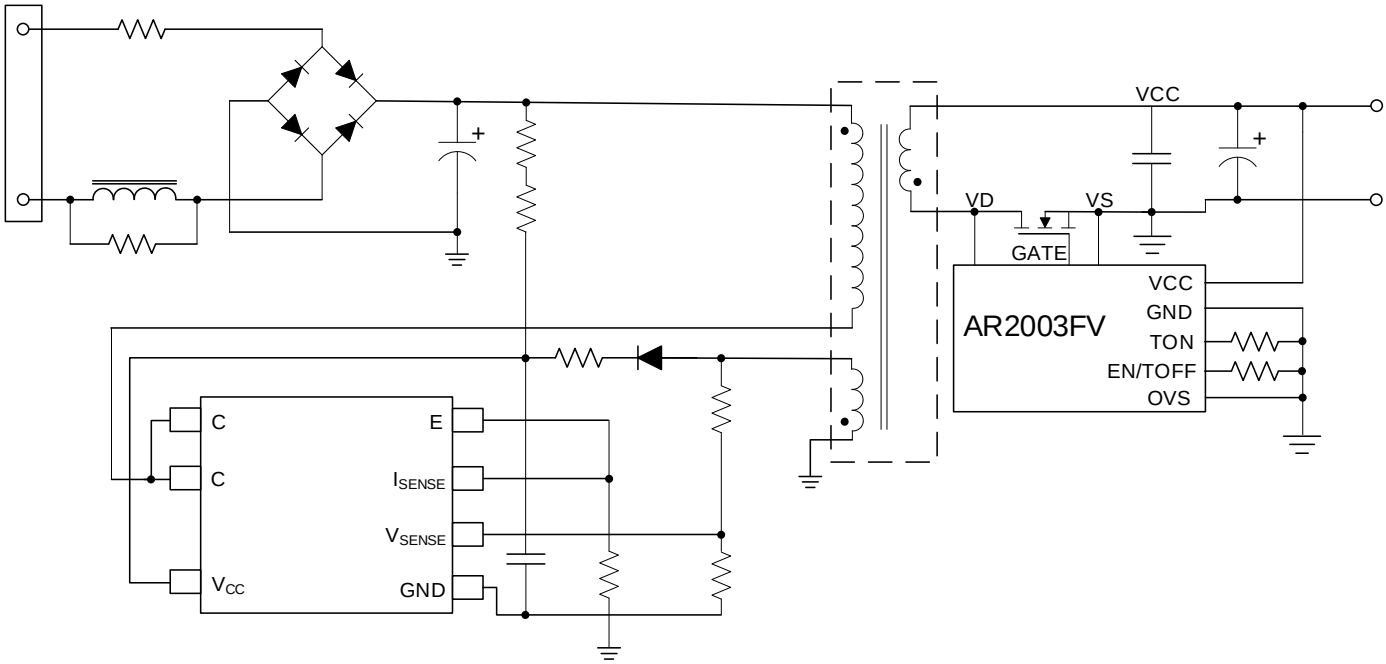
- USB PD Adaptor
- AC-DC Battery Charger
- Fly-back Conversion
- PC Power Supply
- SMPS
- Power Adaptors
- Auxiliary Power Supplies
- PoE Power Devices

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



Secondary-side Synchronous Rectification

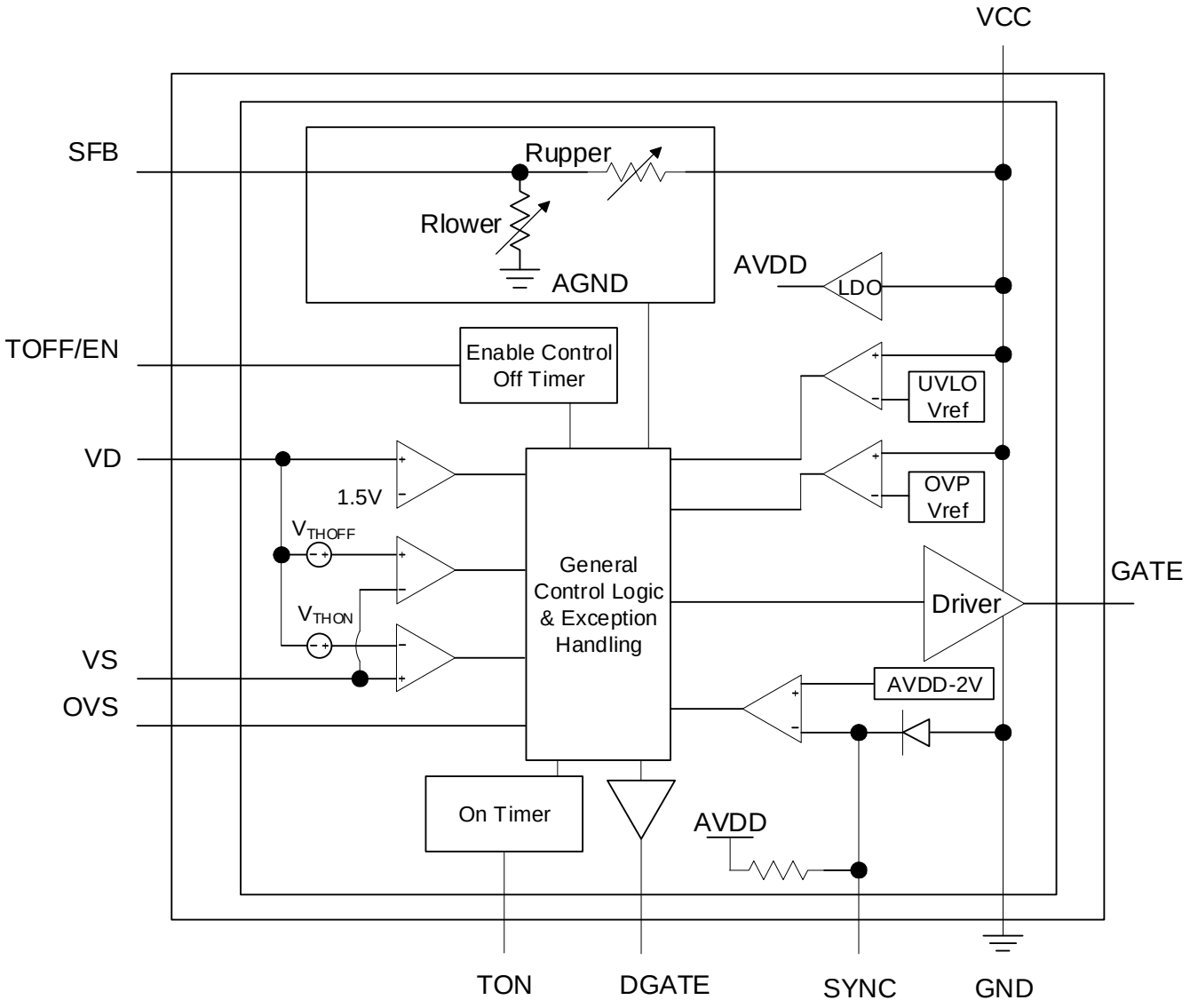


Primary-side Synchronous Rectification

Pin Descriptions

Pin Number	Pin Name	Function
1, 7	NC	Not Connected
2	TON	Minimum On-time Setting Pin
3	AGND	This is the ground reference for all internal comparators and thresholds.
4	TOFF/EN	Enable Pin/ Minimum Off-time This pin combines the functions of setting the programmable minimum off-time as well as acting as the enable pin. The device enters Under Voltage Lock Out (UVLO) mode when VCC falls below the UVLO threshold. At this point the TOFF/EN pin is internally shorted to ground through a resistor. The internal current source (used for setting TOFF) is powered down. Once the UVLO threshold is exceeded, the internal resistance is removed and the current source is activated. If the voltage applied to the TOFF/EN pin exceeds the VEN_{ON} threshold then the device is in Active Mode. If the voltage drops below the VEN_{OFF} threshold then the device is in Sleep Mode.
5	SFB	Output pin of internal feedback resistor which is connected to VCC. It is sent to TL431 (or its compatible) to drive the opto-coupler and provide feedback voltage to primary side controller to realize Secondary Synchronous Rectification.
6	OVS	Output voltage (VCC) select pin, work together with SFB to select output voltage in 5V or 12V.
8	VS	This is the connection to internal MOSFET Source. VS is also connected to GND.
9, VD pad	VD	This is a connection to the internal MOSFET Drain. The pin needs to be connected as closely as possible to the transformer used in the application, to minimize the effects of parasitic inductance on the performance of the device. The device requires that VD has a voltage greater than 1.5V and that the T_{OFF} timer has expired before the MOSFET is able to be activated. Once these conditions are met and the voltage internally sensed on the VD pin is 150mV lower than the VS pin, the internal MOSFET is turned on and the T_{ON} minimum on time period is started. The MOSFET will remain on for at least the length of the minimum on time. The only thing that can override this is if a pulse is detected on the SNYC pin. After the TON period, the MOSFET remains on until the VD to VS voltage has reached to the V_{THOFF} threshold, at which point the internal MOSFET is turned off. As mentioned before, if the V_{THOFF} threshold is reached before the TON period has expired, the device will enter the Light Load Mode. Under this mode, the MOSFET will not be turned on the next switching cycle. When the drain voltage has increased to 1.5V, the TOFF timer is triggered, during which the MOSFET is prevented from turning on.
10	GATE	Connect GATE to the gate of the controlled MOSFET through a small series resistor using short PC board tracks to achieve optimal switching performance. The GATE output can achieve >2-A peak source current when High and >4-A peak sink current when Low into a large N-channel power MOSFET.
11	SYNC	If a falling edge is sensed on this pin, the internal MOSFET is immediately turned off, irrespective of the sensed drain to source voltage or the state of the TON timer. This characteristic allows the device to be easily used in a Continuous Conduction Mode (CCM) system. The SYNC pin needs to be connected to a suitable control signal on the primary side of the convertor, using a high voltage isolation cap, transformer or other suitable means.
12	DGATE	During Over Voltage Protection, DGATE will drive external MOSFET to pull down the output voltage so that Primary side controller will start the Short Circuit Protection handling.
13	GND	This is the reference potential for all internal comparators and thresholds.
14	VCC	VCC supplies all the internal circuitry of the device. A DC supply is required to be connected to this pin. It is required that a 10µF or larger capacitor is placed between this pin and GND, as close to the pins as possible. The device will not function until the V_{CC} has risen above the UVLO threshold. The device can safely be turned off by bringing V_{CC} below the UVLO threshold (minus the UVLO threshold hysteresis). If V_{CC} drops below the UVLO threshold (minus UVLO threshold hysteresis), the MOSFET is turned off and the TOFF/EN pin is internally connected to GND.

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
VCC	Input Voltage Range VCC	-0.3 to 24	V
VD	Input Voltage Range VD	-1 to 200	V
VS	Input Voltage Range VS	-1 to 1	V
TOFF/EN, TON, OVS, SYNC	Input Voltage Range Other	-0.3 to 6	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_L	Lead Temperature	+ 260	°C
T_{ST}	Storage Temperature	-65 to +150	°C
ESD	Human Body Model, JESD22-A114	2	kV
	Charged Device Model, JESD22-C101	0.5	

Note 4: These are stress ratings only. Operation outside the absolute maximum ratings may cause device failure. Operation at the absolute maximum rating for extended periods may reduce device reliability.

Package Thermal Data (@T_A = +25°C, unless otherwise specified)

Symbol	Parameter	Rating	Unit
P_D	Power Dissipation (Note 5)	0.67	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Air (Note 6)	36	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 7)	21	°C/W

Notes: 5. Device mounted on FR-4 PCB, 2oz with minimum recommended pad layout.
6. Device mounted on 25mm x 25mm 2oz copper board.
7. Device mounted on 50mm x 50mm 2oz copper board.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage Range	4.5	21	V
V_{DS}	Voltage Cross Drain and Source	-1	200	
f_{SW}	Switching Frequency	20	600	kHz
T_J	Operating Junction Temperature Range	-40	+125	°C
R_{TOFF}	TOFF Resistor Value	85	200	kΩ
R_{TON}	TON Resistor Value	8.25	100	kΩ
C_{VCC}	VCC Bypass Capacitor	10	–	µF
TW_{sync}	Sync Pulse Width	20	–	nS

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVDD}	Internal Regulator Output	V_{CC} = 5.5V	–	4.5	–	V
		V_{CC} = 12V	–	4.7	–	V
ICC_{START}	Supply Current (Under Voltage)	V_{CC} = 2.6V	–	160	220	µA
$ICC_{STANDBY}$	Supply Current (Disabled)	V_{CC} = 5.5V, $R_{EN/OFF}$ = 0Ω	–	380	500	
		V_{CC} = 12V, $R_{EN/OFF}$ = 0Ω	–	450	600	
ICC_{ON}	Supply Current (Enabled)	V_{CC} = 5.5V, $R_{EN/OFF}$ = 100kΩ, Cgate=0.	–	1.5	2	mA
		V_{CC} = 12V, $R_{EN/OFF}$ = 100kΩ, Cgate=0.	–	1.8	2.5	
		V_{CC} = 5.5V, fsw=100kHz, Cgate=3300pf	–	3.2	4.2	
		V_{CC} = 12V, fsw=100kHz, Cgate=3300pf	–	5	7	
V_{EN-ON}	TOFF/EN Turn-on Threshold, Rising	TOFF/EN driven, V_{TON} > 0.6V	1.31	1.4	1.49	V
V_{EN-OFF}	TOFF/EN Turn-off Threshold, Falling	TOFF/EN driven, V_{TON} < 0.2V	0.55	0.6	0.65	
$I_{EN-START}$	TOFF/EN Input Current, Disabled	R_{TOFF}=50K	-21.5	-20	-18.5	µA
I_{EN-ON}	TOFF/EN Input Current, Enabled	R_{TOFF}=100K	-10.7	-10	-9.3	
Under-Voltage Lockout (UVLO)						
$UVLO_{TH}$	VCC Under Voltage Lockout Threshold Rising	–	2.8	3.0	3.20	V
$UVLO_{HYS}$	VCC Under Voltage Lockout Threshold Hysteresis	–	–	200	–	mV
MOSFET Voltage Sensing						
V_{THARM}	Gate Re-arming Threshold	V_D to GND, Rising	1.3	1.5	1.7	V
V_{THON}	Gate Turn-on Threshold	(V_D-V_S) falling, V_S = 0V	-220	-150	-80	mV
$V_{THOFF\ HV}$	Gate Turn-off Threshold	(V_D-V_S) rising, V_S = 0V, V_{CC} ≥ 4.2V	-6	-4	-2	mV
$V_{THOFF\ LV}$	Gate Turn-off Threshold	V_D-V_S) rising, V_S = 0V, V_{CC} < 4.2V	-30	-20	-10	
TD_{ON}	Gate Turn-on Propagation Delay	From V_{THON} to Gate > 1V	–	30	50	ns
TD_{OFF}	Gate Turn Off Propagation Delay	From V_{THOFF} to Gate < 4V	–	30	60	ns
Minimum On Time						
T_{ON-LR}	Minimum On Time at Low Resistance	R_{TON} = 8.25KΩ	0.26	0.34	0.42	µs
T_{ON-HR}	Minimum On Time at High Resistance	R_{TON} = 100KΩ	2.25	3	3.75	µs
Minimum Off Time						
T_{OFF-LR}	Minimum Off Time at Low Resistance	R_{TOFF} = 100KΩ	0.8	1.4	2	µs
T_{OFF-HR}	Minimum Off Time at High Resistance	R_{TOFF} = 200KΩ	7.5	10	12.5	µs
T_{OFF-LV}	Minimum Off Time at Low Voltage	$V_{EN/TOFF}$=1V	0.8	1.4	2	µs
T_{OFF-HV}	Minimum Off Time at High Voltage	$V_{EN/TOFF}$=2V	7.5	10	12.5	µs
T_{OFF-OV}	Minimum Off Time at Over Voltage	2V<$V_{EN/TOFF}$<V_{AVDD}	7.5	10	12.5	µs

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.) (Cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Over Voltage Protection						
V_{OVP0H}	Output Over Voltage High Threshold when OVS = 0	–	–	6	–	V
V_{OVP0L}	Output Over Voltage Low Threshold when OVS = 0	–	–	5.4	–	V
Synchronization						
V_{THSYNC}	SYNC Falling Threshold	Gate Output from High to Low	V_{AVDD}-2.4	V_{AVDD}-2.0	V_{AVDD}-1.6	V
T_{SDLY}	SYNC Propagation Delay (Note 8)	SYNC falling to Gate Falling 10%, 4.5V < V_{CC} < 5.5V	–	40	70	ns
R_{SYNC}	SYNC Pull Up Resistance (Note 8)	Internal Resistance from SYNC to V_{CC}, 4.5V < V_{CC} < 5.5V	1.6	2.0	2.4	KΩ
Gate Driver						
R_{GUP}	Gate Pull up Resistance Enabled	I_{gate}=-100mA	–	2.3	4	Ω
R_{GDN}	Gate Pull Down Resistance Enabled	I_{gate}=100mA	–	1.1	2	
V_{OHG}	Gate Output High Voltage	I_{gate}=-100mA, VCC=5V	4.7	--	–	V
		I_{gate}=100mA, VCC>10V	9.5	--	–	
V_{OLG}	Gate Output Low Voltage	I_{gate}=100mA, VCC=0V	–	--	0.3	
T_{fgate}	Gate Fall Time	4V to 1V, C_{gate} = 3300pf	–	14	30	ns
		10V to 1V, C_{gate}=3300pf	–	20	35	
T_{rgate}	Gate Rise Time	1V to 4V, C_{gate} = 3300pf	–	16	35	
		1V to 10V, C_{gate} = 3300pf	–	25	40	
T_{DIS}	Disable Delay (note 8)	EN falling to Gate falling	–	160	200	
Exception Handling						
T_{over}	Over Temperature	–	–	+150	–	°C
$T_{recover}$	Temperature to Recover from Over Temperature Exception	–	–	+125	–	°C
T_{dgate}	Delay of Turn On Pull Down MOSFET	Cd_{gate}=400pf	–	1.5	–	uS

Note 8: Guaranteed by design.

Typical Performance Characteristics

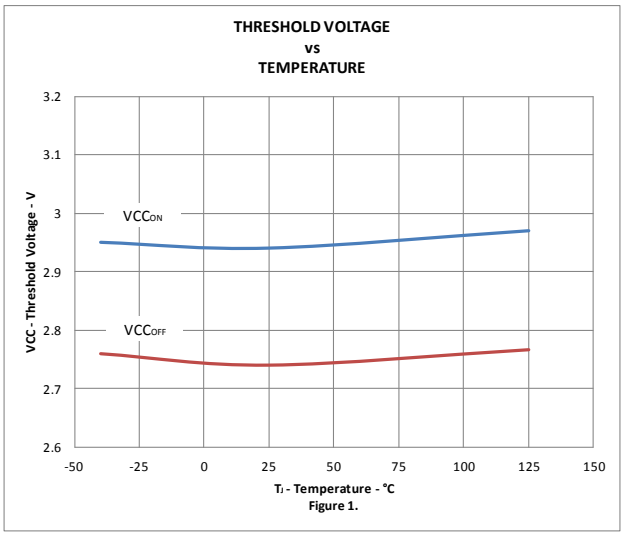


Figure 1.

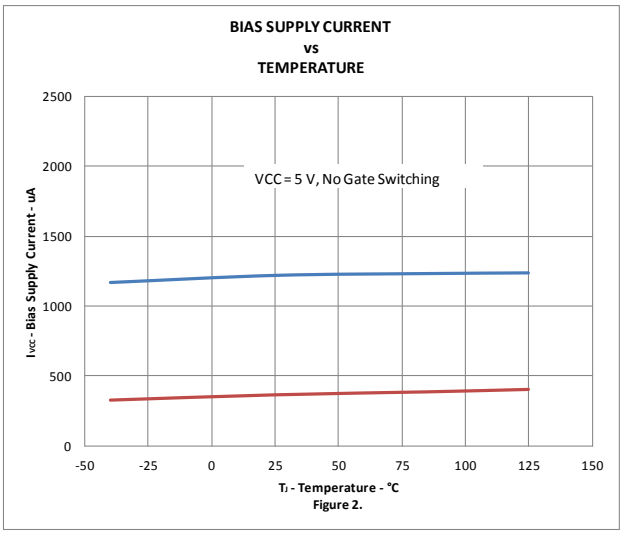


Figure 2.

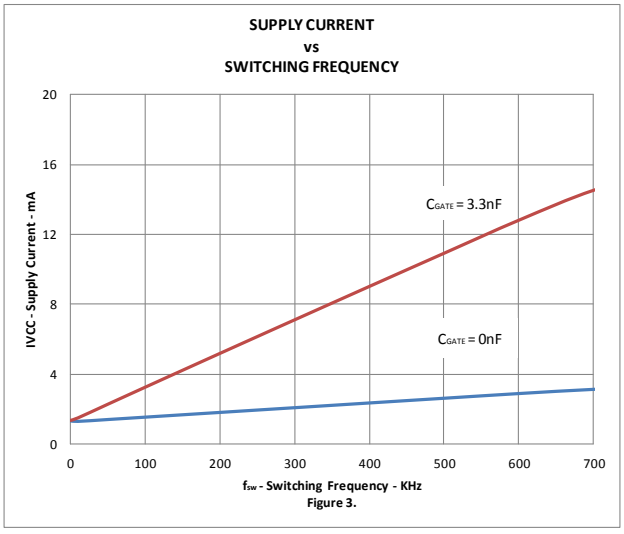


Figure 3.

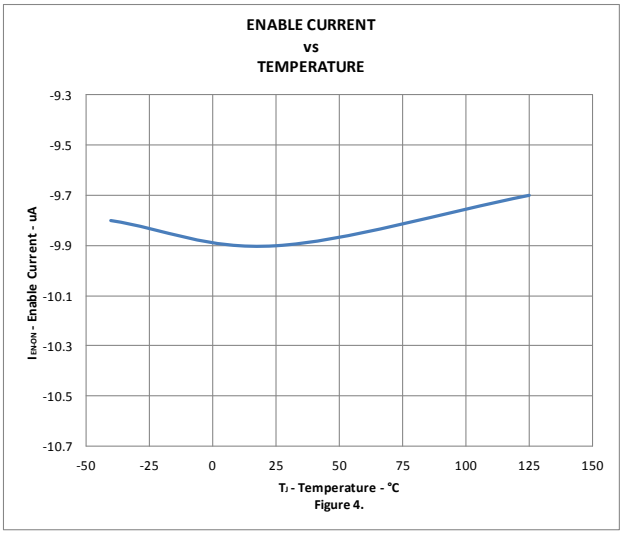


Figure 4.

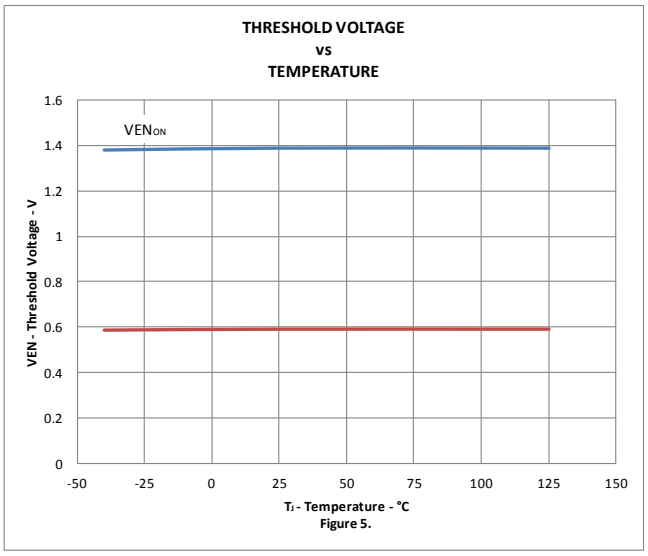
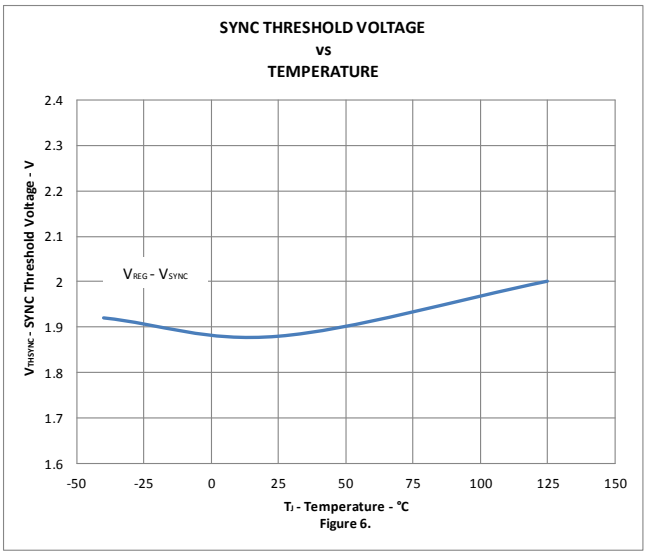


Figure 5.



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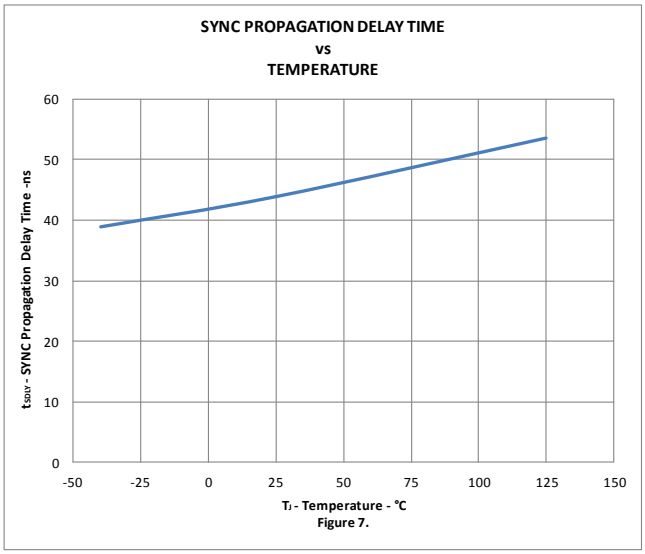

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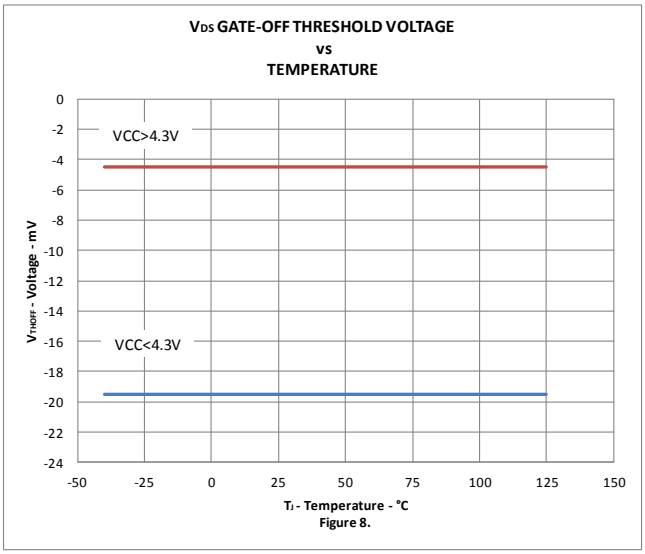

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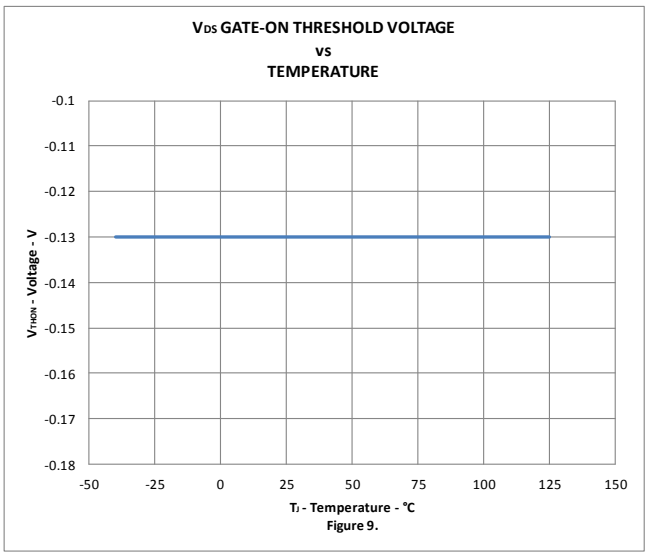

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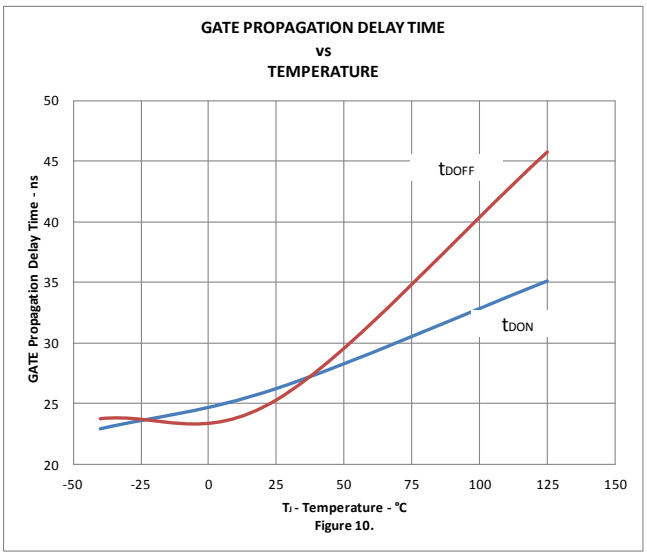

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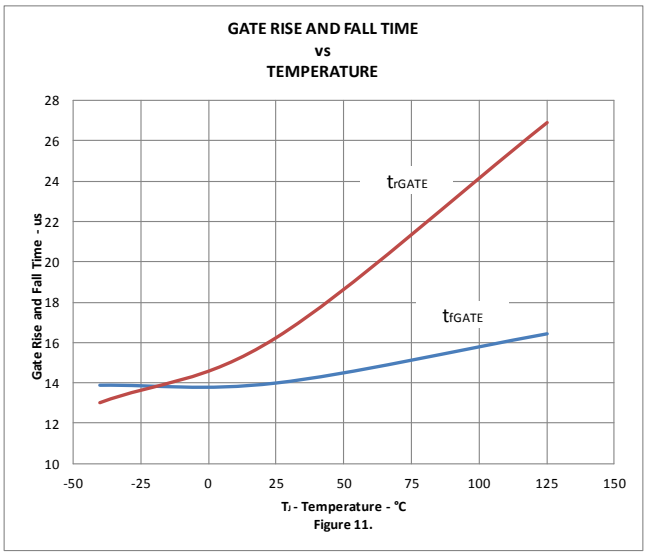


Figure 11.

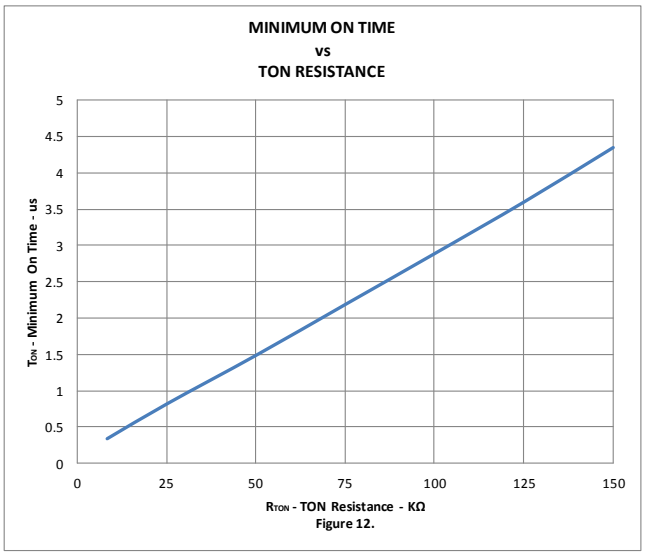


Figure 12.

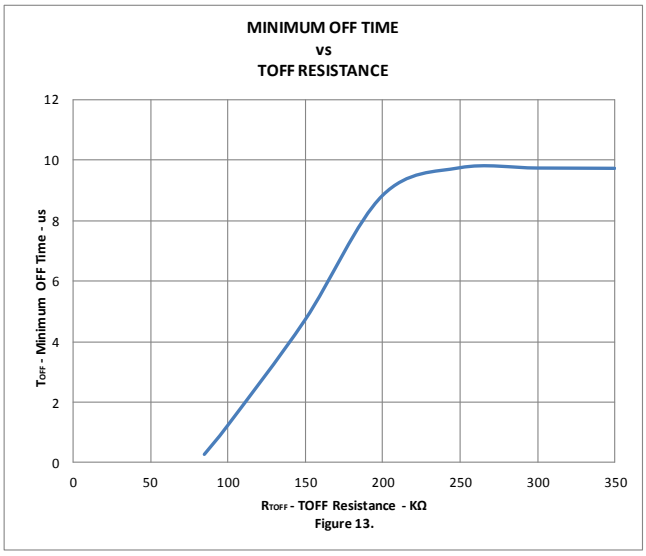


Figure 13.

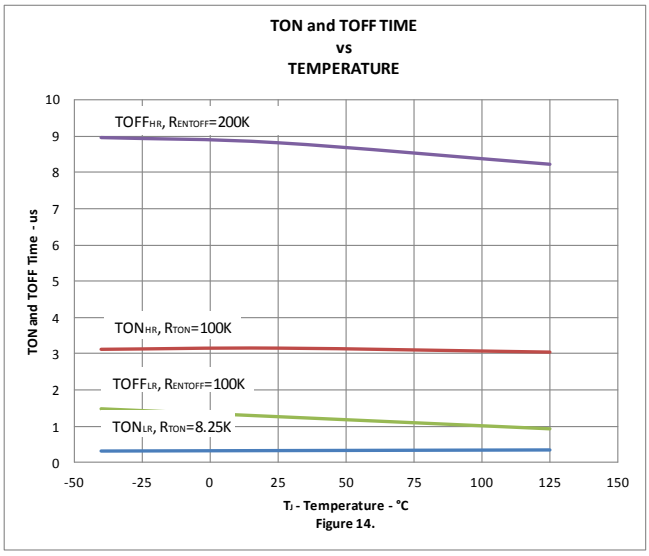


Figure 14.

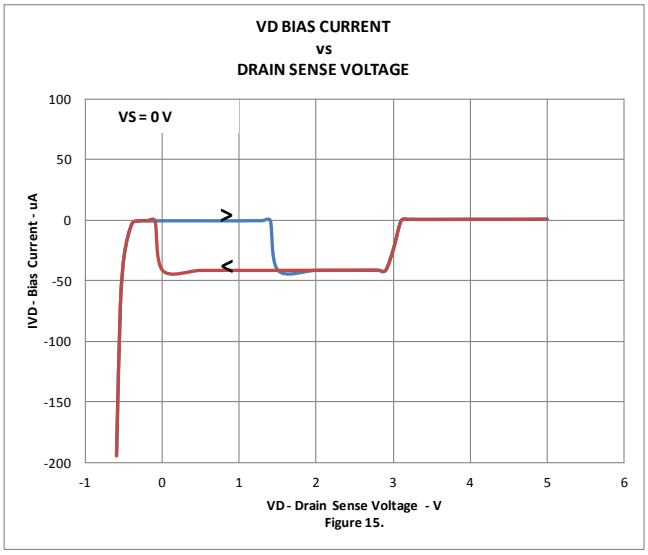


Figure 15.

Modes of Operation

General Description

AR2003FV is an Active/Synchronous Rectifier which can work with many different primary side controllers. AR2003FV can be used in both SSR and PSR systems.

AR2003FV has preset of internal feedback resistor that can reduce external BOM for 5V or 12V system.

UVLO MODE

When VCC does not reach $UVLO_{TH}$, or falls blow $UVLO_{TH}$ - $UVLO_{HYS}$, AR2003FV will be in UVLO MODE.
In this mode, AR2003FV will turn off external MOSFET, and TOFF/EN pin will internally short to GND. VCC current will be ICC_{START}.

Sleep Mode

Sleep Mode is a low-power operating mode similar to UVLO Mode, except that this mode is entered by forcing V_{EN} below the V_{EN-OFF} threshold via external control. Many internal circuits are turned off to reduce power consumption in this model to reduce device operating losses. External control overrides any internal timing conditions, and immediately forces the GATE output low and enters Sleep Mode. VCC current is reduced to $ICC_{STANDBY}$ level. As V_{EN} is restored to above the V_{EN-ON} threshold, the device exits Sleep Mode into Light-Load Mode after a delay of several µs, allowing re-powered internal circuits to settle.

Active Mode

This is the normal operation mode when inductor current is large enough and synchronous conduction time is longer than T_{ON}. AR MOSFET will be turned on and off according to V_D-V_S, T_{ON} and T_{OFF} setting and SYNC pin.

Light-Load Mode

When Inductor current is small and synchronous conduction time is less than T_{ON}, the AR MOSFET will be kept OFF to reduce switching power loss. Voltage across body diode of AR MOSFET is continuously monitored. When the MOSFET body-diode conduction time is more than T_{ON}, the device will be back to Active mode again.

Over Voltage Protection

Over Voltage mostly likely was an indication of optical coupler short. Therefore, just reporting output error information is not enough. AR2003FV will drive an external FET to create a short situation so that primary side can be set to whole system to restart.

Over Temperature Protection (Only for Secondary-side Synchronous Rectification Application)

When AR2003FV is over heated, AR2003FV will light up the optical coupler to let the primary side deliver very little or no energy so that the whole system will cool down. Hysteresis is set to +25°C.

Usually, V_{CC} might drop blow $UVLO_{TH}$ - $UVLO_{HYS}$ (around 2.8V) due to system load. AR2003FV will enter UVLO mode, and system might restart again. If AR2003FV is over heated again in short time, V_{CC} might be kept around 2.8V. The primary side controller might treat this event as over current or short current, and enters its protection mode.

Over Current Protection

Over Current Protection is not implemented in AR2003FV. Over Current Protection will be carried out in Primary side.

Short Current Protection

Short Current Protection is not implemented in AR2003FV. Short Current Protection handling will be carried out in Primary side.

Application Information

ON Timer Programming

The T_{on} period (minimum on-time) is programmed by adding a resistor from TON pin to ground. In the application, it's likely that when the MOSFET is turned on there will be some ringing generated due to parasitic within the system. The minimum on time will stop the device reacting to this ringing, by blanking out any signal received from the Drain to Source (V_D-V_S) comparator once the device is initially triggered. This will keep the MOSFET turned on for duration of the minimum on-time, irrespective of the V_D-V_S voltage during this period.

If V_D-V_S reaches the gate turn-off threshold within the minimum on-time period, the device will change into Light Load Mode for the next switching cycle. If the load conditions of the system change and the MOSFET turn-off threshold is once again reached once the minimum on-time is over, the device reverts to its nominal mode of operation.

T_{ON} (μs) = 0.028μs * R_{TON} (KΩ) + 0.1μs, 0.24μs < T_{ON} < 4.3μs, 5KΩ < R_{TON} <150KΩ

Enabling and OFF Timer Programming

When V_{CC} < UVLO, TOFF/EN is internally connected to ground through a resistor.

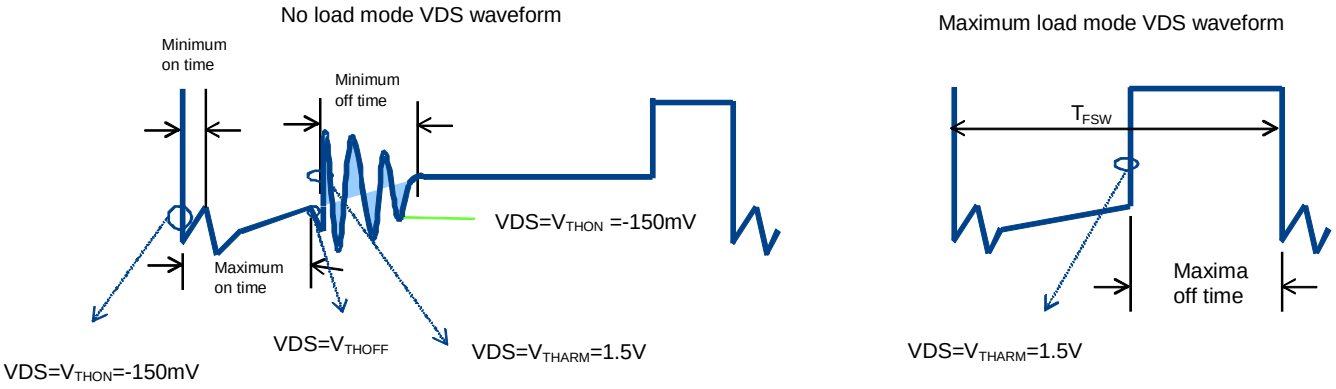
If V_{CC} rises above UVLO, the chip is in the Sleep Mode, a current source will deliver 20μA ($I_{EN-START}$) to TOFF/EN pins. If R_{TOFF} > 70KΩ, $V_{TOFF/EN}$ will over 1.4V (V_{EN-ON}), AR2003FV will enter Active Mode. And the internal current source will switch to deliver 10μA (I_{EN-ON}) to TOFF/EN pin. User can program the minimum off-time by choosing proper value for R_{TOFF}.

T_{OFF} (μs) = 0.083μs* (R_{TOFF} (KΩ)-81KΩ), valid for 85KΩ < R_{TOFF} < 200KΩ

User can also program OFF timer by control the $V_{TOFF/EN}$.

T_{OFF} (μs) = 0.083μs* ($V_{TOFF/EN}$-0.81V), valid for 0.85V < $V_{TOFF/EN}$ < 2V

The minimum off-time is the minimum time; the internal MOSFET will be turned off once V_{THOFF} turn off threshold is reached. This avoids the MOSFET accidentally being retriggered by ringing after turn off.



Minimum On Time	>The time from VDS fall under V_{THON} to VDS ringing voltage < V_{THOFF}	Check with no load waveform
Maximum On Time	< The time from VDS fall under V_{THON} to VDS =V_{THOFF}	Check with no load waveform
Minimum Off Time	> The time from VDS > V_{THARM} to VDS ringing negative voltage higher than V_{THON} after turn off	Check with no load waveform
Maximum Off Time	< The time from VDS=V_{THARM} to VDS drop from VCC level	Check with maximum load waveform

Application Information (Cont.)

SYNC Input Circuit

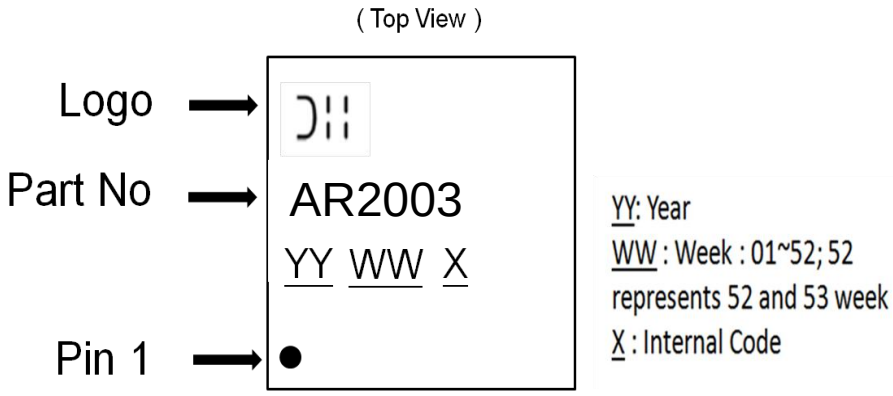
SYNC pin is internally pulled up to internal AVDD (4.2V to 5V) through a 2KΩ resistor. If a falling edge of more than 2V is detected, the external MOSFET will be turned off by AR2003FV. If the amplitude of SYNC signal is larger than 4.2V, an external resistor should be used to limit the input current less than 2mA.

Ordering Information (Note 9)

Part Number	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
AR2003FV-13	AR2003	13	12	3,000

Note 9: For packaging details, go to our website at http://www.diodes.com/products/packages.html.

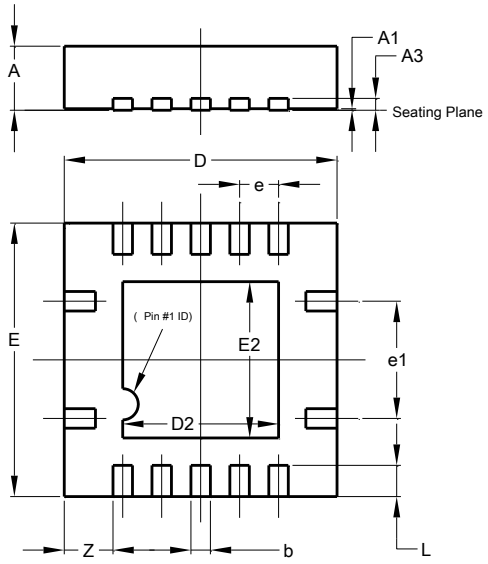
Marking Information



Package Outline Dimensions (All dimensions in mm.)

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.

(1) Package Type: V-DFN3535-14

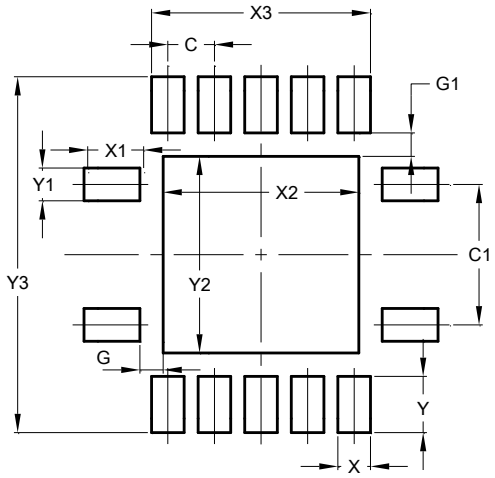


V-DFN3535-14			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	3.45	3.55	3.50
D2	1.90	2.10	2.00
E	3.45	3.55	3.50
E2	1.90	2.10	2.00
e	-	-	0.50
e1	-	-	1.50
L	0.35	0.45	0.40
Z	-	-	0.625
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

(1) Package Type: V-DFN3535-14



Dimensions	Value (in mm)
C	0.500
C1	1.500
G	0.250
G1	0.250
X	0.350
X1	0.600
X2	2.100
X3	2.350
Y	0.600
Y1	0.350
Y2	2.100
Y3	3.800

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