Low Skew 1 to 4 Clock Buffer

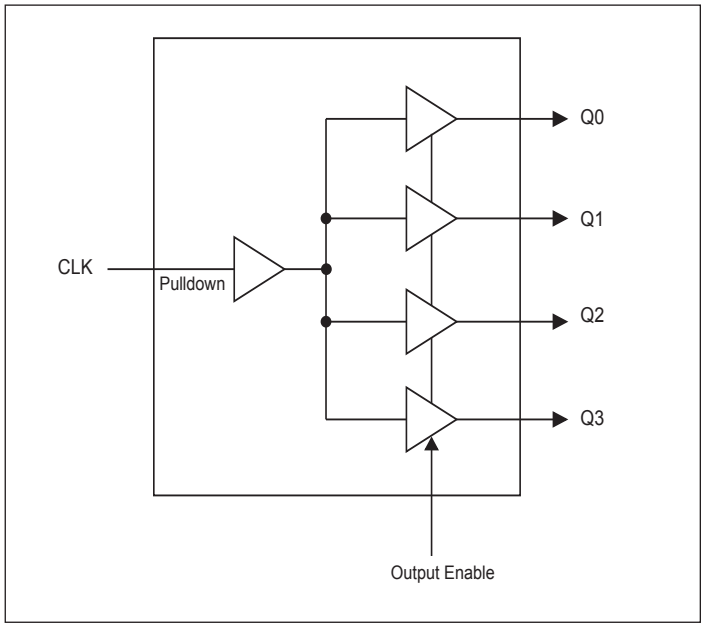
Features

- Low skew outputs (250 ps)
- Low power CMOS technology
- Operating voltages of 1.5V to 3.3V
- Output enable pin tri-states outputs
- 3.6V tolerant input clock
- Industrial temperature ranges
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen- and Antimony-Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green): 8-pin SOIC (W)

Description

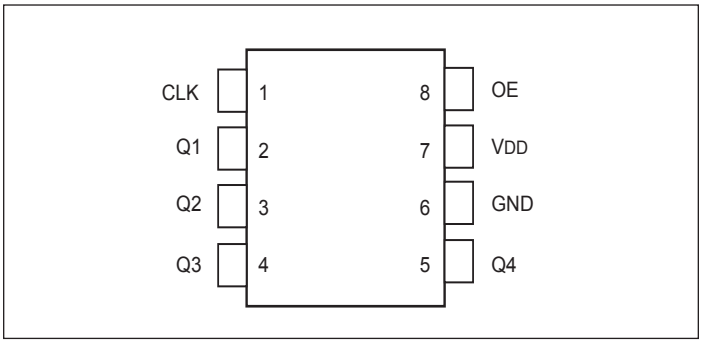
The PI6C49X0204C is a low skew, single input to four output, clock buffer. The device is perfect for fanning out multiple clock outputs.

Block Diagram



Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Descriptions

Pin#	Pin Name	Type	Pin Description
1	CLK	Input	Clock Input. 3.3V tolerant input. Internal 51kΩ pull down resistor.
2	Q1	Output	Clock Output 1.
3	Q2	Output	Clock Output 2.
4	Q3	Output	Clock Output 3.
5	Q4	Output	Clock Output 4.
6	GND	Power	Connect to ground.
7	VDD	Power	Connect to 1.5V, 1.8V, 2.5V or 3.3V.
8	OE	Input	Output Enable. Tri-states outputs when low. Internal 125KΩ pull up resistor. Default on

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 µF should be connected between VDD on pin 7 and GND on pin 6, as close to the device as possible. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

Maximum Ratings

Supply Voltage, VDD 4.6V
Output Enable and All Outputs . . . . . -0.5V to VDD+0.5V
CLK . . . . . -0.5V to 3.6V (VDD > 0V)
Junction Temperature . . . . . Max. 125°C
Storage Temperature . . . . . -65 to +150°C
ESD Protection (HBM) 2000V

Note:
Stresses above the ratings listed below can cause permanent damage to the PI6C49X0204C. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.
Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (industrial)	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+1.425		+3.6	V

DC ELECTRICAL CHARACTERISTICS

VDD=1.5 V ±5%, Ambient temperature -40 to +85° C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		1.425	1.5	1.575	V
V_{IH}	Input High Voltage	CLK(1)	1.17		3.6	V
V_{IL}	Input Low Voltage	CLK(1)			0.575	V
I_{IH}	Input High Current	CLK(1)			40	µA
I_{IL}	Input Low Current	CLK(1)			1	µA
I_{IH}	Input High Current	OE(1)			1	µA
I_{IL}	Input Low Current	OE(1)			40	µA
V_{OH}	Output High Voltage	I_{OH} = -6mA	0.95			V
V_{OL}	Output Low Voltage	I_{OL} = 6mA			0.45	V
IDD	Operating Supply Current	No load, 133 MHz			9	mA
Z_O	Nominal Output Impedance			20		Ω
C_{IN}	Input Capacitance	CLK, OE pin		5		pF
I_{OS}	Short Circuit Current			±12		mA

Notes: 1. Nominal switching threshold is VDD/2

VDD=1.8 V ±5%, Ambient temperature -40 to +85° C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		1.71	1.8	1.89	V
V_{IH}	Input High Voltage	CLK(1)	1.7		3.6	V
V_{IL}	Input Low Voltage	CLK(1)			0.6	V
I_{IH}	Input High Current	CLK(1)			50	µA
I_{IL}	Input Low Current	CLK(1)			1	µA
I_{IH}	Input High Current	OE(1)			1	µA
I_{IL}	Input Low Current	OE(1)			50	µA
V_{OH}	Output High Voltage	I_{OH} = -8mA	1.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA			0.4	V
IDD	Operating Supply Current	No load, 133 MHz			11	mA
Z_O	Nominal Output Impedance			20		Ω
C_{IN}	Input Capacitance	CLK, OE pin		5		pF
I_{OS}	Short Circuit Current			±20		mA

Notes: 1. Nominal switching threshold is VDD/2

VDD=2.5 V ±5%, Ambient temperature -40 to +85° C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		2.375	2.5	2.625	V
V_{IH}	Input High Voltage	CLK(1)	1.7		3.6	V
V_{IL}	Input Low Voltage	CLK(1)			0.7	V
I_{IH}	Input High Current	CLK(1)			60	µA
I_{IL}	Input Low Current	CLK(1)			3	µA
I_{IH}	Input High Current	OE(1)			3	µA
I_{IL}	Input Low Current	OE(1)			60	µA
V_{OH}	Output High Voltage	I_{OH} = -8mA	2			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA			0.4	V
IDD	Operating Supply Current	No load, 133 MHz			15	mA
Z_O	Nominal Output Impedance			20		Ω
C_{IN}	Input Capacitance	CLK, OE pin		5		pF
I_{OS}	Short Circuit Current			±50		mA

Notes: 1. Nominal switching threshold is VDD/2

VDD=3.3 V ±10%, Ambient temperature -40 to +85° C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Operating Voltage		3.0	3.3	3.6	V
V_{IH}	Input High Voltage	CLK(1)	2.1		3.6	V
V_{IL}	Input Low Voltage	CLK(1)			0.7	V
I_{IH}	Input High Current	CLK(1)			85	µA
I_{IL}	Input Low Current	CLK(1)			1	µA
I_{IH}	Input High Current	OE(1)			1	µA
I_{IL}	Input Low Current	OE(1)			85	µA
V_{OH}	Output High Voltage	I_{OH} = -8mA	2.8			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA			0.2	V
IDD	Operating Supply Current	No load, 133 MHz			21	mA
Z_O	Nominal Output Impedance			20		Ω
C_{IN}	Input Capacitance	CLK, OE pin		5		pF
I_{OS}	Short Circuit Current			±50		mA

Notes: 1. Nominal switching threshold is VDD/2

AC ELECTRICAL CHARACTERISTICS

VDD=1.5 V ±5%, Ambient temperature -40 to +85° C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		0		166	MHz
tOR	Output Rise Time	20% to 80%		1.0	1.5	ns
tOF	Output Fall Time	20% to 80%		1.0	1.5	ns
T_{PD}	Propagation Delay (Note1)		2	3	5	ns
T_{SK}	Output to Output Skew (Note2)	Rising edges at VDD/2		0	±250	ps

VDD=1.8 V ±5%, Ambient temperature -40 to +85° C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		0		166	MHz
tOR	Output Rise Time	20% to 80%		1.0	1.5	ns
tOF	Output Fall Time	20% to 80%		1.0	1.5	ns
T_{PD}	Propagation Delay(1)		1.3	2	4	ns
T_{SK}	Output to Output Skew(2)	Rising edges at VDD/2		0	±250	ps
J_{ADD}	Additive Jitter	@156.25MHz, 12k to 20MHz		0.1		ps

VDD=2.5 V ±5%, Ambient temperature -40 to +85° C, unless stated otherwise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		0		200	MHz
tOR	Output Rise Time	20% TO 80%		1.0	1.5	ns
tOF	Output Fall Time	20% TO 80%		1.0	1.5	ns
T_{PD}	Propagation Delay(1)		0.8	1.5	3	ns
T_{SK}	Output to Output Skew(2)	Rising edges at VDD/2		0	±250	ps
J_{ADD}	Additive Jitter	@156.25MHz, 12k to 20MHz		0.05		ps

Notes:
1. With rail to rail input clock
2. Between any 2 outputs with equal loading.

VDD=3.3 V ±10%, Ambient temperature -40 to +85° C, unless stated otherwise

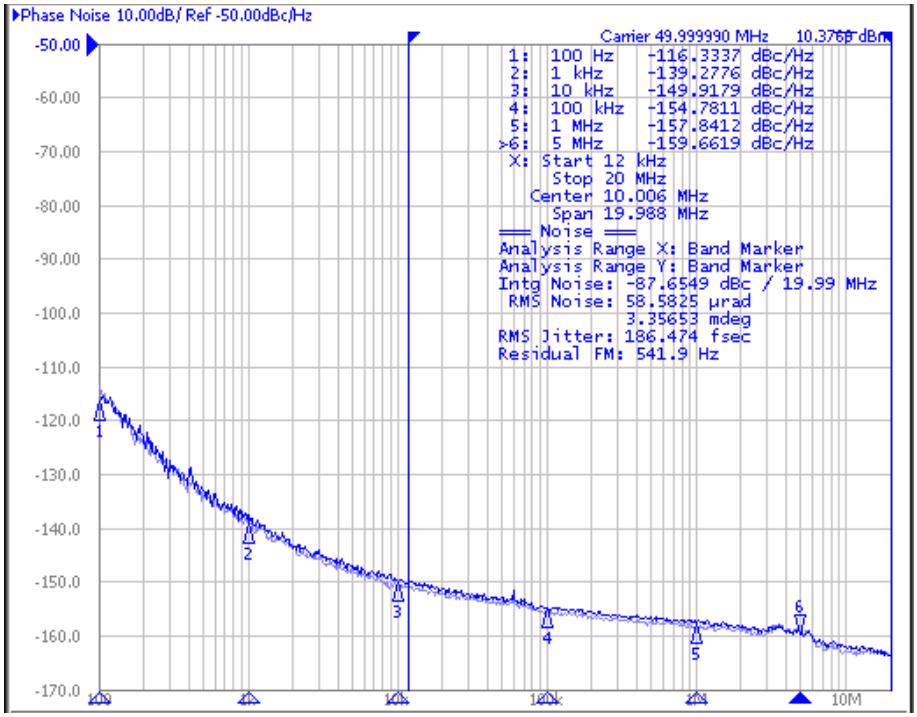
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		0		200	MHz
tOR	Output Rise Time	20% TO 80%		1.0	1.5	ns
tOF	Output Fall Time	20% TO 80%		1.0	1.5	ns
T_{PD}	Propagation Delay (Note1)		0.8	1.0	2.5	ns
T_{SK}	Output to Output Skew (Note2)	Rising edges at VDD/2		0	±250	ps
J_{ADD}	Additive Jitter	@156.25MHz, 12k to 20MHz		0.05		ps

Notes:
1. With rail to rail input clock
2. Between any 2 outputs with equal loading.

Thermal Characteristics

Symbol	Parameter	Typ.	Units
θJA	Thermal Resistance Junction to Ambient	157	°C/W
θJC	Thermal Resistance Junction to Case	42	°C/W

Phase Noise Plot



Application Information

Suggest for Unused Inputs and Outputs

LVCMOS Input Control Pins

It is suggested to add pull-up=4.7k and pull-down=1k for LVCMOS pins even though they have internal pull-up/down but with much higher value (>=50k) for higher design reliability.

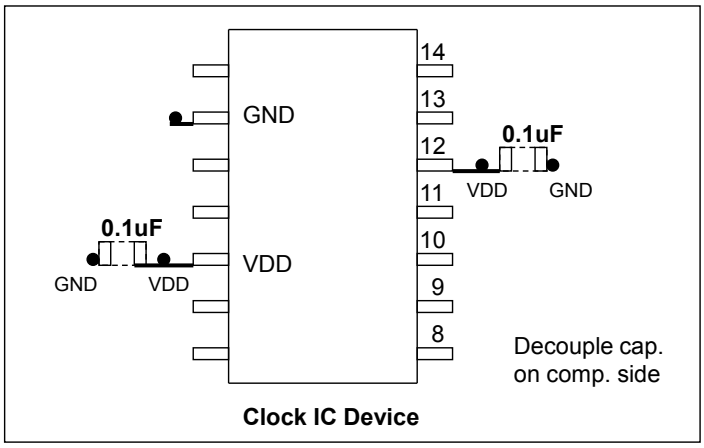
Outputs

All unused outputs are suggested to be left open and not connected to any trace. This can lower the IC power consumption.

Power Decoupling & Routing

VDD Pin Decoupling

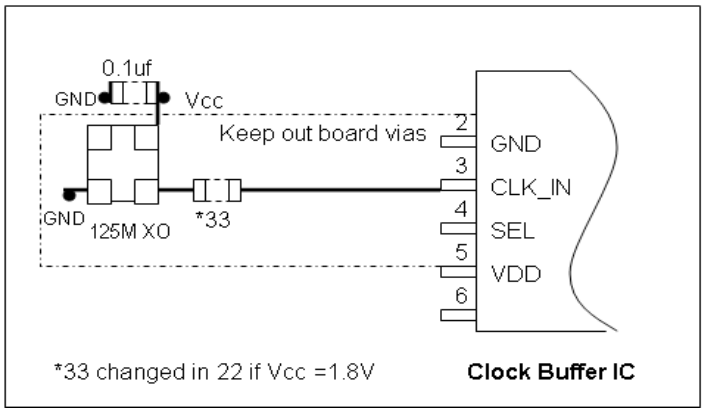
Each VDD pin must have a 0.1uF decoupling capacitor. For better decoupling, 1uF can be used. Locating the decoupling capacitor on the component side has better decoupling filter result as shown.



Placement of Decoupling caps

CMOS Clock Trace Routing

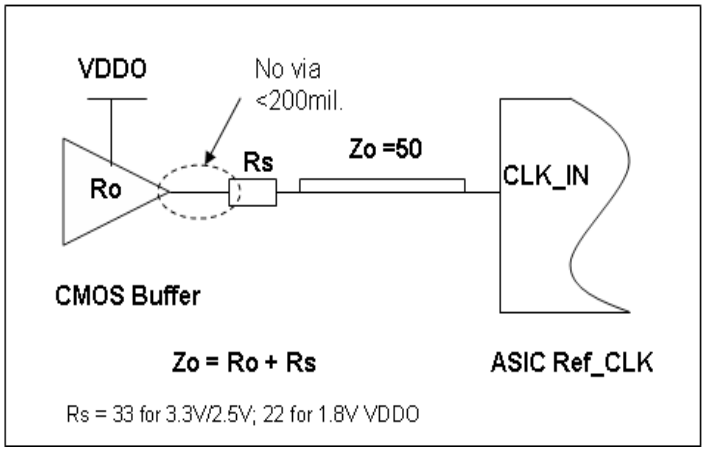
Please ensure that there is a sufficient keep-out area to the adjacent trace (>20mil.). In an example using a 125MHz XO driving a buffer IC, it is better to route the clock trace on the component side with a 33 ohm termination resistor.



CMOS Output Termination

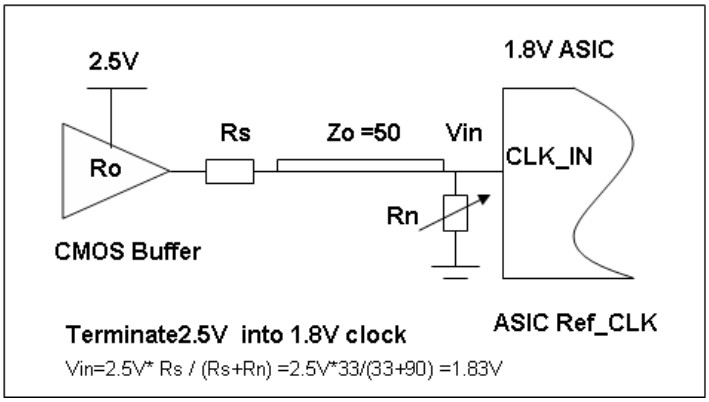
Popular CMOS Output Termination

The most popular CMOS termination is a serial resitor close to the output pin (<=200mil). It is simple and balances the drive strength. The resistor's value can be fine tuned for best performance during board bring-up based on VDDO voltage used.



Combining Serial and Parallel Termination

Designers can also use a parallel termination for CMOS outputs. For example, a 50 ohm pull-down resistor can be used at the Rx side to reduce signal reflection, but it reduces the signals V_swing in half. This pull-down can be combined with a serial resitor to form a smaller clock voltage difference. The following diagram shows how to transition a 2.5V clock into 1.8V clock.



Rs = 33Ω with Rn = 100Ω to transition 3.3V CMOS to 2.5V

Rs= 43Ω with Rn =70Ω to transition 3.3V CMOS to 1.8V

Clock Jitter Definitions

Total jitter= RJ + DJ

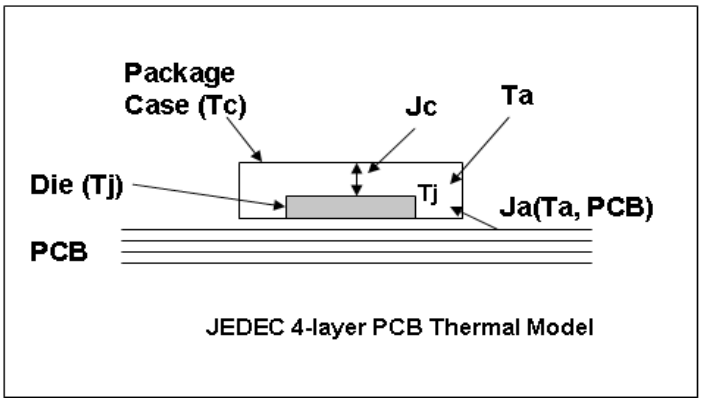
Random Jitter (RJ) is an unpredictable and unbounded timing noise that can fit in a Gaussian math distribution in RMS. RJ test values are directly related with how long or how many test samples are available. Deterministic Jitter (DJ) is timing jitter that is predictable and periodic in a fixed interference frequency. Total Jitter (TJ) is the combination of random jitter and deterministic jitter, where TJ is a factor based on total test sample count. JEDEC std. specifies digital clock TJ in 10k random samples.

Phase Jitter

Phase noise is short-term random noise attached on the clock carrier and is a function of the clock offset from the carrier; for example, dBc/Hz@10kHz, which is phase noise power in 1-Hz normalized bandwidth, vs. the carrier power @10kHz offset. Integration of phase noise in plot over a given frequency band yields RMS phase jitter; for example, to specify phase jitter <=1ps at 12k to 20MHz offset band as SONET standard specification.

Device Thermal Calculation

The JEDEC thermal model in a 4-layer PCB is shown below.



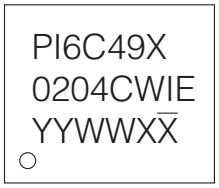
JEDEC 4-layer PCB Thermal Model

JEDEC IC Thermal Model

Important factors to influence device operating temperature are:
1) The power dissipation from the chip (P_chip) is after subtracting power dissipation from external loads. Generally it can be the no-load device Idd
2) Package type and PCB stack-up structure, for example, 1oz 4 layer board. PCB with more layers and are thicker ha better heat dissipation
3) Chassis air flow and cooling mechanism. More air flow M/s and adding heat sink on device can reduce device final die junction temperature Tj

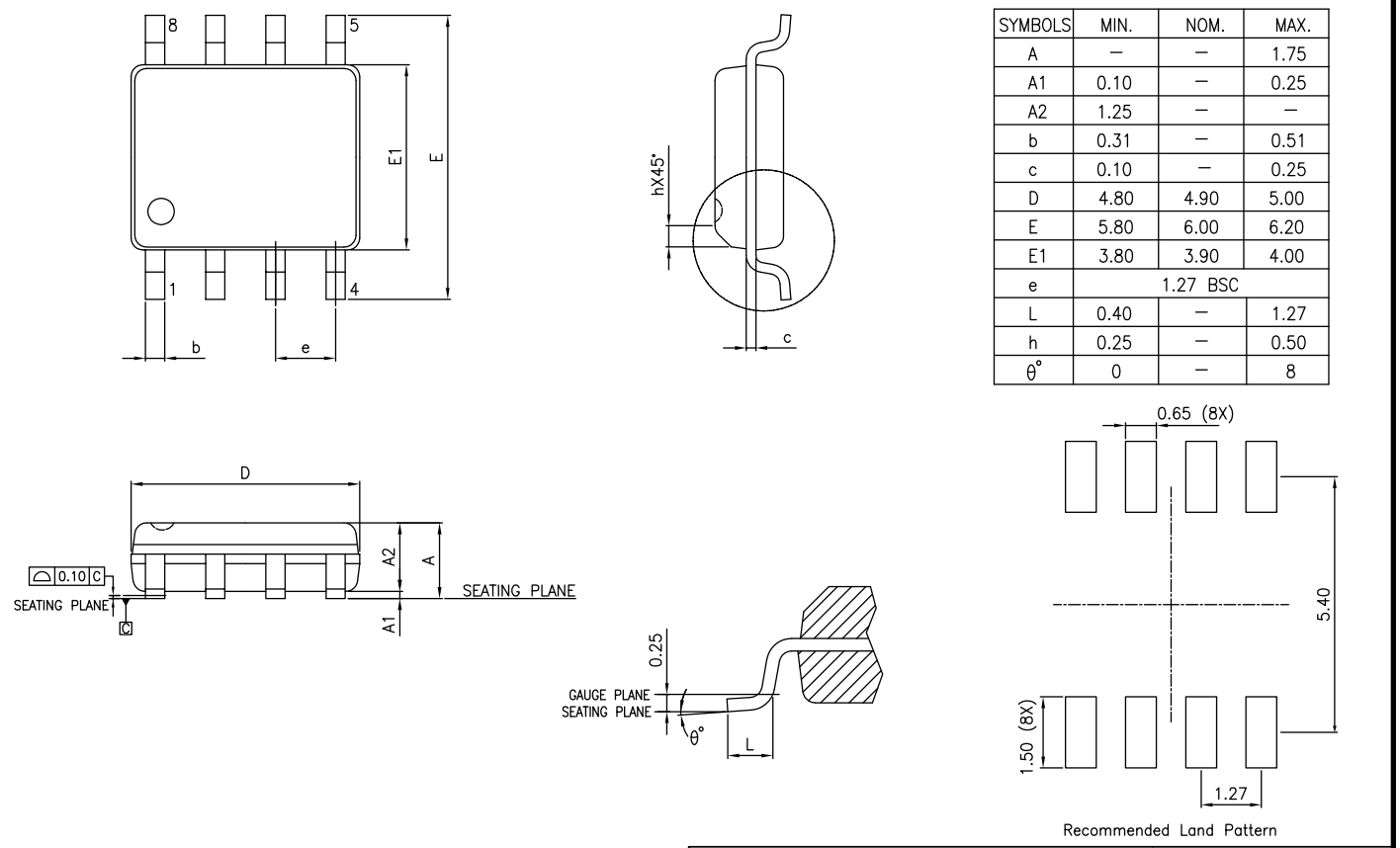
The individual device thermal calculation formula:
Tj =Ta + Pchip x Ja
Tc = Tj - Pchip x Jc
Ja ___ Package thermal resistance from die to the ambient air in C/W unit; This data is provided in JEDEC model simulation. An air flow of 1m/s will reduce Ja (still air) by 20~30%
Jc ___ Package thermal resistance from die to the package case in C/W unit
Tj ___ Die junction temperature in C (industry limit <125C max.)
Ta ___ Ambient air temperature in °C
Tc ___ Package case temperature in °C
Pchip___ IC actually consumes power through Iee/GND current

Part Marking



YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical: 8-SOIC (W)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. DIMENSIONS EXCLUDE BURRS, MOLD FLASH OR PROTRUSIONS
3. REFER JEDEC MS-012
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

20-1273

DATE: 06/02/20

DESCRIPTION: 8-Pin, 150mil-Wide, SOIC

PACKAGE CODE: W (W8)

DOCUMENT CONTROL #: PD-1001 REVISION: H

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description
PI6C49X0204CWIEX	W	8-pin, 150mil-Wide SOIC

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
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4. E = Pb-free and Green
5. X suffix = Tape/Reel

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