USB Charging Port Controller and Load Detection Power Switch

Features

- Supports CDP/DCP Modes per USB Battery Charging Specification 1.2
- Supports Shorted Mode per Chinese Telecommunication Industry Standard YD/T1591-2009
- Supports non-BC1.2 Charging Modes by Automatic Selection
  - Divider-1A mode
  - Divider-2A mode
  - DCP-1.2V mode
- Supports Sleep-Mode Charging and Mouse/Keyboard Wake up
- Load Detection for Power Supply Control in S4/S5 Charging and Port Power Management in all Charge Modes
- Compatible with USB 2.0/3.0 Power Switch Requirements
- Integrated 73-mΩ (Typ.) High-Side MOSFET
- Adjustable Current-Limit up to 3A(Typ.)
- Operating Range:4.5V to 5.5V
- Max Device Current
  - 2μA at Device Disabled
  - 270μA at Device Enabled
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen- and Antimony-Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

  https://www.diodes.com/quality/product-definitions/
- Device Package:
  - 16-pin, ZHD (UQFN)
  - 16-pin, ZH (TQFN)
- UL Listed and CB File No. US-24707-M2-UL

Description

The PI5USB2546J is a USB charging port controller and power switch with an integrated USB 2.0 high-speed data line (D+/D–) switch. The PI5USB2546J provides the electrical signatures on D+/D– to support charging schemes listed under device feature section. This series is compatible with both popular BC1.2 compliant and non-BC1.2 compliant devices.

The PI5USB2546J fully supports system wake up (from S3) with a mouse/keyboard (both low speed and full speed). The PI5USB2546J also supports two distinct power management features, namely, power wake and port power management (PPM) through /STATUS pin. Power wake allows for power supply control in S4/S5 charging and PPM manages port power in a multi-port application.

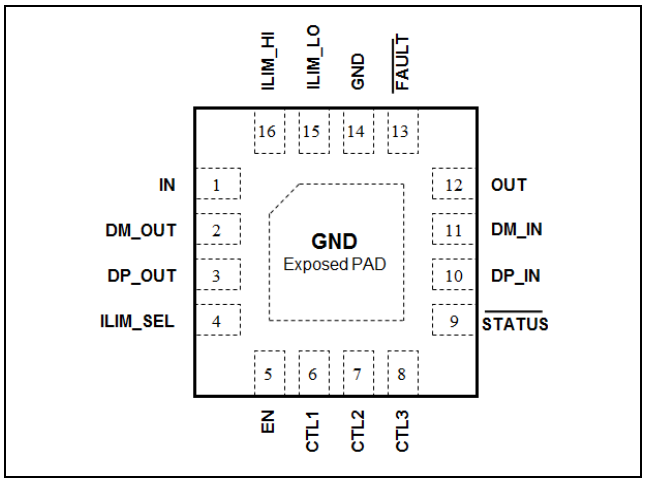
The PI5USB2546J 73-mΩ power-distribution switch is intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. Two programmable current thresholds provide flexibility for setting current limits and load-detect thresholds.

Applications

- USB Ports (Host and Hubs)
- Notebook and Desktop PCs
- Universal Wall Charging Adapters

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration (Top View)



Pin Description

Pin #	Name	Type	Description
1	IN	P	Input voltage and supply voltage; connect 0.1µF or greater ceramic capacitor from IN to GND as close to the device as possible
2	DM_OUT	I/O	D- Data line to USB host controller.
3	DP_OUT	I/O	D+ data line to USB host controller.
4	ILIM_SEL	I	Logic-level input signal used to control the charging mode, current limit threshold, and load detection, see the control truth table. Can be tied directly to IN or GND without pull-up or pull-down resistor.
5	EN	I	Logic-level input for turning the power switch and the signal switches on/off, logic low turns off the signal and power switches and holds OUT in discharger. Can be tied directly to IN or GND without pull-up or pull-down resistor.
6	CTL1	I	Logic-level inputs used to control the charging mode and signal switches; see the control truth table. Can be tied directly to IN or GND without pull-up or pull-down resistor.
7	CTL2	I	
8	CTL3	I	
9	$\overline{\text{STATUS}}$	O	Active-low open-drain output, asserted in load detection conditions.
10	DP_IN	I/O	D+ data line to downstream connector
11	DM_IN	I/O	D- data line to downstream connector.
12	OUT	P	Power-switch output
13	$\overline{\text{FAULT}}$	O	Active-low open-drain output, asserted when over-temperature or current limit condition occurs
14	GND	G	Ground connection
15	ILIM_LO	I	External resistor connection used to set the low current-limit threshold and the load detection current threshold. A resistor to ILIM_LO is optional; see Current-Limit Settings.
16	ILIM_HI	I	External resistor connection used to set the high current-limit threshold.
NA	Exposed PAD	G	Internally connected to GND. Thermal pad to heat-sink the part to the circuit board.

** I = Input; O = Output; P = Power; G = Ground*

Maximum Ratings

All Input (except IN to OUT, and DP_IN, DM_IN, DP_OUT, DM_OUT) ..... -0.3V to +6.0V
IN to OUT ..... -6.0V to +6.0V
DP_IN, DM_IN, DP_OUT, DM_OUT ..... -0.3V to IN+0.3 or +5.7V
Input clamp current (DP_IN, DM_IN, DP_OUT, DM_OUT) ..... ±20mA
Continuous current in SDP or CDP mode
(DP_IN to DP_OUT or DM_IN to DM_OUT) ..... ±100mA
Continuous current in BC1.2 DCP mode (DP_IN to DM_IN) ..... ±50mA
Continuous output current (OUT) ..... Internally limited
Continuous output sink current (/FAULT, /STATUS) 25mA
Continuous output source current (ILIM_LO, ILIM_HI) ..... internally limited
ESD: HBM Mode (All pins) 2kV
CDM Mode (All pins) 500V
HBM (USB connector pins: DP_IN, DM_IN, OUT to GND) 6kV

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage, IN	4.5	-	5.5	V
	Input Voltage, logic-level EN, CTL1, CTL2, CTL3, ILIM_SEL inputs	0	-	5.5	V
	Input Voltage, data line inputs, DP_IN, DM_IN, DP_OUT, DM_OUT	0	-	V_{IN}	V
V_{IH}	High-level input voltage, EN, CTL1, CTL2, CTL3, ILIM_SEL	1.8	-	-	V
V_{IL}	Low-level input voltage, EN, CTL1, CTL2, CTL3, ILIM_SEL	-	-	0.8	V
	Continuous current data line inputs, SDP or CDP mode, DP_IN to DP_OUT or DM_IN to DM_OUT	-	-	±30	mA
	Continuous current data line inputs, BC1.2 DCP mode, DP_IN to DM_IN	-	-	±15	mA
I_{OUT}	Continuous output current, OUT	0	-	2.5	A
	Continuous output sink current, /FAULT, /STATUS	0	-	10	mA
R_{ILIM_XX}	Current-limit set resistor	16.9	-	750	kΩ
T_J	Operating Virtual Junction Temperature Range	-40	-	125	ºC

Electrical Characteristics

4.5V≤V_{IN}≤5.5V; T_J=-40°C to +125°C; V_{EN} =V_{IN}, V_{ILIM_SEL}=V_{IN}, V_{CTL1}= V_{CTL2}= V_{CTL3}=V_{IN}, $R_{/FAULT}$=$R_{/STATUS}$=10kΩ R_{ILIM_HI}=20kΩ, R_{ILIM_LO}=80.6kΩ, Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND. unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Power Switch						
$R_{DS(on)}$	On Resistance(1)	T_J = 25°C, I_{OUT} = 2A		73	84	mΩ
		-40°C ≤ T_J ≤ 85°C, I_{OUT} = 2A		73	105	
		-40°C ≤ T_J ≤ 125°C, I_{OUT} = 2A		73	120	
t_r	OUT voltage rise time	VIN = 5V, CL = 1µF, RL = 100Ω	0.7	1.0	1.60	ms
t_f	OUT voltage fall time		0.2	0.35	0.5	
t_{on}	OUT voltage turn-on time	VIN = 5V, CL = 1µF, RL = 100Ω		2.7	4	ms
t_{off}	OUT voltage turn-off time			1.7	3	
I_{REV}	Reverse leakage current	V_{OUT} = 5.5V, V_{IN} = V_{EN} = 0V, -40°C ≤ T_J ≤ 85°C, Measure I_{OUT}			2	µA
Discharge						
R_{DCHG}	OUT discharge resistance	V_{OUT} = 4V, V_{EN} = 0V	400	500	630	Ω
t_{DCHG}	OUT discharge hold time	Time V_{OUT}< 0.7V	1.30	2.0	2.9	s
EN, ILIM_SEL, CTL1,CTL2, CTL3, inputs						
	Input pin rising logic threshold voltage	-	1	1.35	1.70	V
	Input pin falling logic threshold voltage	-	0.85	1.15	1.45	V
	Hysteresis(2)	-	-	200	-	mV
	Input current	Pin voltage= 0V to 5.5V	-0.5	-	0.5	µA

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; Thermal effects must be taken into account separately
(2) These parameters are provided for reference only and do not constitute part of Diodes' published device specifications for purposes of Diodes' product warranty

Electrical Characteristics

4.5V≤V_{IN}≤5.5V; T_J=-40°C to +125°C; V_{EN} =V_{IN}, V_{ILIM_SEL}=V_{IN}, V_{CTL1}= V_{CTL2}= V_{CTL3}=V_{IN}, $R_{/FAULT}$=$R_{/STATUS}$=10kΩ R_{ILIM_HI}=20kΩ, R_{ILIM_LO}=80.6kΩ, Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND. unless otherwise specified.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
ILIM_SEL Current Limit						
I_{OS}	OUT Current-limit(2)	V_{ILIM_SEL}= 0 V R_{ILIM_LO}=210kΩ	205	240	275	mA
		V_{ILIM_SEL}= 0 V R_{ILIM_LO}=80.6kΩ	575	625	680	
		V_{ILIM_SEL}= 0 V R_{ILIM_LO}=22.1kΩ	2120	2275	2430	
		V_{ILIM_SEL}= V_{IN} R_{ILIM_HI}=20kΩ	2340	2510	2685	
		V_{ILIM_SEL}= V_{IN} R_{ILIM_HI}=16.9kΩ	2770	2970	3170	
t_{IOS}	Response time to OUT short circuit(1)	V_{IN} = 5.0V, R=0.1Ω, lead length=2”	-	1.5	-	µs
Supply Current						
I_{IN_OFF}	Disabled IN supply current	V_{EN}=0V, V_{OUT}=0V, T_J =-40°C to +125°C	-	0.1	2	µA
I_{IN_ON}	Enable IN supply current	V_{CTL1}=V_{CTL2}= V_{IN}; V_{CTL3}= 0V V_{ILIM_SEL} = 0V	-	165	220	
		V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}, V_{ILIM_SEL} = 0V	-	175	230	
		V_{CTL1} = V_{CTL2} = V_{IN}; V_{CTL3} = 0V, V_{ILIM_SEL} = V_{IN}	-	185	240	
		V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN},V_{ILIM_SEL} = V_{IN}	-	195	250	
		V_{CTL1} = 0V; V_{CTL2} = V_{CTL3} = V_{IN}, V_{ILIM_SEL} = 0V	-	215	270	
		V_{CTL1} = 0V; V_{CTL2} = V_{CTL3} = V_{IN}, V_{ILIM_SEL} = V_{IN}	-	240	295	
Undervoltage Lockout						
V_{UVLO}	IN rising UVLO threshold voltage	-	3.9	4.1	4.3	V
	Hysteresis(1)	-	-	100	-	mV
/FAULT						
V_{OL}	Output low voltage	$I_{/FAULT}$ = 1mA	-	-	100	mV
I_{OFF}	Off-state leakage current	$V_{/FAULT}$ = 5.5V	-	-	1	µA
T_D	Over current /FAULT rising and falling deglitch	-	5	8.2	12	ms
/STATUS						
V_{OL}	Output low voltage	$I_{/STATUS}$ = 1mA	-	-	100	mV
I_{OFF}	Off-state leakage	$V_{/STATUS}$ = 5.5V	-	-	1	µA
Thermal Shutdown						
OTSD	Thermal shutdown threshold	-		170	-	°C
	Hysteresis(1)	-	-	20	-	

Note:

(1) These parameters are provided for reference only and do not constitute part of Diodes’ published device specifications for purposes of Diodes’ product warranty

(2) Pulse-testing techniques maintain junction temperature close to ambient temperature; current limit value tested at 80% output voltage. Thermal effects must be taken into account separately.

Electrical Characteristics, High-Bandwidth Switch

$4.5V \le V_{IN} \le 5.5V$; T_J=-40°C to +125°C; $V_{EN} = V_{IN}$, $V_{ILIM\_SEL} = V_{IN}$, $V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}$, $R_{/FAULT} = R_{/STATUS}$=10kΩ R_{ILIM_HI}=20kΩ, R_{ILIM_LO}=80.6kΩ, Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND. unless otherwise specified.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
HIGH_BANDWIDTH ANALOG SWITCH						
	DP/DM switch on resistance	V_{DP/DM_OUT}= 0V, I_{DP/DM_IN}= 30mA	-	2	4	Ω
		V_{DP/DM_OUT}= 2.4V, I_{DP/DM_IN}= -15mA	-	3	6	Ω
	Switch resistance mismatch between DP/DM channels	V_{DP/DM_OUT}= 0V, I_{DP/DM_IN}= 30mA	-	0.05	0.15	Ω
		V_{DP/DM_OUT}= 2.4V, I_{DP/DM_IN}= -15mA	-	0.05	0.15	Ω
	DP/DM switch off-state capacitance(1)	V_{EN}=0V, V_{DP/DM_IN}= 0.3V, V_{ac}= 0.6V_{PK-PK}, f=1MHz	-	4.5		pF
	DP/DM switch on-state capacitance(2)	V_{DP/DM_IN}= 0.3V,V_{ac}= 0.6V_{PK-PK}, f = 1MHz	-	5.4	6.2	pF
O_{IRR}	Off-state isolation(3)	V_{EN} = 0V, f = 250MHz	-	33	-	dB
X_{TALK}	Off-state cross channel isolation(3)	f = 250MHz	-	52	-	dB
I_{OFF}	Off-state leakage current	V_{EN} = 0V, V_{DP/DM_IN} = 3.6V, V_{DP/DM_OUT} = 0V, measure I_{DP/DM_OUT}	-	0.1	1.5	µA
BW	Bandwidth(-3dB)(3)	R_L =50Ω	-	2.0	-	GHz
t_{pd}	Propagation delay(3)	-	-	0.25	-	ns
t_{SK}	Skew between opposite transitions of the same port($t_{PHL} - t_{PLH}$)	-	-	0.1	0.2	ns

Note:

(1) The resistance in series with the parasitic capacitance to GND is typically 250 Ω.
(2) The resistance in series with the parasitic capacitance to GND is typically 150 Ω.
(3) These parameters are provided for reference only and do not constitute part of Diodes' published device specifications for purposes of Diodes' product warranty.

Electrical Characteristics, Charging Controller

4.5V≤V_{IN}≤5.5V; T_J=-40°C to +125°C; V_{EN} =V_{IN}, V_{ILIM_SEL}=V_{IN}, V_{CTL1}= V_{CTL2}= V_{CTL3}=V_{IN}, $R_{/FAULT}$=$R_{/STATUS}$=10kΩ R_{ILIM_HI}=20kΩ, R_{ILIM_LO}=80.6kΩ, Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND. unless otherwise specified.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
SHORTED MODE (BC1.2 DCP)						
	DP_IN/DM_IN shorting resistance	V_{CTL1}= V_{IN}; V_{CTL2}= V_{CTL3}= 0V	-	125	200	Ω
DCP-1.2V MODE						
	DP_IN/DM_IN output voltage	V_{CTL1}= 0V; V_{CTL2}= V_{CTL3}= V_{IN}, Apply 3V on DP_IN for 0.5s and measure the D+/D- voltage within the 2s	1.19	1.25	1.31	V
	DP_IN/DM_IN output impedance		60	75	94	kΩ
DIVIDER-1A MODE						
	DP_IN Divider-1A output voltage	V_{CTL1}= 0V; V_{CTL2}= V_{CTL3}= V_{IN},	1.9	2.0	2.1	V
	DM_IN Divider-1A output voltage		2.57	2.7	2.84	V
	DP_IN/DM_IN output impedance		7.5	10.5	16	kΩ
DIVIDER-2A MODE						
	DP_IN Divider-2A output voltage	V_{CTL1}= 0V; V_{CTL2}= V_{CTL3}= V_{IN}; I_{OUT}= 1A	2.57	2.7	2.84	V
	DM_IN Divider-2A output voltage		1.9	2.0	2.1	V
	DP_IN/DM_IN output impedance		7.5	10.5	16	kΩ
CHARGING DOWNSTREAM PORT						
V_{DM_SRC}	DP_IN CDP output voltage	V_{CTL1}= V_{CTL2}= V_{CTL3}= V_{IN}, V_{IN} =0.6V, -250μA ≤ I_{DM_IN} ≤ 0μA	0.5	0.6	0.7	V
V_{DAT_REF}	DP_IN rising lower window threshold for V_{DM_SRC} activation	V_{CTL1}= V_{CTL2}= V_{CTL3}= V_{IN}	0.25	-	0.4	V
	Hysteresis(1)		-	50	-	mV
V_{LGC_REF}	DP_IN rising upper window threshold for V_{DM_SRC} de-activation		0.8	-	1.5	V
	Hysteresis(1)		-	100	-	mV
LOAD DETECT- NON POWER WAKE						
I_{LD} ($R_{ILIM\ LO}$ = 80.6kΩ)	I_{OUT} rising load detect current threshold	V_{CTL1}= V_{CTL2}= V_{CTL3}= V_{IN}	550	650	765	mA
	Hysteresis(1)		-	50	-	mA
I_{LD} ($R_{ILIM\ LO}$ = 2.7MΩ)	I_{OUT} rising load detect current threshold		30	-	100	mA
	I_{OUT} falling load detect current threshold		1	-	70	mA
t_{LD_SET}	Load detect set time		140	200	275	ms
	Load detect reset time		1.9	3	4.2	s

Note:

(1) These parameters are provided for reference only and do not constitute part of Diodes' published device specifications for purposes of Diodes' product warranty.

Electrical Characteristics, Charging Controller

4.5V≤V_{IN}≤5.5V; T_J=-40°C to +125°C; V_{EN} =V_{IN}, V_{ILIM_SEL}=V_{IN}, V_{CTL1}= V_{CTL2}= V_{CTL3}=V_{IN}, $R_{/FAULT}$=$R_{/STATUS}$=10kΩ R_{ILIM_HI}=20kΩ, R_{ILIM_LO}=80.6kΩ, Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND. unless otherwise specified.

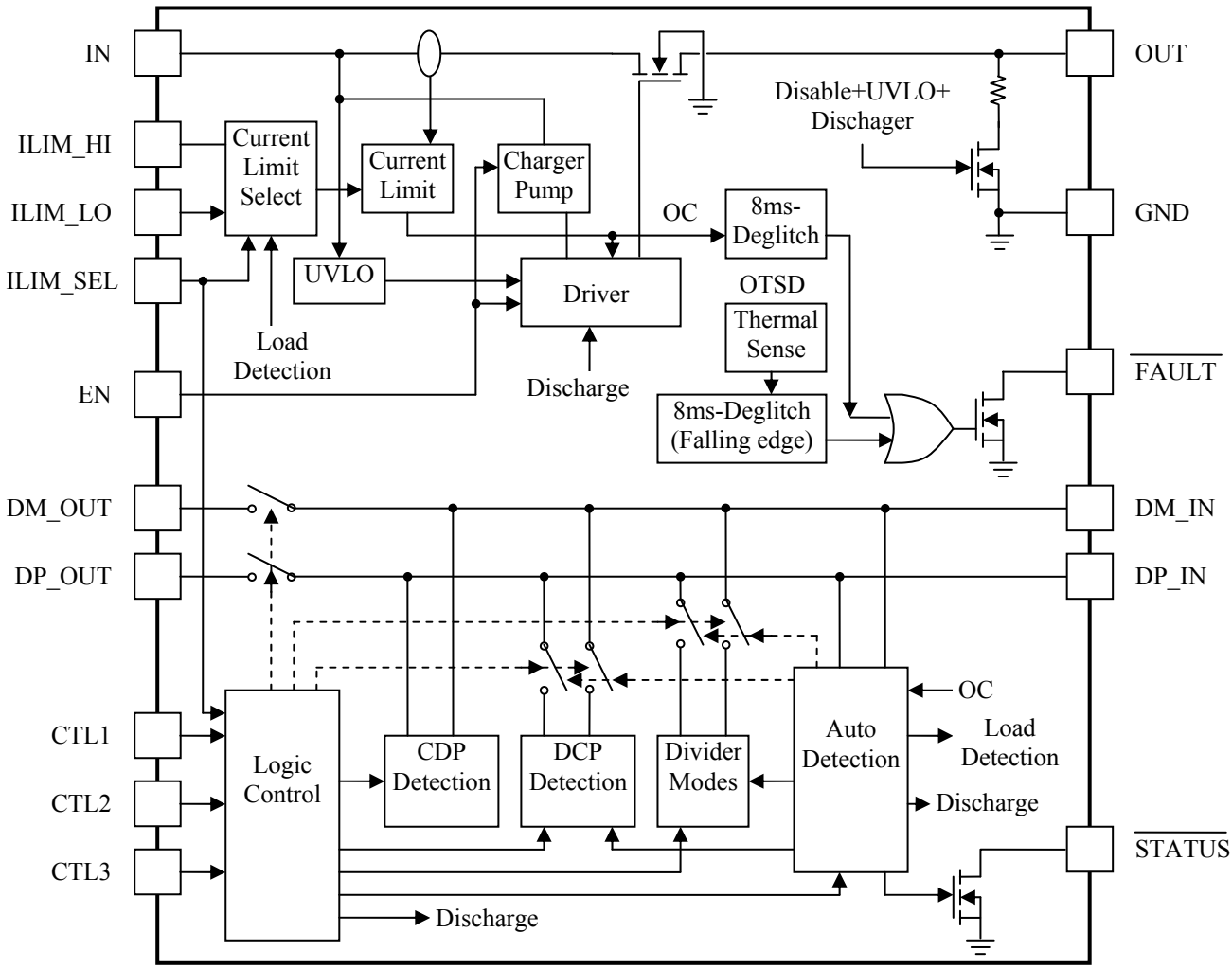
Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
LOAD DETECT- POWER WAKE						
I_{OS_PW}	Power wake short circuit current limit	V_{CTL1}= V_{CTL2}= 0V, V_{CTL3}= V_{IN}	20	55	90	mA
	I_{OUT} falling power wake reset current threshold		10	45	85	mA
	Reset current hysteresis(1)		-	5	-	mA
	Power wake reset time		10.7	15	20.6	s

Note:

(1) These parameters are provided for reference only and do not constitute part of Diodes' published device specifications for purposes of Diodes' product warranty.

Functional Description

PI5USB2546J Block Diagram



Details Description

The following overview references various industry standards. It is always recommended to consult the most up-to-date standard to ensure the most recent and accurate information. Rechargeable portable equipment requires an external power source to charge its batteries. USB ports are a convenient location for charging because of an available 5V power source. Universally accepted standards are required to make sure host and client-side devices operate together in a system to ensure power management requirements are met. Traditionally, host ports following the USB 2.0 specification must provide at least 500mA to downstream client-side devices. Because multiple USB devices can be attached to a single USB port through a bus-powered hub, it is the responsibility of the client-side device to negotiate its power allotment from the host to ensure the total current draw does not exceed 500mA. In general, each USB device is granted 100mA and may request more current in 100mA unit steps up to 500mA. The host may grant or deny based on the available current. A USB 3.0 host port not only provides higher data rate than USB 2.0 port but also raises the unit load from 100mA to 150mA. It is also required to provide a minimum current of 900mA to downstream client-side devices.

Additionally, the success of USB has made the mini-USB connector a popular choice for wall adapter cables. This allows a portable device to charge from both a wall adapter and USB port with only one connector. As USB charging has gained popularity, the 500mA minimum defined by USB 2.0 or 900mA for USB 3.0 has become insufficient for many handset and personal media players which need a higher charging rate. Wall adapters can provide much more current than 500mA/900mA. Several new standards have been introduced defining protocol handshaking methods that allow host and client devices to acknowledge and draw additional current beyond the 500mA/900mA minimum defined by USB 2.0/3.0 while still using a single micro-USB input connector. The PI5USB2546J supports four of the most common USB charging schemes found in popular hand-held media and cellular devices:

- USB Battery Charging Specification BC1.2
- Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider-1A and Divider-2A
- DCP-1.2V Mode

YD/T 1591-2009 is a subset of BC1.2 spec. supported by vast majority of devices that implement USB charging.
Divider-1A, Divider-2A and DCP-1.2V charging schemes are supported in devices from specific yet popular device makers.
BC1.2 lists three different port types as listed below:

- Standard Downstream Port (SDP)
- Charging Downstream Port (CDP)
- Dedicated Charging Port (DCP)

BC1.2 defines a charging port as a downstream facing USB port that provides power for charging portable equipment, under this definition CDP and DCP are defined as charging ports
Table 1 shows the differences between these ports.

Table 1. Operation Modes

Port Type	Support USB 2.0 Communication	Max. allowable current draw by portable device
SDP (USB 2.0)	Yes	0.5A
SDP (USB 3.0)	Yes	0.9A
CDP	Yes	1.5A
DCP	No	1.5A

Standard Downstream Port (SDP) USB 2.0/USB 3.0

An SDP is a traditional USB port that follows USB 2.0/3.0 protocol and supplies a minimum of 500mA/900mA per port. USB 2.0/3.0 communications is supported, and the host controller must be active to allow charging. PI5USB2546J supports SDP mode in system power state S0 when system is completely powered ON and fully operational. For more details on control pin (CTL1, CTL2, CTL3 and ILIM_SEL) settings to program this state please refer to device truth table.

Charging Downstream Port (CDP)

A CDP is a USB port that follows USB BC1.2 and supplies a minimum of 1.5A per port. It provides power and meets USB 2.0 requirements for device enumeration. USB 2.0 communications is supported and the host controller must be active to allow charging. What separates a CDP from an SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device and allows for additional current draw by the client device.

The CDP hand-shaking process is done in two steps. During step one the portable equipment outputs a nominal 0.6V output on its D+ line and reads the voltage input on its D- line. The portable device concludes it is connected to an SDP if the voltage is less than the nominal data detect voltage of 0.3V. The portable device concludes that it is connected to a Charging Port if the D- voltage is greater than the nominal data detect voltage of 0.3V and optionally less than 0.8V.

The second step is necessary for portable equipment to determine if it is connected to CDP or DCP. The portable device outputs a nominal 0.6V output on its D- line and reads the voltage input on its D+ line. The portable device concludes it is connected to a CDP if the data line being read remains less than the nominal data detect voltage of 0.3V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3V.

PI5USB2546J supports CDP mode in system power state S0 when system is completely powered ON and fully operational. For more details on control pin (CTL1, CTL2, CTL3 and ILIM_SEL) settings to program this state please refer to device truth table.

Dedicated Charging Port (DCP)

A DCP only provides power but does not support data connection to an upstream port. As shown in following sections, a DCP is identified by the electrical characteristics of its data lines. The PI5USB2546J emulates DCP in two charging states, namely DCP Forced and DCP Auto as shown in Figure 4. In DCP Forced state the device will support one of the two DCP charging schemes, namely Divider-1A or DCP_Shorted. In the DCP Auto state, the device charge detection state machine is activated to selectively implement charging schemes involved with the Shorted DCP mode, Divider-1A, Divider-2A and DCP-1.2V modes. Shorted DCP mode complies with BC1.2 and Chinese Telecommunications Industry Standard YD/T 1591-2009, while the Divider-1A, Divider-2A and DCP-1.2V modes are employed to charge devices that do not comply with BC1.2 DCP standard.

DCP BC1.2 and YD/T 1591-2009

Both standards define that the D+ and D- data lines should be shorted together with a maximum series impedance of 200Ω. This is shown as Figure 1.

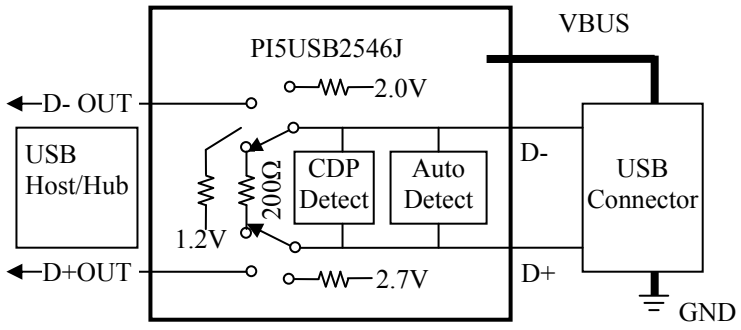


Figure 1. DCP Supporting BC1.2/YD/T 1591-2009

Divider-1A and Divider-2A Charging Scheme

There are two charging schemes supported by PI5USB2546J, Divider-1A and Divider-2A as shown below. In Divider-1A charging scheme the device applies 2.0V and 2.7V to D+ and D- data line respectively. This is reversed in Divider-2A mode.

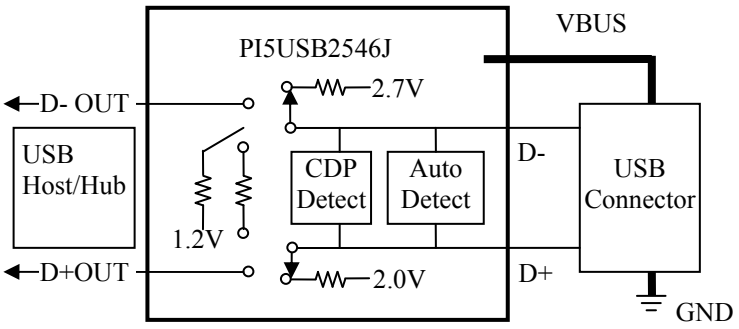


Figure 2a. Divider-1A Charging Scheme

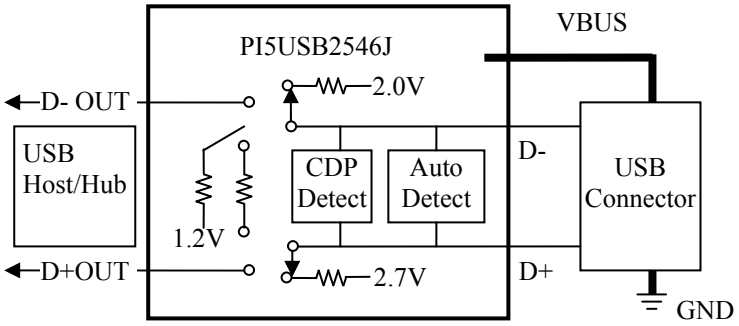


Figure 2b. Divider-2A Charging Scheme

DCP-1.2V Charging Scheme

DCP-1.2V charging scheme is used by some handheld devices to enable fast charging at 2.0A. PI5USB2546J supports this scheme in the DCP-Auto mode before the device enters BC1.2 shorted mode. To simulate this charging scheme D+/D- lines are shorted and pulled-up to 1.2V for fixed duration then device moves to DCP shorted mode as defined in BC1.2 spec. This is shown as Figure 3.

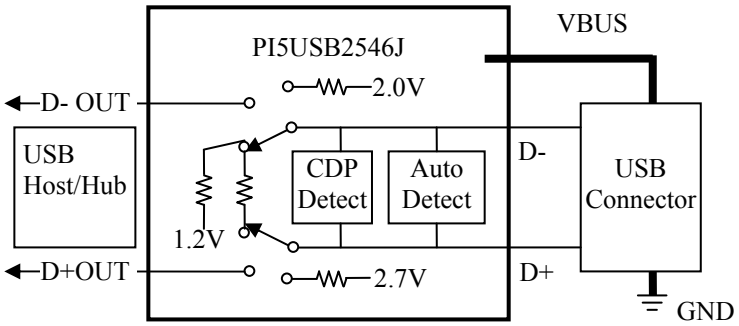


Figure 3. DCP-1.2V Charging Scheme

DCP Auto Mode

As mentioned above the PI5USB2546J integrates an auto-detect state machine that supports all the above DCP charging schemes. It starts in Divider-1A scheme, however if a BC1.2 or YD/T 1591-2009 compliant device is attached, the PI5USB2546J responds by discharging OUT, turning back on the power switch and operating in 1.2Vmode briefly and then moving to BC1.2 DCP mode. It then stays in that mode until the device releases the data line, in which case it goes back to Divider-1A scheme. When a Divider-1A compliant device is attached the PI5USB2546J will stay in Divider-1A state.

Also, the PI5USB2546J will automatically switch between the Divider-1A and Divider-2A schemes based on charging current drawn by the connected device. Initially the device will set the data lines to Divider-1A scheme. If charging current of the device >750mA is measured by the PI5USB2546J, it switches to Divider-2A scheme and test to see if the peripheral device will still charge at a high current. If it does then it stays in Divider-2A charging scheme otherwise it will revert to Divider-1A scheme.

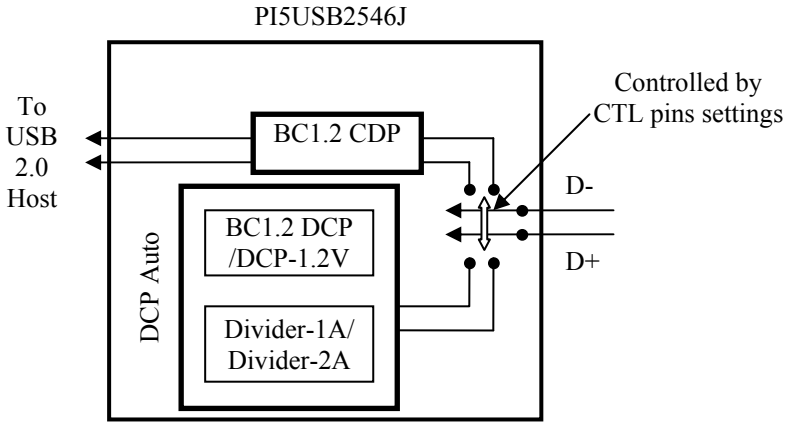


Figure 4. DCP_Auto Mode

DCP Forced Shorted / DCP Forced Divider-1A

In this mode the device is permanently set to one of the DCP schemes (BC1.2/ YD/T 1591-2009 or Divider-1A) as commanded by its control pin setting per device truth table.

High-Bandwidth Data Line Switch

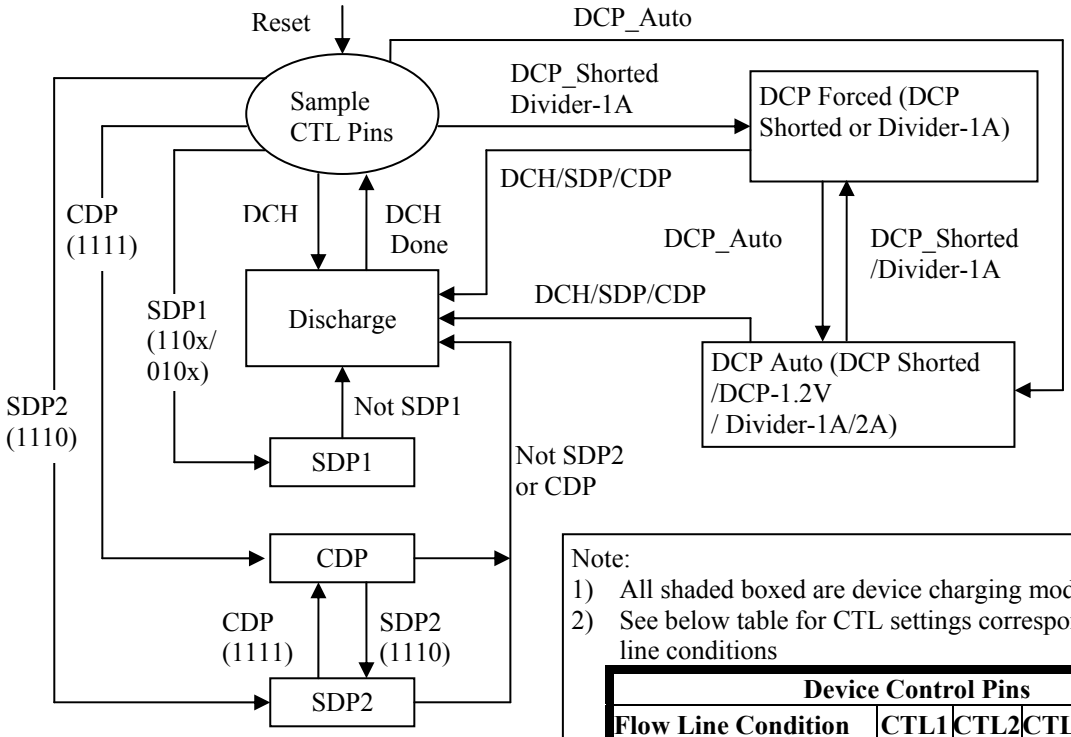
The PI5USB2546J passes the D+ and D- data lines through the device to enable monitoring and handshaking while supporting charging operation. A wide bandwidth signal switch is used, allowing data to pass through the device without corrupting signal integrity. The data line switches are turned on in any of CDP or SDP operating modes.
The EN input also needs to be at logic High for the data line switches to be enabled.

NOTE:

1. Under CDP mode, the data switches are ON even while CDP handshaking is occurring.
2. The data line switches are OFF if EN or all CTL pins are held low, or if in DCP mode. They are not automatically turned off if the power switch (IN to OUT) is in current limit.
3. The data switches are for USB 2.0 differential pair only. In the case of a USB 3.0 host, the super speed differential pairs must be routed directly to the USB connector without passing through the PI5USB2546J.
4. Data switches are OFF during OUT (VBUS) discharge

Device Operation

Please refer to the simplified device state diagram below. Power-on-reset (POR) holds device in initial state while output is held in discharge mode. Any POR event will take the device back to initial state. After POR clears, device goes to the next state depending on the CTL1, CTL2, CTL3 and ILIM_SEL lines as shown Figure 5.



Note:
1) All shaded boxed are device charging modes.
2) See below table for CTL settings corresponding to flow line conditions

Device Control Pins				
Flow Line Condition	**CTL1**	**CTL2**	**CTL3**	**ILIM_SEL**
DCH(Discharge)	0	0	0	x
CDP	1	1	1	1
SDP2(No Discharge from/to CDP)	1	1	1	0
SDP1(Discharge from/to any charging state including CDP)	1	1	0	x
	0	1	0	x
DCP_Short	1	0	0	x
DCP/Divider-1A	1	0	1	x
DCP_Auto	0	1	1	x
	0	0	1	x

Figure 5. PI5USB2546J Charging States

Output Discharge

To allow a charging port to renegotiate current with a portable device, PI5USB2546J uses the OUT discharge function. It proceeds by turning off the power switch while discharging OUT, then turning back on the power switch to reassert the OUT voltage. This discharge function is automatically applied as shown in device state diagram.

Wake on USB Feature (Mouse/Keyboard Wake Feature)

USB 2.0 Background Information

The PI5USB2546J data lines interface with USB 2.0 devices. USB 2.0 defines three types of devices according to data rate. These devices and their characteristics relevant to PI5USB2546J Wake on USB operation are shown below:

Low-speed USB devices

- 1.5 Mb/s
- Wired mice and keyboards are examples
- No devices that need battery charging
- All signaling performed at 2.0V and 0.8V hi/lo logic levels
- D- high to signal connect and when placed into suspend
- D- high when not transmitting data packets

Full-speed USB devices

- 12 Mb/s
- Wireless mice and keyboards are examples
- Legacy phones and music players are examples
- Some legacy devices that need battery charging
- All signaling performed at 2.0V and 0.8V hi/lo logic levels
- D+ high to signal connect and when placed into suspend
- D+ high when not transmitting data packets

High-speed USB devices

- 480 Mb/s
- Tablets, phones and music players are examples
- Many devices that need battery charging
- Connect and suspend signaling performed at 2.0V and 0.8V hi/lo logic levels
- Data packet signaling performed a logic levels below 0.8V
- D+ high to signal connect and when placed into suspend (same as a full-speed device)
- D+ and D- low when not transmitting data packets

Wake On USB

Wake on USB is the ability of a wake configured USB device to wake a computer system from its S3 sleep state back to its S0 working state. Wake on USB requires the data lines to be connected to the system USB host before the system is placed into its S3 sleep state and remain continuously connected until they are used to wake the system.

The PI5USB2546J supports low and full speed HID (human interface device like mouse/key board) wake function. There are two scenarios under which wake on mouse are supported by the PI5USB2546J. The specific CTL pin changes that the PI5USB2546J will override are shown below. The information is presented as CTL1, CTL2 and CTL3.The ILIM_SEL pin plays no role

1. 111 (CDP/SDP2) to 011 (DCP-Auto)
2. 110/010 (SDP1) to 011 (DCP-Auto)

USB Low-Speed / Full-Speed Device Recognition

PI5USB2546J is capable of detecting LS or FS device attachment when PI5USB2546J is in SDP or CDP mode. Per USB spec when no device is attached, the D+ and D- lines are near ground level. When a low speed compliant device is attached to the PI5USB2546J charging port, D- line will be pulled high in its idle state (mouse/keyboard not activated). However when a FS device is attached the opposite is true in its idle state, i.e. D+ is pulled high and D- remains at ground level.

PI5USB2546J monitors both D+ and D- lines while CTL pin settings are in CDP or SDP mode to detect LS or FS HID device attachment. To support HID sleep wake, PI5USB2546J must first determine that it is attached to a LS or FS device when system is in S0 power state. PI5USB2546J does this as described above. While supporting a LS HID wake is straight forward, supporting FS HID requires making a distinction between a FS and a HS device. This is because a high speed device will always present itself initially as a full speed device (by a 1.5K pull up resistor on D+). The negotiation for high speed then makes the distinction whereby the 1.5K pull up resistor gets removed.

PI5USB2546J handles the distinction between a FS and HS device at connect by memorizing if the D+ line goes low after connect. A HS device after connect will always undergo negotiation for HS which will require the 1.5KΩ resistor pull-up on D+ to be removed. To memorize a FS device, PI5USB2546J requires the device to remain connected for at least 60 sec while system is in S0 mode before placing it in sleep or S3 mode. If system is placed in sleep mode earlier than the 60 sec window, a FS device may not get recognized and hence could fail to wake system from S3. This requirement does not apply for LS device.

No CTL Pin Timing Requirement after Wake Event and Transition from S3 to S0

There is no CTL pin timing requirement for the PI5USB2546J when the wake configured USB device wakes the system from S3 back to S0.

Device Control Pins Truth Table

Device Control Pins Table lists all valid bias combinations for the four control pins CTL1, CTL2, CTL3 and ILIM_SEL pins and their corresponding charging mode. It is important to note that the Device Control Pins Table *purposely* omits matching charging modes of the PI5USB2546J with global power states (S0-S5) as device is agnostic to system power states. The PI5USB2546J monitors its CTL inputs and will transition to whatever charging state it is commanded to go to (except when LS/FS HID device is detected). For example if sleep charging is desired when system is in standby or hibernate state then user must set PI5USB2546J control pins to correspond to DCP_Auto charging mode per below table. When system is put back to operation mode then set control pins to correspond to SDP or CDP mode and so on.

PI5USB2546J Device Control Pins Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	/STATUS Output (Active low)	Comment
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	I_{OS_PW} & ILIM_HI(1)	DCP load present(2)	Data lines disconnected and load detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP load present(3)	Data lines disconnected and load detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	
1	0	1	0	Divider-1A	ILIM_LO	OFF	Device forced to stay in Divider-1A charging mode
1	0	1	1	Divider-1A	ILIM_HI	OFF	
1	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2(4)	ILIM_LO	OFF	
1	1	1	1	CDP(4)	ILIM_HI	CDP load present(5)	Data lines connected and load detect active

Note:

(1) PI5USB2546J: Current limit (IOS) is automatically switched between IOS_PW and the value set by ILIM_HI according to the Load Detect –Power Wake functionality.

(2) DCP Load present governed by the "Load Detection – Power Wake" limits.

(3) DCP Load present governed by the "Load Detection – Non Power Wake" limits.

(4) No OUT discharge when changing between 1111 and 1110.

(5) CDP Load present governed by the "Load Detection – Non Power Wake" limits and BC1.2 primary detection.

Below tables can be used as an aid to program the PI5USB2546J per system states however not restricted to below settings only.

PI5USB2546J Control Pin Setting Matched to System Power States

System Global Power State	Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP1	1	1	0	1 or 0	ILIM_HI/ILIM_LO
S0	SDP2, no discharge to/from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 25mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds	0	0	1	1	ILIM_HI
S3/S4/S5	Auto mode, no load detection	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake up, load detection with ILIM_LO + 25mA thresholds	0	1	1	1	ILIM_HI
S3	Auto mode, keyboard/mouse wake up, no load detection	0	1	1	0	ILIM_HI
S3	SDP1, keyboard/mouse wake up	0	1	0	1 or 0	ILIM_HI/ILIM_LO

Load Detect

PI5USB2546J offer system designers unique power management strategy not available in the industry from similar devices. There are two power management schemes supported by the PI5USB2546J via the /STATUS pin, they are:

1. Power Wake (PW)
2. Port Power Management (PPM)

Either feature may be implemented in a system depending on power savings goals for the system. In general Power Wake feature is used mainly in mobile systems like a notebook where it is imperative to save battery power when system is in deep sleep (S4/S5) state. On the other hand Port Power Management feature would be implemented where multiple charging ports are supported in the same system and system power rating is not capable of supporting high current charging on multiple ports simultaneously.

Power Wake

Goal of power wake feature is to save system power when system is in S4/S5 state. In S4/S5 state system is in deep sleep and typically running of the battery; so every “mW” in system power savings will translate to extending battery life. In this state the PI5USB2546J will monitor charging current at the OUT pin and provide a mechanism via the /STATUS pin to switch out the high power DC-DC controller and switch in a low power LDO when charging current requirement is <45mA (typ.). This would be the case when no peripheral device is connected at the charging port or if a device has attained its full battery charge and draws <45mA. Power wake flow chart and description is shown as Figure 6.

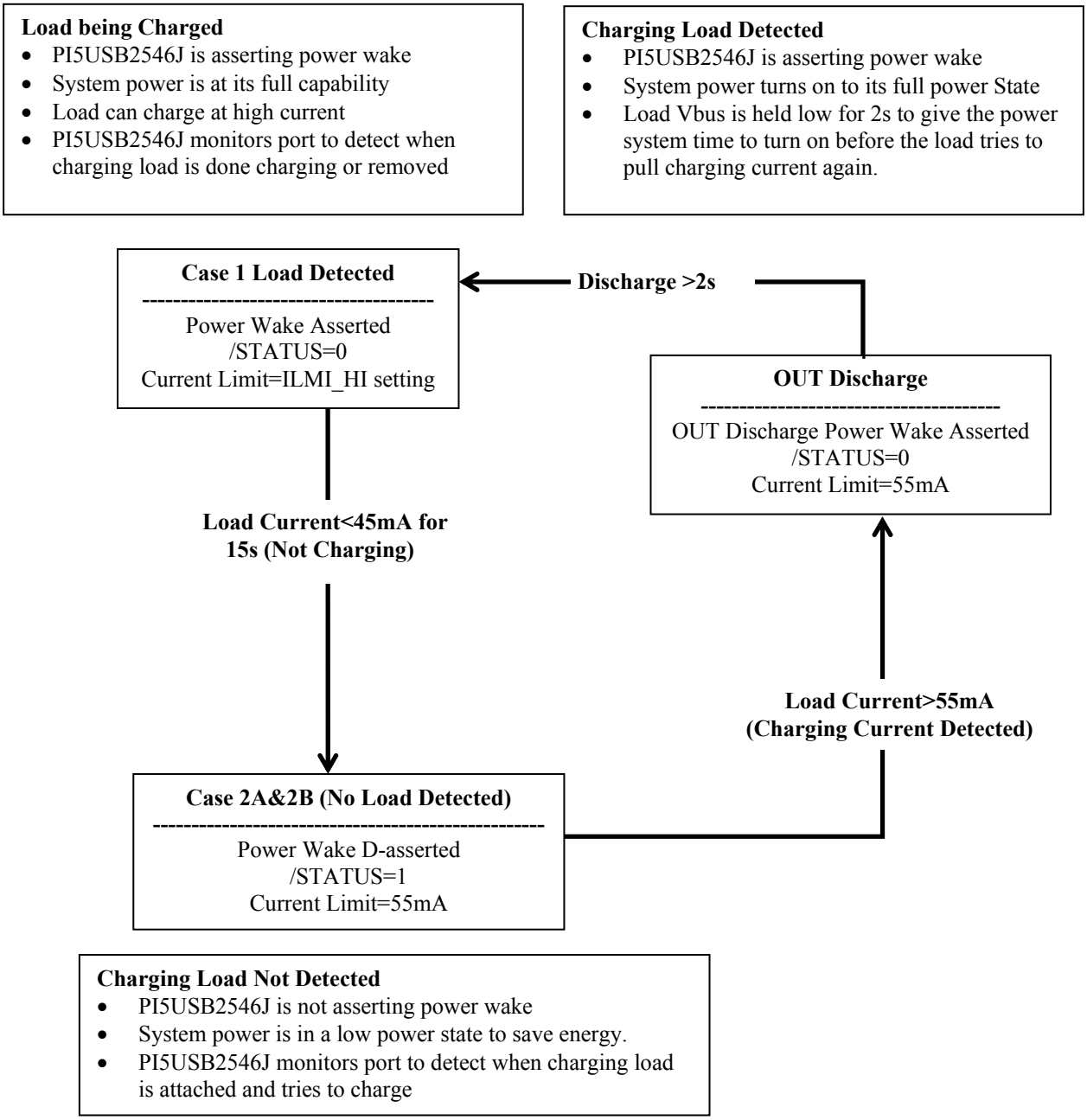


Figure 6. Power Wake flow chart

Implementing Power Wake in Notebook System

An implementation of power wake in notebook platforms with the PI5USB2546J is shown as below. Power wake function is used to select between a high power DC-DC converter and low power LDO (100mA) based on charging requirements. System power saving is achieved when under no charging conditions (the connected device is fully charged or no device is connected) the DC-DC converter is turned-off (to save power since it is less efficient in low power operating region) and the low power LDO supplies standby power to the charging port.

Power wake is activated in S4/S5 mode (0011 setting, see device truth table), PI5USB2546J is charging connected device as shown as case 1, /STATUS is pulled LOW (Case 1) which switches-out the LDO and switches-in the DC-DC converter to handle high current charging.

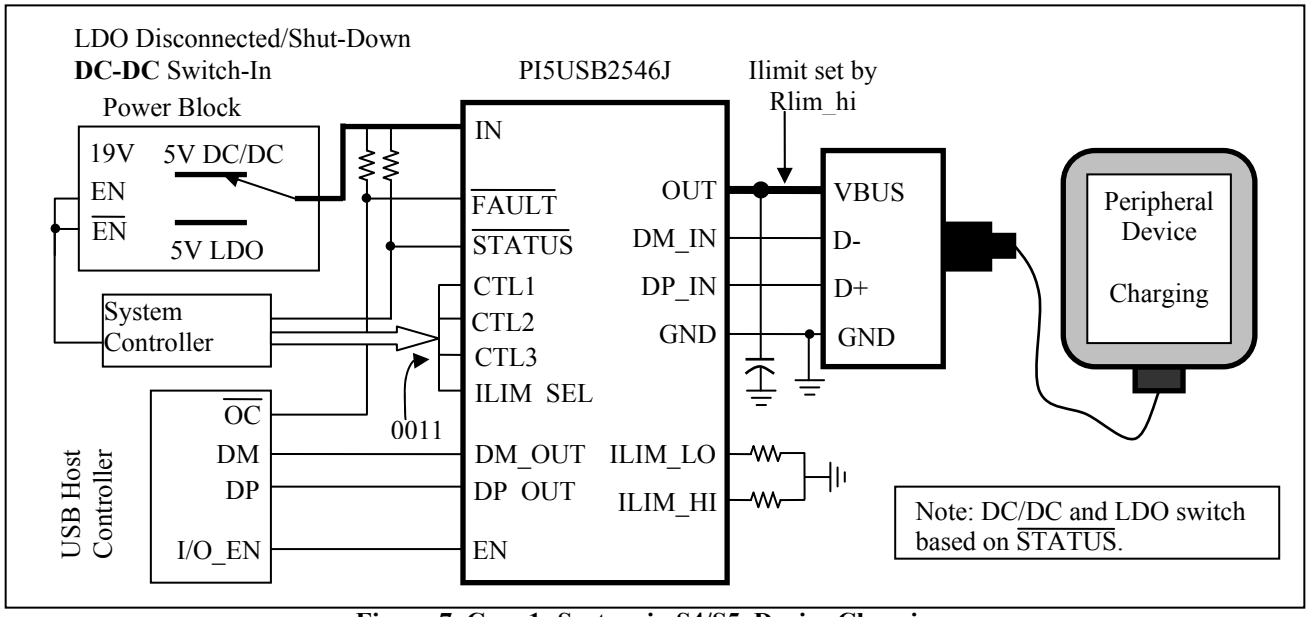


Figure 7. Case 1: System in S4/S5, Device Charging

As shown in Case 2A (Figure 8) and Case 2B (Figure 9), when connected device is fully charged or gets disconnected from the charging port, the charging current will fall. If charging current falls to <45mA and stays below this threshold for over 15s, PI5USB2546J automatically sets a 55mA internal current limit and /STATUS is de-asserted (pulled HI). As shown in Case 2A and Case 2B. This results in DC-DC converter turning off and the LDO turning on. Current limit of 55mA is set to prevent the low power LDO output voltage from collapsing in case there is a spike in current draw due to device attachment or other activity such as display panel LED turning ON in connected device.

Following Power Wake flow chart when a device is attached and draws >55mA of charging current the PI5USB2546J will hit its internal current limit. This will trigger the device to assert /STATUS (LO) and turn on the DC-DC converter and turn off the LDO. PI5USB2546J will discharge OUT for >2s (typ.) to allow the main power supply to turn on. After the discharge the device will turn back on with current limit set by ILIM_HI (Case 1, Figure 7)

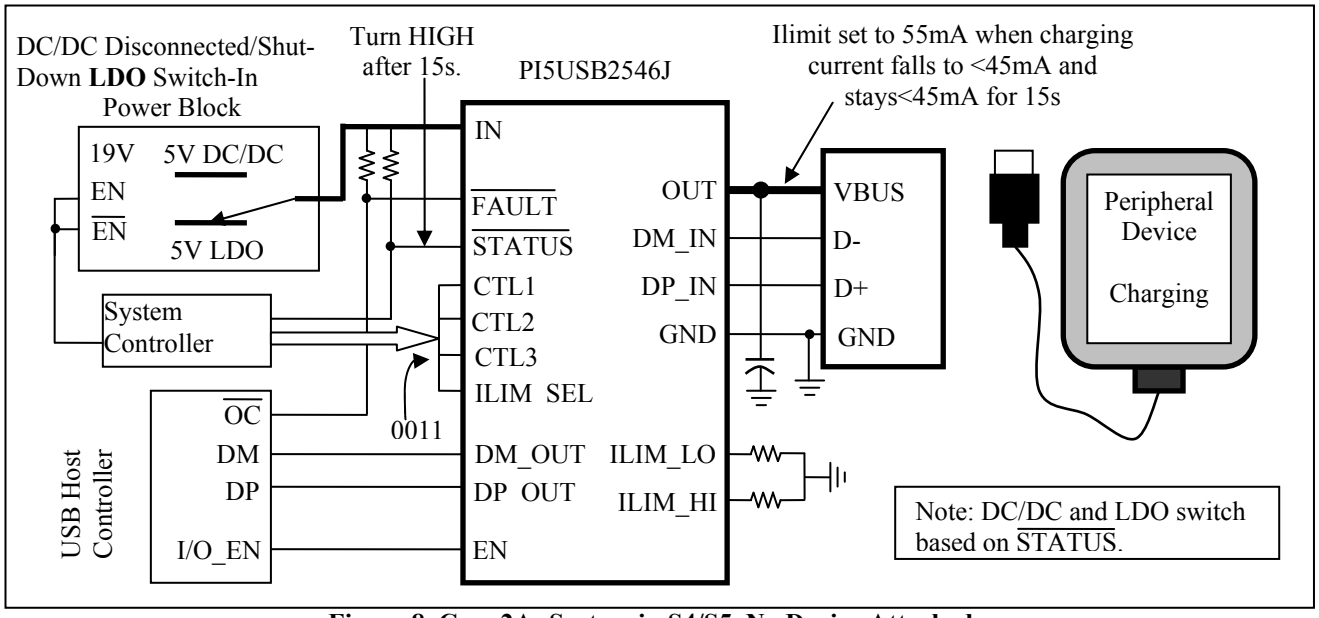


Figure 8. Case 2A: System in S4/S5, No Device Attached

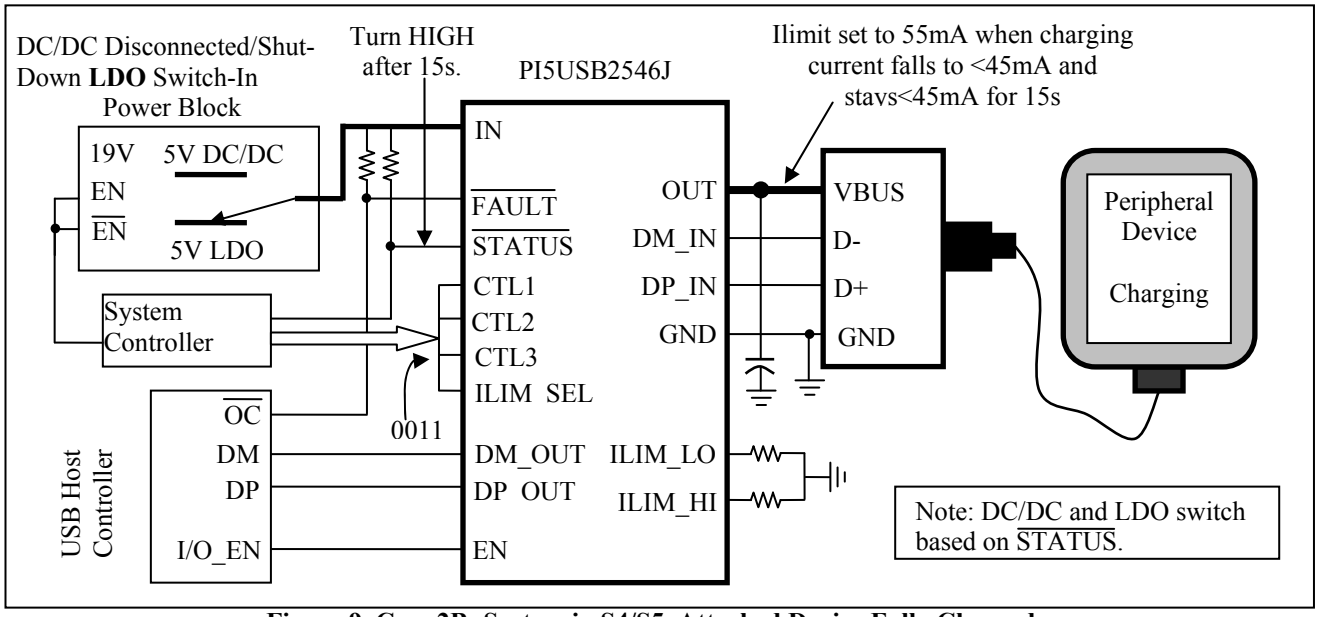


Figure 9. Case 2B: System in S4/S5, Attached Device Fully Charged

Port Power Management (PPM)

PPM is the intelligent and dynamic allocation of power. It is for systems that have multiple charging ports but cannot power them all simultaneously.

Goal of this feature are:

1. Enhances user experience since user does not have to search for charging port
2. Power supply only has to be designed for a reasonable charging load

Initially all ports are allowed to broadcast high current charging, charging current limit is based on ILIM_HI resistor setting. System monitors /STATUS to see when high current loads are present. Once allowed number of ports assert /STATUS, remaining ports are toggled to a non-charging port. Non-charging ports are SDP ports with current limit based on ILIM_LO. PI5USB2546J allows for a system to toggle between charging and non-charging ports either with an OUT discharge or without an OUT discharge.

Benefits of PPM

- Delivers better user experience
- Prevents overloading of system's power supply
- Allows for dynamic power limits based on system state
- Allows every port to potentially be a high power charging port
- Allows for smaller power supply capacity since the loading is controlled

PPM Details

All ports are allowed to broadcast high current charging – CDP or DCP. Current limit is based on ILIM_HI and system monitors /STATUS pin to see when high current loads are present. Once allowed number of ports assert /STATUS, remaining ports are toggled to a SDP non-charging port. SDP current limit is based on ILIM_LO setting. SDP ports are automatically toggled back to CDP or DCP mode when a charging port de-asserts /STATUS.

Based on CTL settings there is a provision for a port to toggle between charging and non-charging ports either with a VBUS discharge or without a VBUS discharge. For example when a port is in SDP2 mode (1110) and its ILIM_SEL pin is toggled to 1 due to another port releasing its high current requirements. The SDP2 port will automatically revert to CDP mode (1111) without a discharge event. This is desirable if this port was connected to a media device where it was syncing data from the SDP2 port; a discharge event would mess-up the syncing activity on the port and cause user confusion.

/STATUS trip point is based on the programmable ILIM_LO current limit set point. This does not mean /STATUS is a current limit – the port itself is using the ILIM_HI current limit. Since ILIM_LO defines the current limit for a SDP port, it works well to use the ILIM_LO value to define a high current load. /STATUS asserts in CDP and DCP when load current is above ILIM_LO+25mA for 200ms. /STATUS de-asserts in CDP and DCP when load current is below ILIM_LO-25mA for 3s.

Implementing PPM in a System with Two Charging Ports

Below shows the implementation of two charging ports and each port with its own PI5USB2546J. In this example 5V power supply for the two charging ports is rated at <3A or <15W max. Both devices have RLIM chosen to correspond to the low (0.9A) and high (1.5A) current limit setting for the port. In this implementation the system can support only one of the two ports at 1.5A charging current while the other port is set to SDP mode and I_{LIMIT} corresponding to 0.9A.

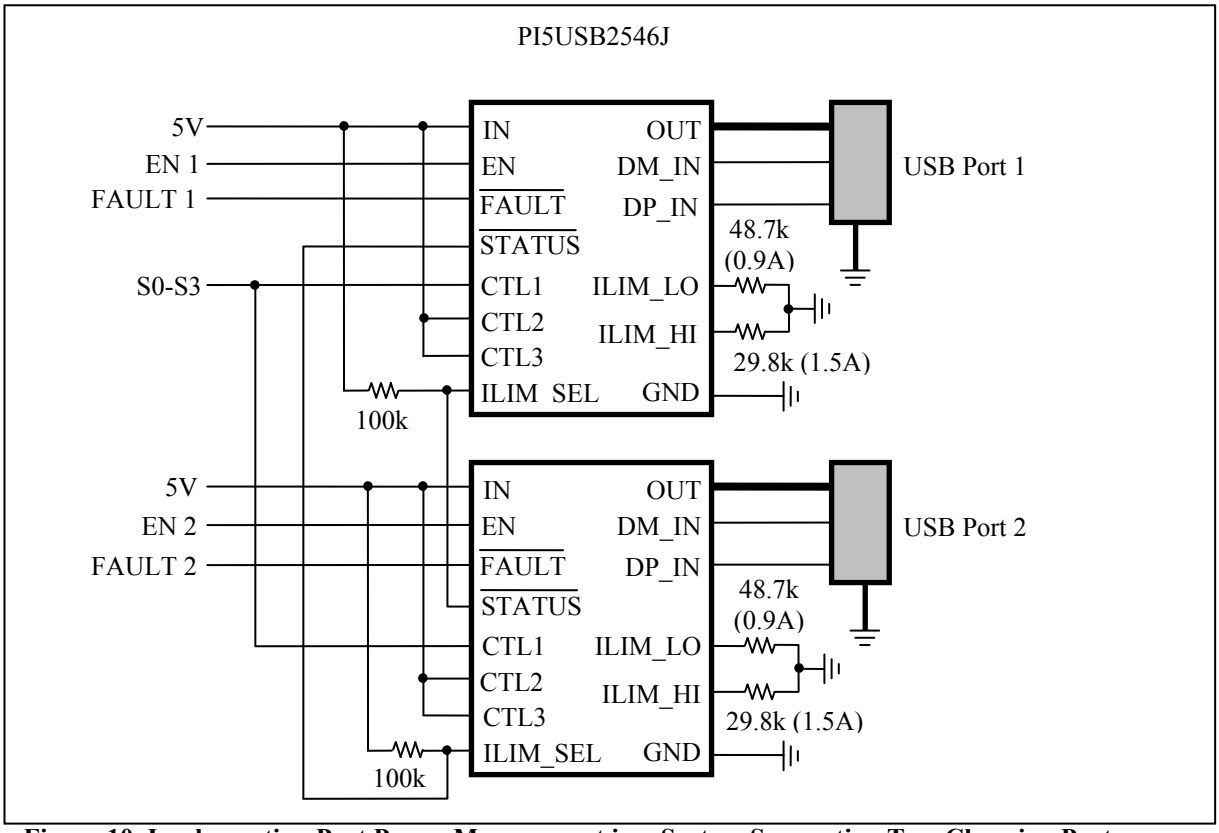


Figure 10. Implementing Port Power Management in a System Supporting Two Charging Ports

Over-Current Protection

When an over-current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before VIN has been applied. The PI5USB2546J senses the short and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for nominally one to two microseconds before the current-limit circuit can react. The device operates in constant-current mode after the current-limit circuit has responded. Complete shutdown occurs only if the fault is presented long enough to activate thermal limiting. The device will remain off until the junction temperature cools approximately 20°C and will then re-start. The device will continue to cycle on/off until the over-current condition is removed.

Current-Limit Settings

The PI5USB2546J has two independent current limit settings that are each programmed externally with a resistor. The ILIM_HI setting is programmed with R_{ILIM_HI} connected between ILIM_HI and GND. The ILIM_LO setting is programmed with R_{ILIM_LO} connected between ILIM_LO and GND. Consult the Device Truth Table to see when each current limit is used. Both settings have the same relation between the current limit and the programming resistor. R_{ILIM_LO} is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:

1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used

The following equation programs the typical current limit:
I_{OS_TYP} (mA)=50250/R_{LIM_xx} (kΩ)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

Many applications require that the current limit meet specific tolerance limits. When designing to these tolerance limits, both the tolerance of the PI5USB2546J current limit and the tolerance of the external programming resistor must be taken into account. The following equations approximate the PI5USB2546J minimum / maximum current limits to within a few mA and are appropriate for design purposes. These equations assume an ideal – no variation - external programming resistor. To take resistor tolerance into account, first determine the minimum /maximum resistor values based on its tolerance specifications and use these values in the equations. Because of the inverse relation between the current limit and the programming resistor, use the maximum resistor value in the I_{OS_MIN} equation and the minimum resistor value in the I_{OS_MAX} equation.

I_{OS_MIN} (mA)=45271/(R_{LIM_xx} (kΩ))$^{0.98437}$-30
I_{OS_MAX} (mA) =55325/ (R_{LIM_xx} (kΩ)) $^{1.0139}$+30

The traces routing the R_{ILIM_XX} resistors should be a sufficiently low resistance as to not affect the current-limit accuracy. The ground connection for the R_{ILIM_XX} resistors is also very important. The resistors need to reference back to the PI5USB2546J GND pin. Follow normal board layout practices to ensure that current flow from other parts of the board does not impact the ground potential between the resistors and the PI5USB2546J GND pin.

/FAULT Response

The /FAULT open-drain output is asserted (active low) when an over-temperature or current limit condition occurs. The PI5USB2546J is designed to eliminate false /FAULT reporting by using an internal deglitch circuit for current limit conditions without the need for external circuitry. This ensures that /FAULT is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. Over-temperature conditions are not deglitched and assert the /FAULT signal immediately.

Under-Voltage Lockout (UVLO)

The under-voltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn on threshold. Built-in hysteresis prevents unwanted oscillations on the output due to input voltage drop from large current surges.

Thermal Sense

The PI5USB2546J protects itself with thermal sensing circuit that monitor the operating temperature of the power distribution switch and disables operation if the temperature exceeds recommended operating conditions. The device operates in constant-current mode during an over-current condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, so the junction temperature rises during an over-current condition. The thermal sensor turns off the power switch when the die temperature exceeds 135°C regardless of whether the power switch is in current limit. Hysteresis is built into thermal sensor, and the switch turns on after the device has cooled by approximately 20°C. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output /FAULT is asserted (active low) when an over-temperature shutdown condition.

Application Information

Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1uF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute-maximum voltage of the device during heavy transient conditions or output shorting. This is especially important during bench testing when long inductive cables are used to connect the evaluation board to the bench power supply. Normally suggested the distance between IC and DC supply is less than 15cm.

Output capacitance also must be close to IC as possible. When large transient currents are expected on the output， placing a high-value electrolytic capacitor on the output pin is recommended,

Layout Design Guideline

1. The PCB is suggested to use at least 4 layers
2. The high speed differential pair should be maintain 90Ω
3. Do not route the high speed signal over any split plane
4. Minimized the number of vias and corners on the high speed trace for reducing the signal reflections and impedance changes
5. If it's necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This can reduces reflections on the signal by minimizing impedance discontinuities.
6. The high speed trace should be routed symmetrically and parallelism (including the test points on the high speed trace). The non-parallelism trace will cause the impedance discontinuities and affect the signal quality
7. Avoid any unnecessary stubs on the differential pair. The stubs will introduce the signal reflections which affect the signal quality
8. Avoid routing the high speed differential pair under the crystal, oscillator, clock synthesizer, magnetic devices or ICs to cause the interference.
9. Avoid anti-etch on the GND plane

Part Marking

ZHD Package

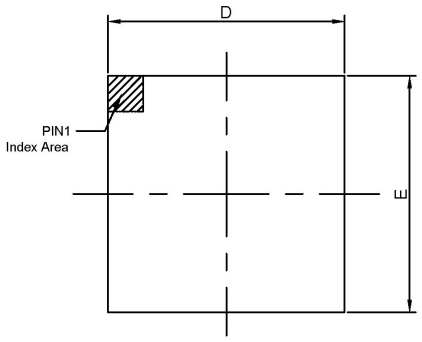
xPZHDE: PI5USB2546JZHDE
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code
Bar above 2nd “X” means Cu wire

ZH Package

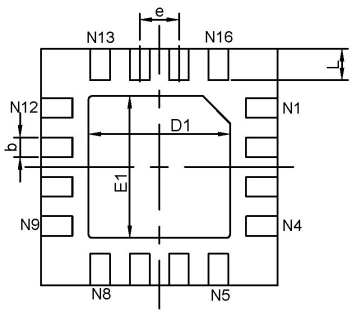
xPZHE: PI5USB2546JZHE
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code
Bar above 2nd “X” means Cu wire

Packaging Mechanical

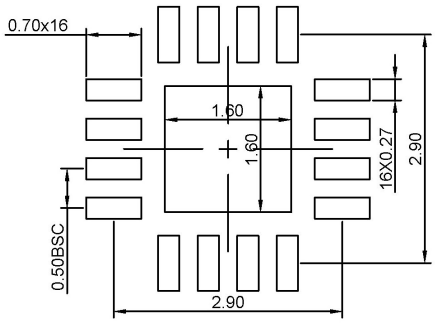
16-UQFN (ZHD)



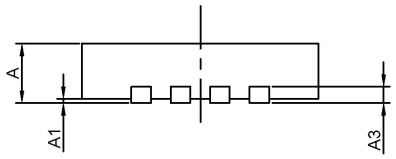
Top View



Bottom View



RECOMMENDED LAND PATTERN(unit:mm)



Side View

PKG. DIMENSIONS(MM)			
SYMBOL	Min	Nom	Max
A	0.55	0.60	0.65
A1	0.00	0.02	0.05
A3		0.15 REF	
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	1.60	1.75	1.90
E1	1.60	1.75	1.90
b	0.18	0.24	0.30
e		0.50 BSC	
L	0.25	0.40	0.55

Note:

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

DATE: 04/22/20

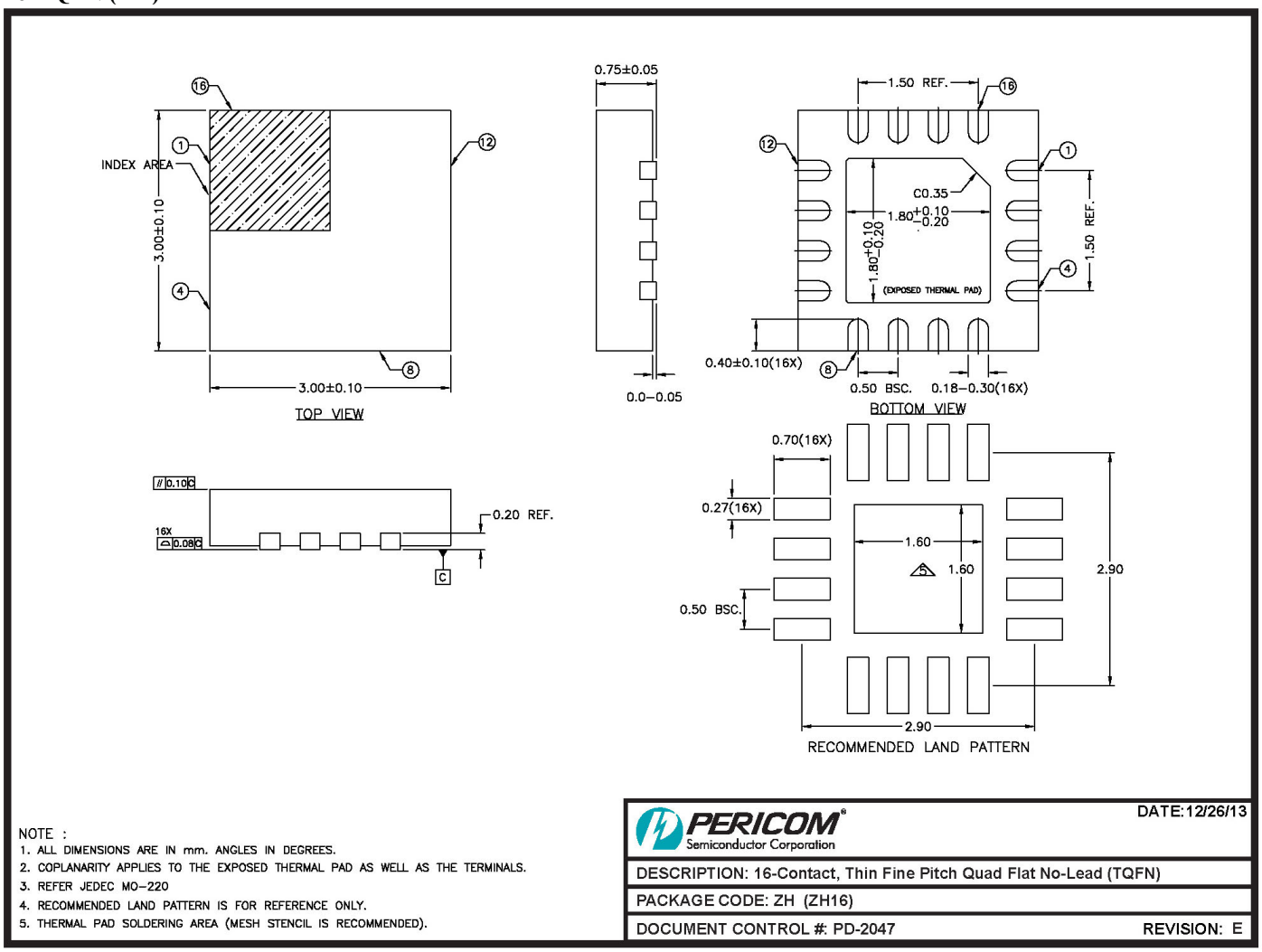
DESCRIPTION: 16-Pin, UQFN, 3X3 (U-QFN3030-16)

PACKAGE CODE: ZHD(ZHD16)

DOCUMENT CONTROL#: PD-2209 REVISION: A

20-1248

16-TQFN (ZH)



14-0244

For latest package info.
please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part Numbers	Package Code	Package Description
PI5USB2546JZHDEX	ZHD	16-pin, 3x3 (UQFN)
PI5USB2546JZHEX	ZH	16-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or

2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

www.diodes.com

单击下面可查看定价，库存，交付和生命周期等信息

>>Diodes Incorporated(达迩科技（美台）)