10Gbps, 2-Port, USB 3.1 Mux/Demux ReDriver™

Features

ReDriver

- 10Gbps Serial Link with Linear Equalizer
- Full Compliancy to USB 3.1 Gen-2 and Gen-1 Super-Speed Standard
- 1-to-2 DeMux from Host Tx to Device Rx
- 2-to-1 Mux from Device Tx to Host Rx
- Adjustable-Output Linear Swing, Flat Gain and Equalization via I2C or Pin Control
- 100Ω Differential CML I/Os
- Automatic Receiver Detect
- Auto "Slumber" Mode for Adaptive Power Management
- Supply Voltage 3.3V
- Temperature Range: -40°C to 70°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Packaging (Pb-free & Green):
  - 40-contact, ZLC40 (TQFN)

Applications

- Notebooks
- Mobile Phones
- Tablets
- Docking Station

Description

PI3EQX10612 is a low-power, high-performance 10Gbps 2-Port USB 3.1 Gen-2/Gen-1 Mux/DeMux ReDriver.

The Two-Port Mux/Demux ReDriver

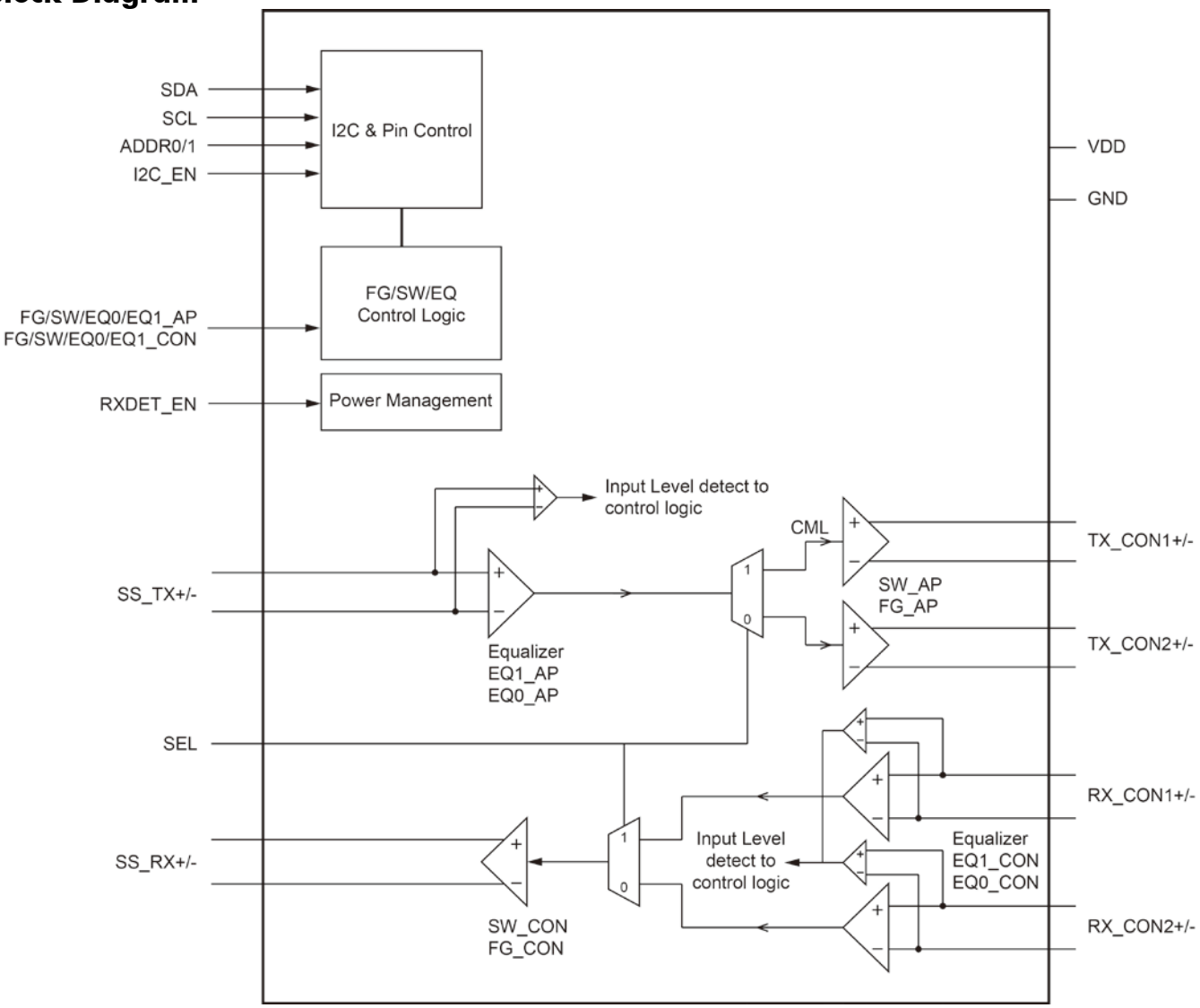
The ReDriver provides programmable equalization, swing, and flat gain to optimize performance over a variety of physical mediums by reducing intersymbol interference. The ReDriver supports two 100Ω differential CML data I/Os between the Protocol ASIC to a switch fabric, overcable, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver. A low-level input-signal detection and output-squelch function is provided for each channel. Each channel operates fully independently. The channels' input-signal level determines whether the output is active.

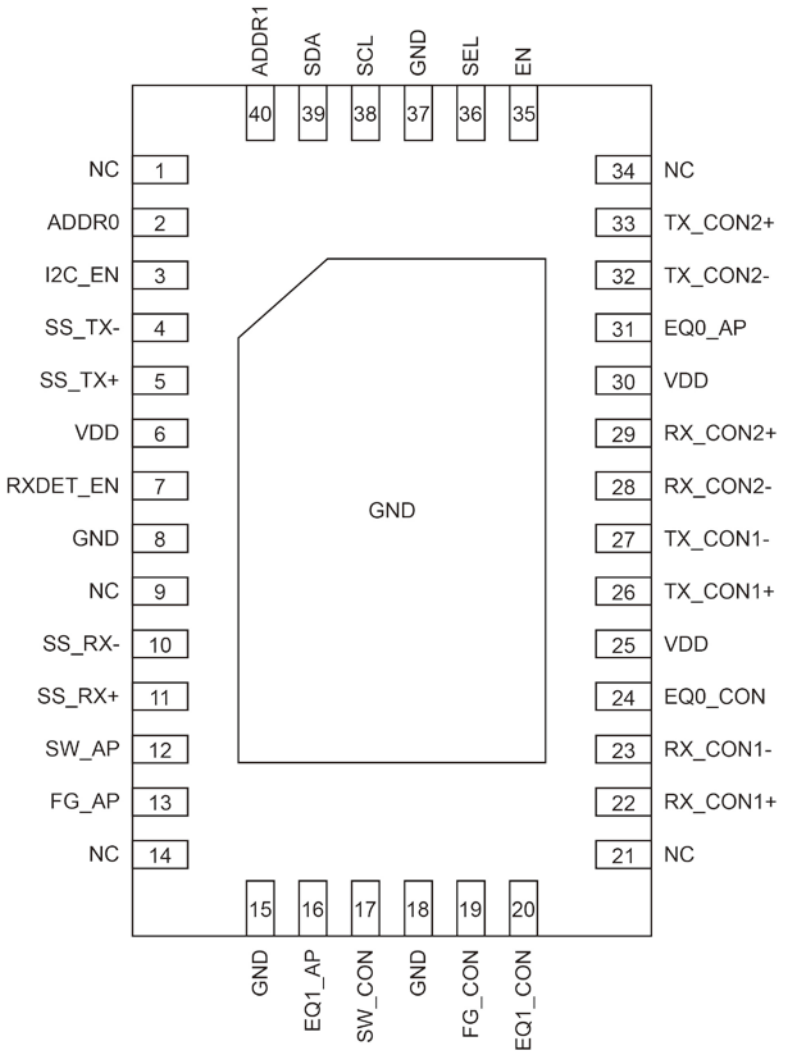
The ReDriver also includes an adaptive power management feature to maximize battery life for power-sensitive consumer devices.

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Block Diagram



Pin Configuration



Pin Descriptions

Pin #	Pin Name	I/O	Description
Thermal PAD, 8, 15,18,37	GND	Ground	Ground pin. Thermal pad.
2, 40	ADDR0, ADDR1	I	Input pins to indicate I2C address: Refer to *I2C Slave Address* table.
3	I2C_EN	I	Input pin to enable I2C mode
5,4 22,23 29,28	SS_TX+, SS_TX-, RX_CON1+, RX_CON1-, RX_CON2+, RX_CON2-	I	Input terminals. Selectable input termination between 50Ω to VDD, 75kΩ to VbiasRX, or 75kΩ to GND.
6,25,30	VDD	Power	Dedicated 3.3V power supply.
7	RXDET_EN	I	ReDriver loading detection enable pin. 1 = ReDriver loading detection enabled (default setting in application) 0 = ReDriver loading detection disabled
11,10 26,27 33,32	SS_RX+,SS_RX-, TX_CON1+,TX_CON1-, TX_CON2+, TX_CON2-	O	Output terminals. Selectable output termination between 50Ω to VbiasTx, 6kΩ to VbiasTx, 75kΩ to VbiasTx, and 75kΩ to GND.
12,13,16,31	SW_AP FG_AP EQ1_AP, EQ0_AP	I	SW/FG/EQ setup for USB channels with receiver terminal is connected to AP side.
17,19,20,24	SW_CON FG_CON EQ1_CON, EQ0_CON	I	SW/FG/EQ setup for USB channels with receiver terminal is connected to connector side.
35	EN	I	Active-high enable input pin (with internal weak pull high). EN=GND — disabled/low power state EN=VDD — enabled/active state
36	SEL	I	Input pin to select USB channel.
38	SCL	I	I2C communication clk signal.
39	SDA	I/O	I2C communication data signal.
1,9,14,21,34	NC	—	No connection.

Maximum Ratings

Storage Temperature	-65 to 150	℃
Supply Voltage	-0.5 to 3.8	V
Voltage of 3.3V IO pins (SCL, SDA, RXDET_EN, ADDR0/1, SEL, EN, SW_AP,FG_AP,EQ1_AP, EQ0_AP,SW_CON,FG_CON,EQ1_CON,EQ0_CON)	-0.5 to VDD+0.5	V
Voltage of SS_TX+/-,SS_RX+/-,TX_CON1/2 +/-, RX_CON1/2 +/-	-0.5 to VDD+0.5	V
Sink Current from SDA	10	mA
Continuous Input Current to SS_TX+/-, RX_CON1/2 +/-	±30	mA
ESD (HBM)	2	KV

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply Voltage	3.0	3.6	V
V_{IO}	Voltage of IO pins (SCL, SDA, RXDET_EN, ADDR0/1, SEL, EN, SW_AP,FG_AP, EQ1_AP, EQ0_AP,SW_CON,FG_CON, EQ1_CON,EQ0_CON)	0	3.6	V
V_{TXRX}	Voltage of SS_TX+/-,SS_RX+/-,TX_CON1/2 +/-, RX_CON1/2 +/-	0	3.6	V
V_{NOISE}	Supply Noise up to 50MHz	—	100	mVpp
T_A	Operating Temperature	-40	70	°C

ReDriver AC/DC Electrical Characteristics

Power Consumption (VDD)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{PD}	Typical Pin Power-Down Current	EN=0	—	26	100	µA
I_{DDQ_PD}	I2C Power-Down Current	EN=1 I2C Byte4<7:4>=1111	—	—	340	µA
USB 3.1 Gen 2 Mode						
I_{U0}	Current in USB U0 Mode	EN=1, USB U0 mode	—	80	112	mA
I_{U1}	Current in USB U1 Mode	EN=1, USB U1 mode	—	16	20	mA
$I_{U2/U3}$	Current in USB U2/U3 Mode	EN=1, USB U2/U3 mode	—	0.5	0.6	mA
I_{RXDET}	Current RXDET Mode	EN=1, RXDET mode	—	0.5	0.6	mA
Four-Level Control Pins (FG_AP, FG_CON, EQ1_AP, EQ0_AP, EQ1_CON,EQ0_CON, SW_AP, SW_CON)						
V_{IH}	DC-Input Logic High	—	0.92 × VDD	VDD	—	V
V_{IF}	DC-Input Logic “Float”	—	0.59 × VDD	0.67 × VDD	0.75 × VDD	V
V_{IR}	DC-Input Logic with Rext to GND	—	0.25 × VDD	0.33 × VDD	0.41 × VDD	V
V_{IL}	DC-Input Logic Low	—	—	GND	0.08 × VDD	V
I_{IH}	Input-High Current	—	—	—	50	µA
I_{IL}	Input-Low Current	—	-75	—	—	µA
Rext	External Resistance Connects to GND (±5%)	—	64.6	68	71.4	kΩ
Two-Level Control Pins (EN, SEL, ADDR0/1, RXDET_EN)						
V_{IH}	DC-Input Logic High	—	2.0	—	—	V
V_{IL}	DC-Input Logic Low	—	—	—	0.8	V
I_{IH}	Input-High Current	—	—	—	25	µA
I_{IL}	Input-Low Current	—	-25	—	—	µA
I2C Interface Pins (SCL, SDA)						
V_{IH}	DC-Input Logic High	—	1.1	—	—	V
V_{IL}	DC-Input Logic Low	—	—	—	0.4	V

USB Differential Channel

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
USB Differential Input						
$C_{RXPARASITIC}$	Parasitic Capacitor for RX	—	—	—	1.0	pF
$R_{RX-DIFF-DC}$	DC Differential Input Impedance	—	72	—	120	Ω
$R_{RX-SINGLE-DC}$	DC Single-ended Input Impedance	DC impedance limits are required to guarantee RxDet. Measured with respect to GND over a voltage of 500mV max.	18	—	30	Ω
$Z_{RX-HIZ-DC-PD}$	DC Input CM Input Impedance for V>0 During Reset or Power Down	(Vcm=0 to 500mV)	25	—	—	kΩ
$C_{AC\_COUPLING}$	AC-Coupling Capacitance	—	75	—	265	nF
$V_{RX-CM-AC-P}$	Common-Mode Peak Voltage	AV up to 5GHz	—	—	150	mVpeak
$V_{RX-CM-DC-Active-Idle-Delta-P}$	Common-Mode Peak Voltage	Between U0 and U1, Ac up to 5GHz	—	—	200	mVpeak
USB Differential Output						
$V_{TX-DIFF-PP}$	Output Differential p-p Voltage Swing	Differential Swing $\lvert V_{TX-D+}-V_{TX-D-}\rvert$	—	—	1.2	Vppd
$R_{TX-DIFF-DC}$	DC Differential TX Impedance	—	72	—	120	Ω
$V_{TX-RCV-DET}$	Amount of Voltage Change Allowed During RxDet	—	—	—	600	mV

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$C_{ac\_coupling}$	AC-Coupling Capacitance	—	75	—	265	nF
$T_{TX-EYE(10Gbps)}$	Transmitter eye, Include all Jitter	At the silicon pad, 10Gbps	0.646	—		UI
$T_{TX-EYE(5Gbps)}$	Transmitter eye, Include all jitter	At the silicon pad, 5Gbps	0.625	—		UI
$T_{TX-DJ-DD(10Gbps)}$	Transmitter Deterministic Jitter	At the silicon pad, 10Gbps	—	—	0.17	UI
$T_{TX-DJ-DD(5Gbps)}$	Transmitter Deterministic Jitter	At the silicon pad, 5Gbps	—	—	0.205	UI
$C_{TXPARASITIC}$	Parasitic Capacitor for TX	—	—	—	1.1	pF
$R_{TX-DC-CM}$	Common Mode DC Output Impedance	—	18	—	30	Ω
$V_{TX-DC-CM}$	Instantaneous-Allowed DC Common-Mode Voltage at the Connector Side of the AC-Coupling Capacitors	$\|V_{TX-D+}+V_{TX-D-}\|/2$	0	—	2.2	V
V_{TX-C}	Common-Mode Voltage	$\|V_{TX-D+}+V_{TX-D-}\|/2$	VDD-2	—	VDD	V
$V_{TX-CM-AC-PP-Active}$	Active-Mode TX AC Common-Mode Voltage	$V_{TX-D+}+V_{TX-D-}$ for both time and amplitude	—	—	100	mVpp
$V_{TX-CM-DC-Active\_Idle-Delta}$	Common-Mode Delta Voltage $\|Avg_{uo}(\|V_{TEX-D+} + V_{TX-D-}\|)/2 - Avg_{u1}(\|V_{TX-D+} + V_{TX-D-}\|)/2\|$	Between U0 to U1	—	—	200	mV-peak
$V_{TX-Idle-Diff-AC-pp}$	Idle-Mode AC Common-Mode Delta Voltage $\|V_{TX-D+}-V_{TX-D-}\|$	Between Tx+ and Tx- in idle mode. Use the HPF to remove DC components. =1/LPF. No AC and DC signals are applied to Rx terminals.	—	—	10	mVppd
$V_{TX-Idle-Diff-DC}$	Idle-Mode DC Common-Mode Delta Voltage $\|V_{TX-D+}-V_{TX-D-}\|$	Between Tx+ and Tx- in idle mode. Use the LPF to remove DC components. =1/HPF. No AC and DC signals are applied to Rx terminals.	—	—	10	mV
G_p	Peaking Gain (Compensation at 5GHz, Relative to 100MHz, 100mV_{p-p} Sine Wave Input)	EQ<3:0>=0000 EQ<3:0>=0101 EQ<3:0>=1010 EQ<3:0>=1111	—	6.42 9.5 11.77 13.54	—	dB
		Variation around typical	-3	—	+3	dB
G_F	Flat Gain (100MHz, EQ<3:0>=0000, SW<1:0>=01)	FG<1:0>=00 FG<1:0>=01 FG<1:0>=10 FG<1:0>=11	—	-2.07 -0.24 +0.62 +1.77	—	dB
		Variation around typical	-3	—	+3	dB
V_{SW_100M}	-1dB Compression Point Output Swing (at 100MHz)	SW<1:0>=00 SW<1:0>=01	—	900 1000	—	mVppd
V_{SW_5G}	-1dB Compression Point Output Swing (at 5GHz)	SW<1:0>=00 SW<1:0>=01	—	600 750	—	mVppd
DD_{NEXT} Note3	Differential Near-End Crosstalk	100MHz to 5GHz	—	-45	—	dB
DD_{FEXT} Note3	Differential Far-End Crosstalk	100MHz to 5GHz	—	-45	—	dB
$V_{NOISE-INPUT}$	Input-Referred Noise(2)	100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=0000, SW<1:0>=01	—	0.6	—	mV_{RMS}
		100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=1111, SW<1:0>=01	—	0.5	—	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{NOISE-OUTPUT}$	Output-Referred Noise(2)	100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=0000, SW<1:0>=01	—	0.8	—	mV_{RMS}
		100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=1111, SW<1:0>=01	—	1	—	mV_{RMS}
S11	Input-Return Loss	10 MHz to 4.1 GHz differential	—	-13.0	—	dB
		1 GHz to 4.1 GHz common mode	—	-5.0	—	dB
S22	Output-Return Loss	10 MHz to 4.1 GHz differential	—	-15	—	dB
		1 GHz to 4.1 GHz common mode	—	-6.0	—	dB
Signal and Frequency Detectors						
V_{TH_UPM}	Unplug-Mode Detector Threshold	Threshold of LFPS when the input impedance of the ReDriver is 67kΩ to VbiasRx only. Used in the unplug mode.	200	—	800	mVppd
V_{TH_DSM}	Deep-Slumber Mode Detector Threshold	LFPS signal threshold in deep-slumber mode	100	—	600	mVppd
V_{TH_AM}	Active-Mode Detector Threshold	Signal threshold in active and slumber mode	65	—	175	mVppd
F_{TH}	LFPS Frequency Detector	Detect the frequency of the input CLK pattern	100	—	400	MHz
T_{ON_UPM}	Turn-on of Unplug Mode	TX pin-to-RX pin latency when input signal is LFPS	—	—	3	ms
T_{ON_DSM}	Turn-on of Deep Slumber Mode		—	—	5	µs
T_{ON_SM}	Turn-on of Slumber Mode		—	—	20	ns

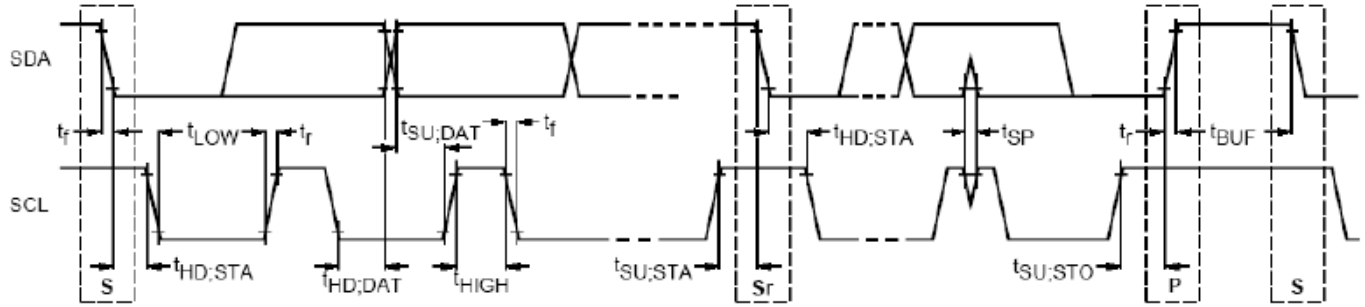
Note:
1. Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
2. Guaranteed by design and characterization.
3. Subtract the Channel Gain from the Total Gain to get the Actual Crosstalk.

I²C AC Electrical Characteristics

Symbol	Parameter	Standard Mode I²C		Fast Mode I²C		Fast Mode Plus I²C		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0	100	0	400	0	1000	kHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	4.7	—	1.3	—	0.5	—	µs
$t_{HD;STA}$	Hold Time (Repeated) START Condition	4.0	—	0.6	—	0.26	—	µs
$t_{SU;STA}$	Setup Time for a Repeated START Condition	4.7	—	0.6	—	0.26	—	µs
$t_{SU;STO}$	Setup Time for STOP Condition	4.0	—	0.6	—	0.26	—	µs
$t_{VD;ACK}$ [1]	Data Valid Acknowledge Time	—	3.45	—	0.9	—	0.45	µs
$t_{HD;DAT}$ [2]	Data Hold Time	0	—	0	—	0	—	ns
$t_{VD;DAT}$	Data Valid Time	—	3.45	—	0.9	—	0.45	ns
$t_{SU;DAT}$	Data Setup Time	250	—	100	—	50	—	ns
t_{LOW}	LOW Period of the SCL Clock	4.7	—	1.3	—	0.5	—	µs
t_{HIGH}	HIGH Period of the SCL Clock	4.0	—	0.6	—	0.26	—	µs
t_f	Fall Time of Both SDA and SCL Signals	—	300	—	300	—	120	ns
t_r	Rise Time of Both SDA and SCL Signals	—	1000	—	300	—	120	ns
t_{SP}	Pulse Width of Spikes that must be Suppressed by the Input Filter	—	50	—	50	—	50	ns

Notes:

1. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SETDAT} \geq 250ns$ must be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr_max + t_{SETDAT} = 1000 + 250 = 1250ns (according to the standard-mode I²C bus specification) before the SCL line is released.
2. C_b equals the total capacitance of one BUS line in pF. If mixed with high-speed devices, faster fall times are allowed according to the I²C specification.

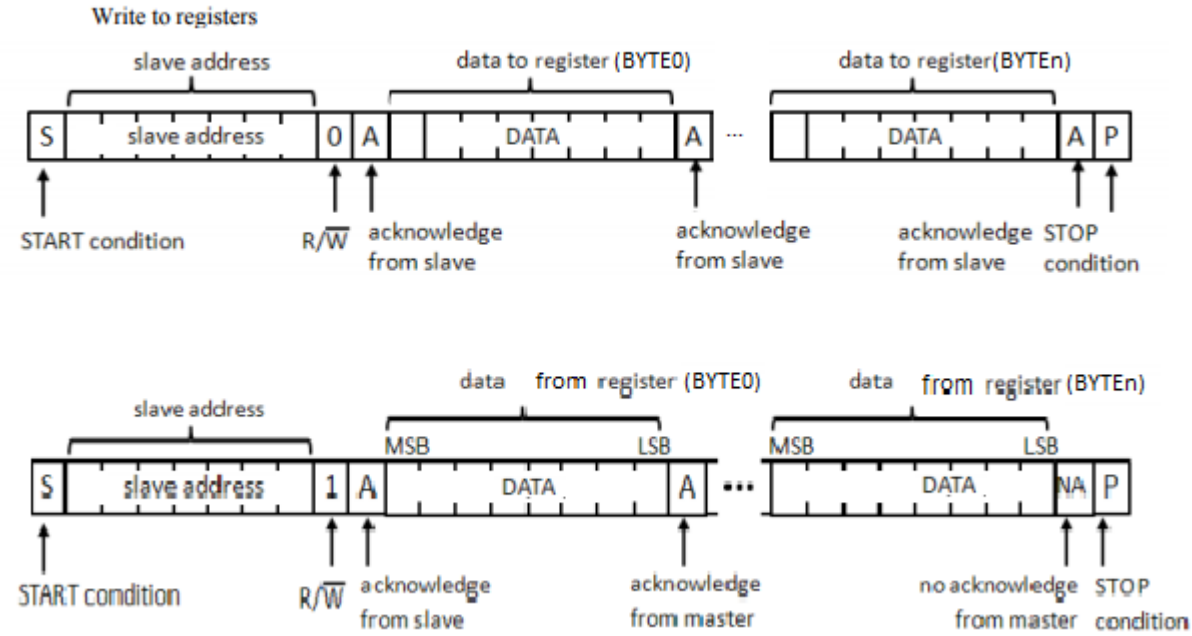


Definition of Timing for Full-Speed Mode Devices on the I²C Bus

I²C Slave Address

I2C_EN	ADDR1	ADDR0	RedriverI2C Slave Address
VDD	GND	GND	A0h
VDD	GND	VDD	A2h
VDD	VDD	GND	A4h
VDD	VDD	VDD	A6h
GND	X	X	Pin Mode

I²C Data Transfer



***Registers of ReDriver can be Read/Written in Bulk Mode only**

ReDriver Detailed Description

ReDriver Register Table

Register Assignment				
BYTE 0 (Revision and Vendor ID Register)				
Bit	**Type**	**Power-up Condition**	**Control Affected**	**Comment**
7	RO	0	Revision ID	Rev# = 0000
6	RO	0		
5	RO	0		
4	RO	0		
3	RO	0	Vendor ID	Pericom ID = 0011
2	RO	0		
1	RO	1		
0	RO	1		
BYTE 1 (Device Type/ Device ID Register)				
Bit	**Type**	**Power-up Condition**	**Control Affected**	**Comment**
7	RO	0	Device Type	Device Type 0000 = Passive MUX 0001 = Active MUX
6	RO	0		
5	RO	0		
4	RO	1		
3	RO	0	Device ID	Device ID = 0001
2	RO	0		
1	RO	0		
0	RO	1		
BYTE 2 (Byte count Register 32 Bytes)				
Bit	**Type**	**Power-up Condition**	**Control Affected**	**Comment**
7	RO	0	Register Byte count	I2C byte count = 32 bytes
6	RO	0		
5	RO	1		
4	RO	0		
3	RO	0		
2	RO	0		
1	RO	0		
0	RO	0		
BYTE 3 (Channel Assignment and Receiver Detection Enable Control)				
Bit	**Type**	**Power-up Condition**	**Control Affected**	**Comment**
7	R/W	0	—	Reserved
6	R/W	1	CONF<2>	Channel Assignment
5	R/W	0	CONF<1>	
4	R/W	1	CONF<0>	
3	R/W	0	—	Reserved
2	R/W	0 if RXDET_EN pin=1; 1 if RXDET_EN pin=0	RXDET_EN#	Far-end receiver detection enable/disable 0 = Enable 1 = Disable
1	R/W	1	—	Reserved
0	R/W	0	—	Reserved
BYTE 4 (Power Down Control)				
Bit	**Type**	**Power-up Condition**	**Control Affected**	**Comment**
7	R/W	0	PD_CON_Rx1	CONx power override 0 – Normal operation 1 – Force the CONx to power-down state
6	R/W	0	PD_CON_Tx1	
5	R/W	0	PD_CON_Tx2	
4	R/W	0	PD_CON_Rx2	
3	R/W	0	—	Reserved
2	R/W	0	—	Reserved
1	R/W	0	—	Reserved
0	R/W	0	—	Reserved

BYTE 5 (Equalization, Flat Gain and -1dB Linear Swing Setting of CON_Rx2)				
Bit	**Type**	**Power-up Condition**	**Control Affected**	**Comment**
7	R/W	0	EQ_CON<3>	CON_Rx2 setting configuration Equalizer Flat Gain Swing
6	R/W	0	EQ_CON<2>	
5	R/W	0	EQ_CON<1>	
4	R/W	0	EQ_CON<0>	
3	R/W	0	FG_CON<1>	
2	R/W	1	FG_CON<0>	
1	R/W	0	SW_CON<1>	
0	R/W	1	SW_CON<0>	
BYTE 6 (Equalization, Flat Gain, and -1dB Linear Swing Setting of AP_Tx2)				
Bit	**Type**	**Power-up Condition**	**Control Affected**	**Comment**
7	R/W	0	EQ_AP<3>	CON_Tx2 setting configuration Equalizer Flat Gain Swing
6	R/W	0	EQ_AP<2>	
5	R/W	0	EQ_AP<1>	
4	R/W	0	EQ_AP<0>	
3	R/W	0	FG_AP<1>	
2	R/W	1	FG_AP<0>	
1	R/W	0	SW_AP<1>	
0	R/W	1	SW_AP<0>	
BYTE 7 (Equalization, Flat Gain, and -1dB Linear Swing Setting of AP_Tx1)				
Bit	**Type**	**Power-up Condition**	**Control Affected**	**Comment**
7	R/W	0	EQ_AP<3>	CON_Tx1 setting configuration Equalizer Flat Gain Swing
6	R/W	0	EQ_AP<2>	
5	R/W	0	EQ_AP<1>	
4	R/W	0	EQ_AP<0>	
3	R/W	0	FG_AP<1>	
2	R/W	1	FG_AP<0>	
1	R/W	0	SW_AP<1>	
0	R/W	1	SW_AP<0>	
BYTE 8 (Equalization, Flat Gain, and -1dB Linear Swing Setting of CON_Rx1)				
Bit	**Type**	**Power-up Condition**	**Control Affected**	**Comment**
7	R/W	0	EQ_CON<3>	CON_Rx1 setting configuration Equalizer Flat Gain Swing
6	R/W	0	EQ_CON<2>	
5	R/W	0	EQ_CON<1>	
4	R/W	0	EQ_CON<0>	
3	R/W	0	FG_CON<1>	
2	R/W	1	FG_CON<0>	
1	R/W	0	SW_CON<1>	
0	R/W	1	SW_CON<0>	
BYTE 9-11 (Reserved)				
BYTE 12 (Threshold, Feature Enable/ Disable, and Timing Setting)				
Bit	**Type**	**Power-up Condition**	**Control Affected**	**Comment**
7	R/W	0	IDET_VTH<1>	High-speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default) 10 80mVppd 11 95mVppd
6	R/W	1	IDET_VTH<0>	
5	R/W	1	Reserved	—
4	R/W	1	Reserved	—
3	R/W	0	Reserved	—
2	R/W	0	Reserved	—
1	R/W	0	Reserved	—
0	R/W	1	Reserved	—
BYTE 13-31 (Reserved)				

Equalization Setting (dB):

EQ1pin	EQ0pin	EQ3	EQ2	EQ1	EQ0	@ 2.5GHz	@ 3GHz	@ 4GHz	@ 5GHz	@ 6GHz	Note
0	F	0	0	0	0	3.57	4.22	5.44	6.42	7.27	Default
0	1	0	0	0	1	3.83	4.56	5.93	7.04	8.00	—
0	0	0	0	1	0	4.13	4.93	6.47	7.71	8.76	—
0	R	0	0	1	1	4.41	5.29	6.95	8.29	9.42	—
R	1	0	1	0	0	4.98	5.89	7.61	8.99	10.14	—
R	F	0	1	0	1	5.25	6.23	8.05	9.50	10.70	—
R	R	0	1	1	0	5.55	6.59	8.51	10.04	11.28	—
R	0	0	1	1	1	5.82	6.92	8.93	10.51	11.78	—
F	0	1	0	0	0	6.39	7.44	9.39	10.93	12.16	—
F	R	1	0	0	1	6.63	7.74	9.76	11.34	12.60	—
F	F	1	0	1	0	6.90	8.05	10.14	11.77	13.05	—
F	1	1	0	1	1	7.14	8.34	10.49	12.15	13.44	—
1	R	1	1	0	0	7.51	8.71	10.87	12.53	13.81	—
1	0	1	1	0	1	7.74	8.97	11.18	12.87	14.15	—
1	1	1	1	1	0	7.98	9.25	11.51	13.23	14.51	—
1	F	1	1	1	1	8.20	9.51	11.81	13.54	14.82	—

Flat Gain Setting:

FGpin is the selection pin for the DC gain

FGpin	FG<1:0>	Flat Gain Setting (dB)
R	00	-2.07
F	01	-0.24 (Default)
0	10	0.62
1	11	1.77

Swing -1dB Compression Point Output Swing Setting:

SWpin is the selection pin for SW

SWpin	SW<1:0>	Swing Setting
0	00	900 mVppd
1	01	1000 mVppd (Default)
F	10	1100 mVppd
R	11	1200 mVppd

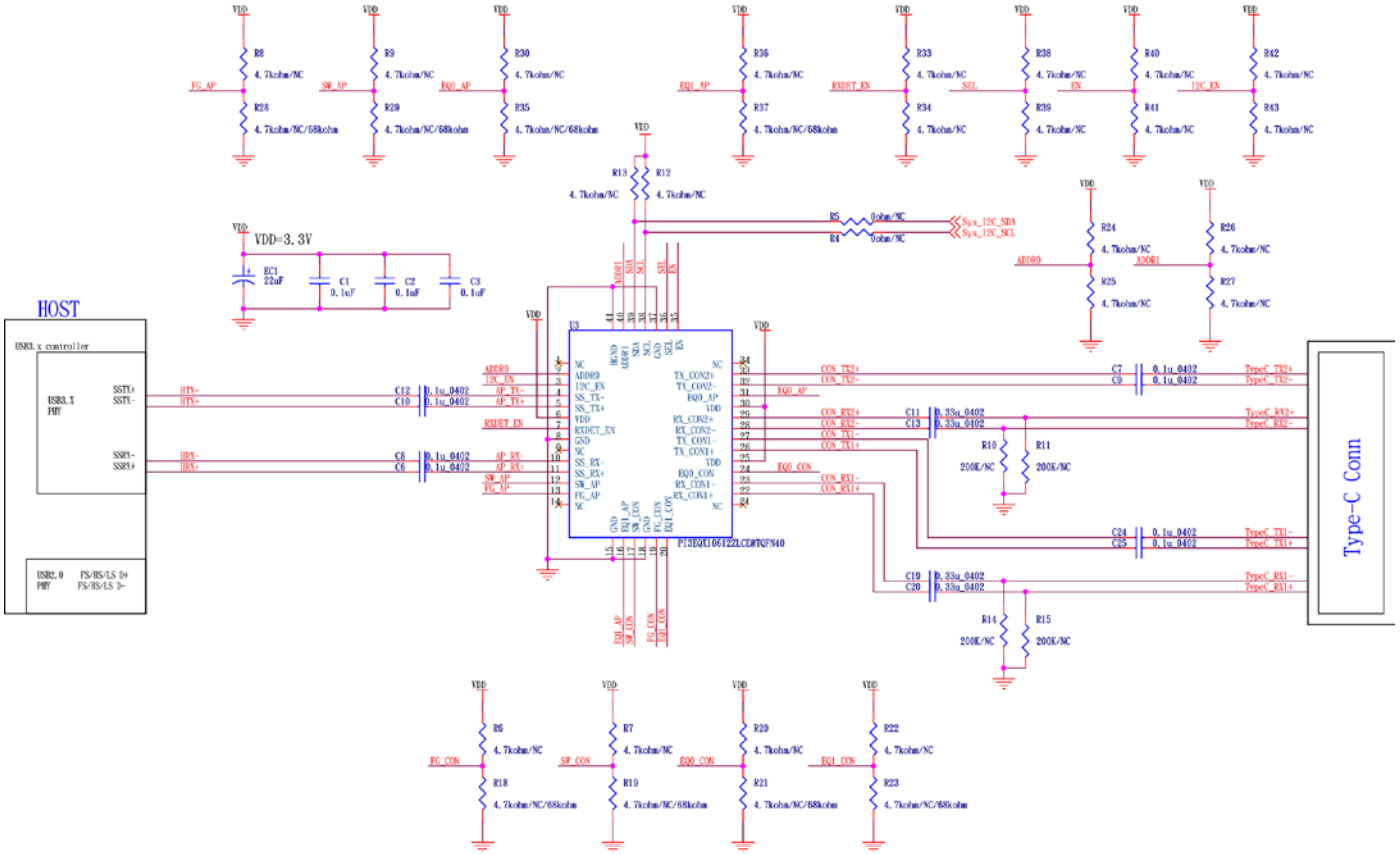
ReDriver Connection in Pin Mode

EN	SEL	ReDriver Status
0	X	Inactive
1	1	TX_CON1/RX_CON1 Active
1	0	TX_CON2/RX_CON2 Active

ReDriver Connection in I2C Mode

EN	BYTE3 CONF<2:0>	ReDriver Status
0	X	Inactive
1	100	TX_CON1/RX_CON1 Active
1	101 (default)	TX_CON2/RX_CON2 Active

Application Diagram

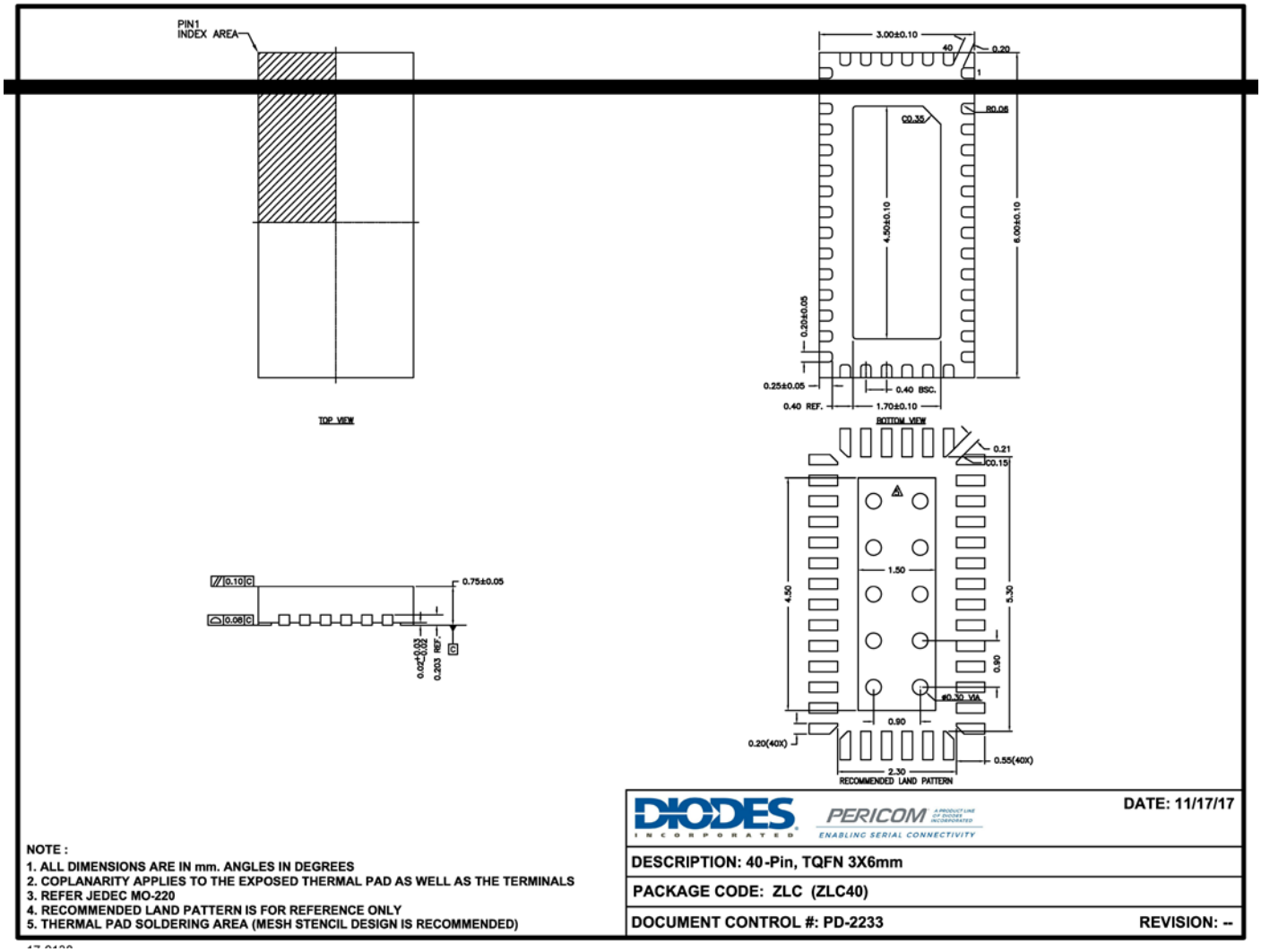


Part Marking

Top mark not available at this time. To obtain advanced information regarding the top mark, contact your local sales representative.

Packaging Mechanical

40-TQFN (ZLC)



For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX10612ZLCEX	ZLC	40-Pin, 3mm × 6mm (TQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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