DMC2004LPK

COMPLEMENTARY PAIR ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

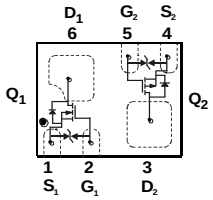
Features

- Low On-Resistance
- Low Gate Threshold Voltage $V_{GS(th)}$ < 1V
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Complementary Pair MOSFET
- Ultra-Small Surface Mount Package
- ESD Protected Gate
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e.: parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please refer to the related automotive grade (Q-suffix) part. A listing can be found at https://www.diodes.com/products/automotive/automotive-products/.**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability. https://www.diodes.com/quality/product-definitions/**

Mechanical Data

- Case: X1-DFN1612-6
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminal Connections: See Diagram
- Terminals: Finish – NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.003 grams (approximate)

X1-DFN1612-6



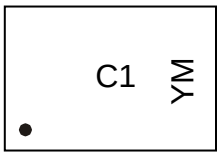
TOP VIEW
Internal Schematic

Ordering Information (Note 4)

Part Number	Case	Packaging
DMC2004LPK-7	X1-DFN1612-6	3000/Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



C1 = Marking Code
YM = Date Code Marking
Y = Year (ex: Z = 2012)
M = Month (ex: 9 = September)

Date Code Key

Year	2012	2013	2014	2015	2016	2017	2018
Code	Z	A	B	C	D	E	F

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings N-CHANNEL – Q_1 (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	±8	V
Drain Current (Note 5)	T_A = +25°C T_A = +85°C	I_D	750 540	mA

Maximum Ratings P-CHANNEL – Q_2 (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±8	V
Drain Current (Note 5)	T_A = +25°C T_A = +85°C	I_D	-600 -430	mA

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P_D	500	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	250	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-65 to +150	°C

Electrical Characteristics N-CHANNEL – Q_1 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	V_{GS} = 0V, I_D = 10µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 16V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	± 1	µA	V_{GS} = ±4.5V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(th)}$	0.5	—	1.0	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	— — —	0.4 0.5 0.7	0.55 0.70 0.90	Ω	V_{GS} = 4.5V, I_D = 540mA V_{GS} = 2.5V, I_D = 500mA V_{GS} = 1.8V, I_D = 350mA
Forward Transfer Admittance	$\|Y_{fs}\|$	200	—	—	mS	V_{DS} =10V, I_D = 0.2A
Diode Forward Voltage (Note 6)	V_{SD}	0.5	—	1.2	V	V_{GS} = 0V, I_S = 115mA
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	—	—	150	pF	V_{DS} = 16V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	—	25	pF	
Reverse Transfer Capacitance	C_{rss}	—	—	20	pF	

Electrical Characteristics P-CHANNEL – Q_2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1.0	µA	V_{DS} = -20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	± 1.0	µA	V_{GS} = ±4.5V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.5	—	-1.0	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	—	0.7 1.1 1.7	0.9 1.4 2.0	Ω	V_{GS} = -4.5V, I_D = -430mA V_{GS} = -2.5V, I_D = -300mA V_{GS} = -1.8V, I_D = -150mA
Forward Transfer Admittance	$\|Y_{fs}\|$	200	—	—	mS	V_{DS} =10V, I_D = 0.2A
Diode Forward Voltage (Note 5)	V_{SD}	-0.5	—	-1.2	V	V_{GS} = 0V, I_S = -115mA
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	—	—	175	pF	V_{DS} = -16V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	—	30	pF	
Reverse Transfer Capacitance	C_{rss}	—	—	20	pF	

Notes: 5. Device mounted on FR-4 PCB.
6. Short duration pulse test used to minimize self-heating effect.

Q_1, N-CHANNEL

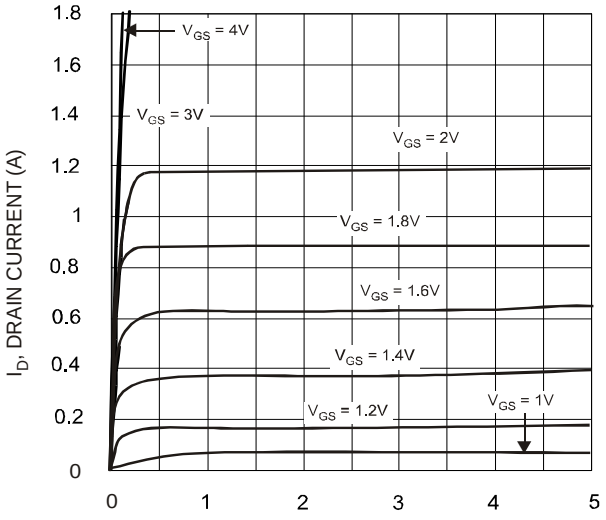


Fig. 1 Typical Output Characteristics

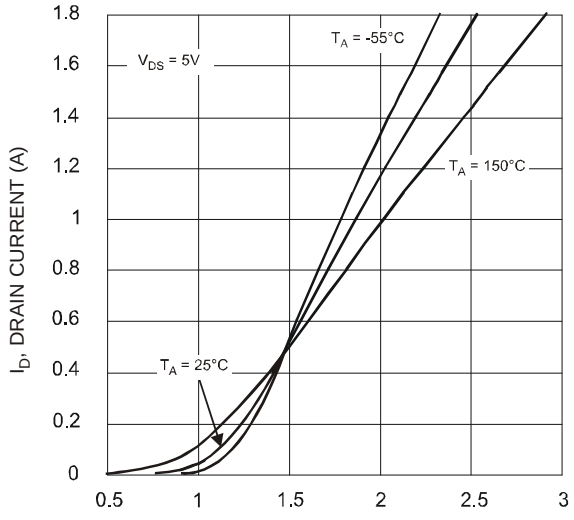


Fig. 2 Typical Transfer Characteristics

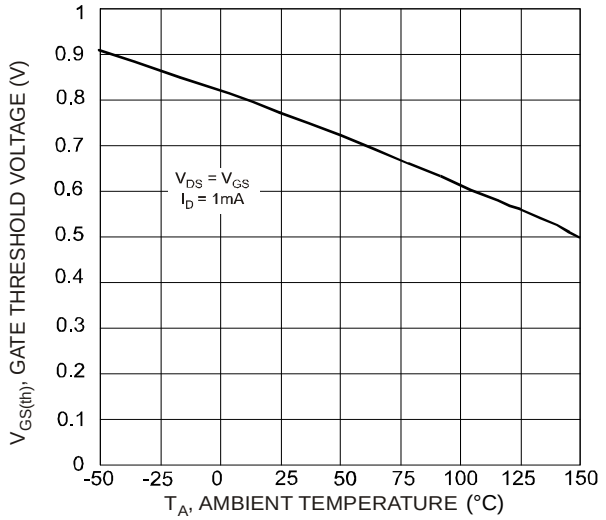


Fig. 3 Gate Threshold Voltage vs. Ambient Temperature

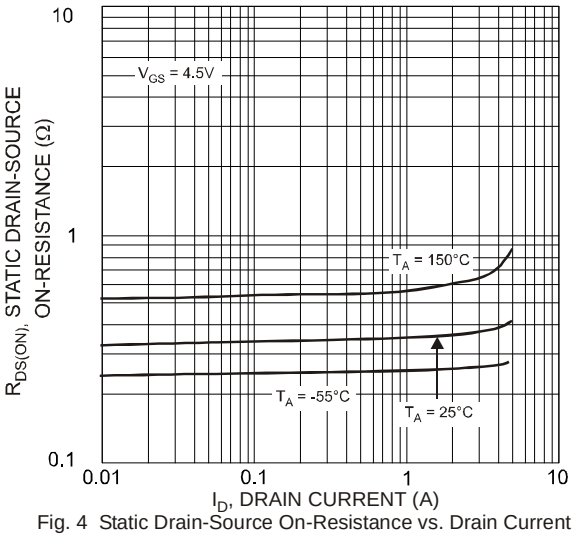


Fig. 4 Static Drain-Source On-Resistance vs. Drain Current

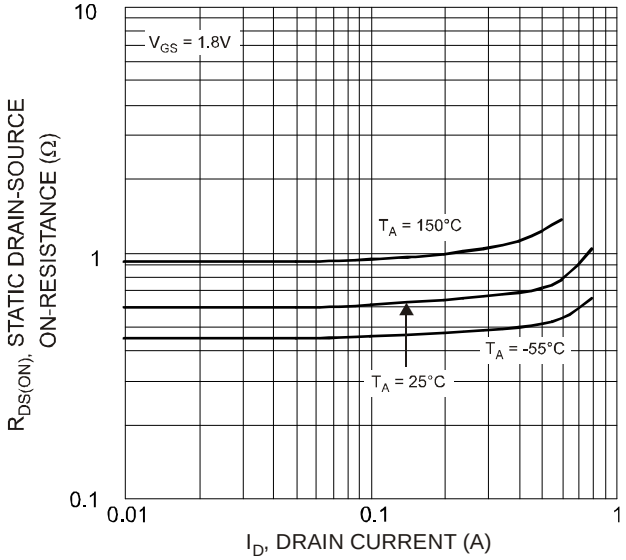


Fig. 5 Static Drain-Source On-Resistance vs. Drain Current

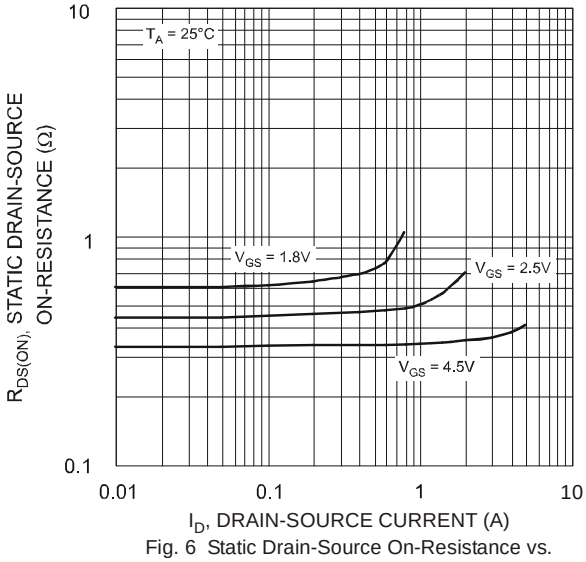


Fig. 6 Static Drain-Source On-Resistance vs. Drain-Source Current vs. Gate Source Voltage

Q_1, N-CHANNEL (continued)

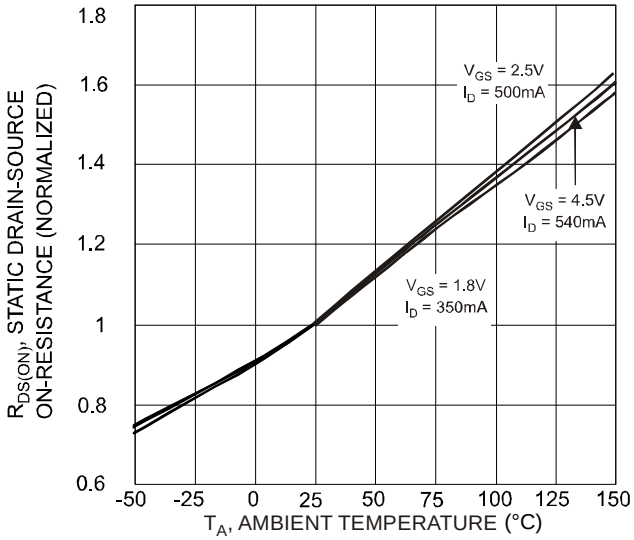


Fig. 7 Static Drain-Source On-State Resistance vs. Ambient Temperature

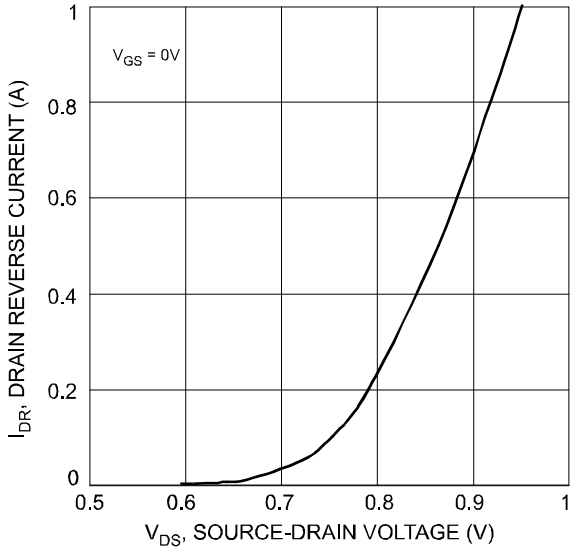


Fig. 8 Drain Reverse Current vs. Source-Drain Voltage

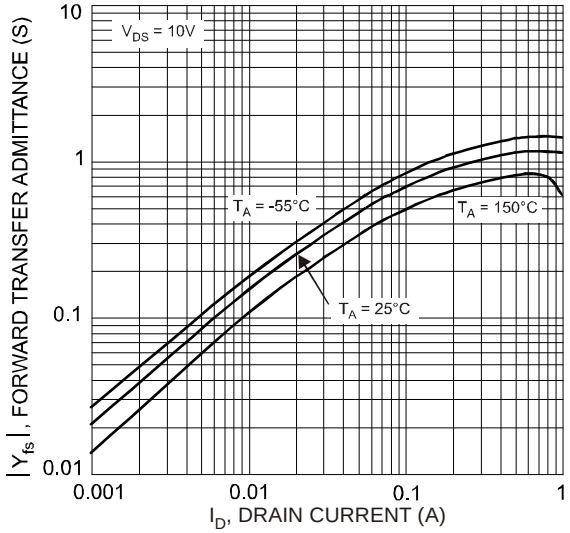


Fig. 9 Forward Transfer Admittance vs. Drain Current

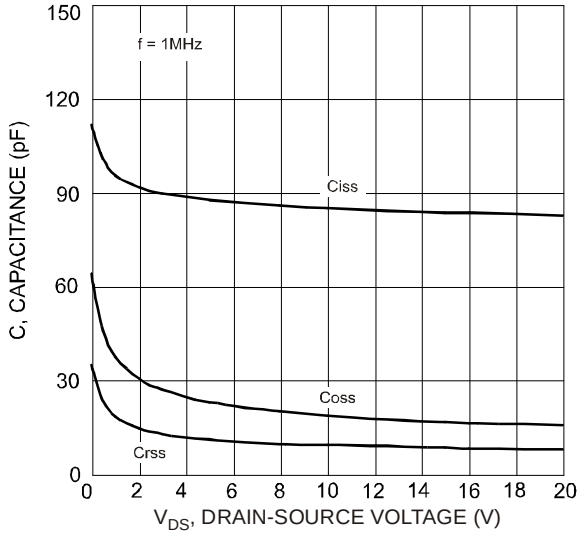


Fig. 10 Typical Capacitance

Q_2, P-CHANNEL

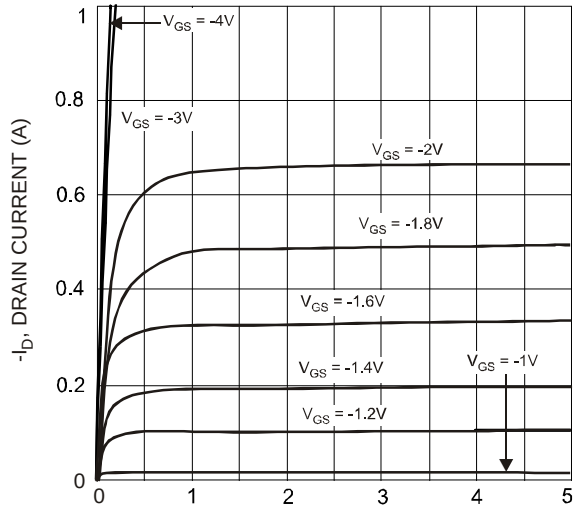


Fig. 11 Typical Output Characteristics

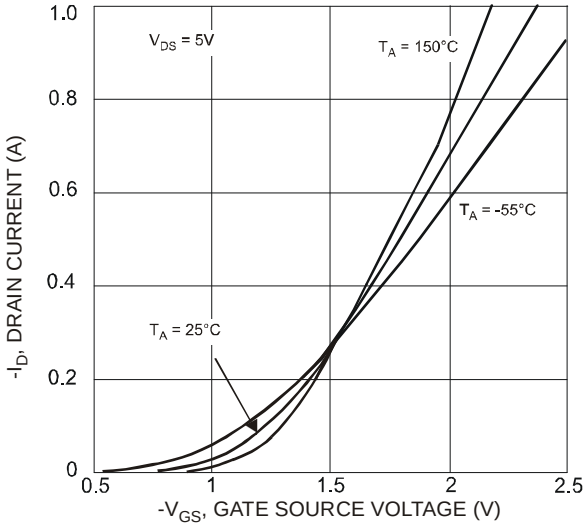


Fig. 12 Typical Transfer Characteristics

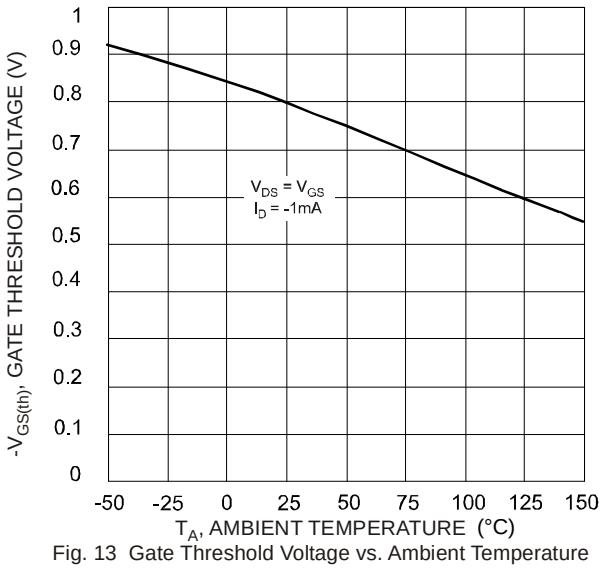


Fig. 13 Gate Threshold Voltage vs. Ambient Temperature

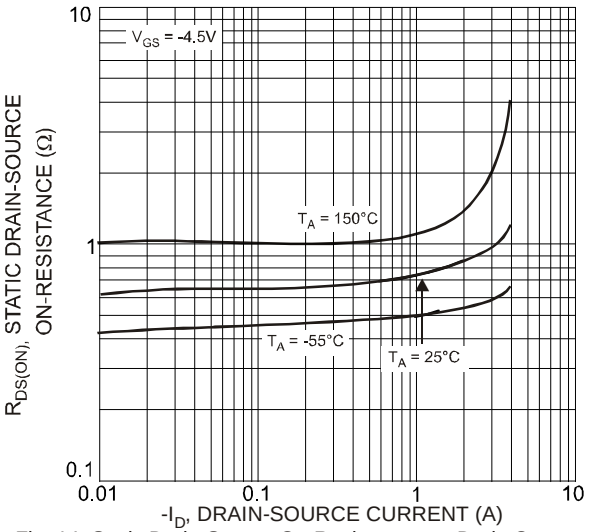


Fig. 14 Static Drain-Source On-Resistance vs. Drain Current

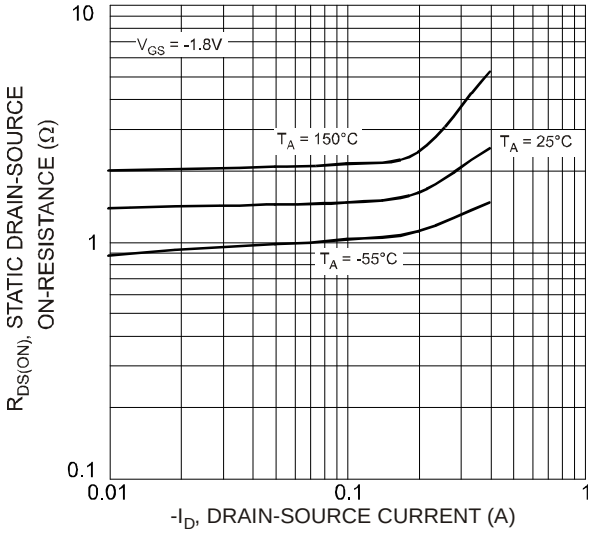


Fig. 15 Static Drain-Source On-Resistance vs. Drain Current

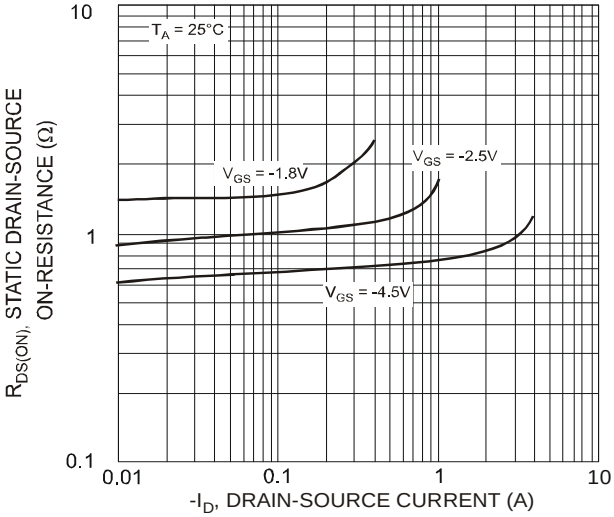


Fig. 16 Static Drain-Source On-Resistance vs. Drain-Source Current vs. Gate Source Voltage

Q_2, P-CHANNEL (continued)

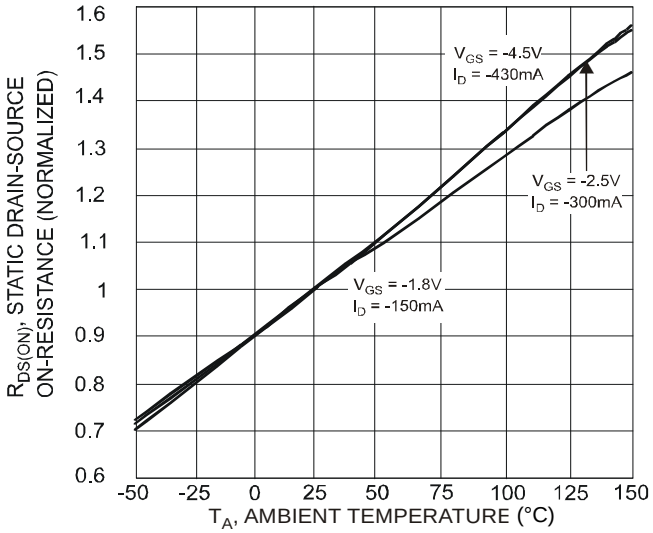


Fig. 17 Static Drain-Source On-State Resistance vs. Ambient Temperature

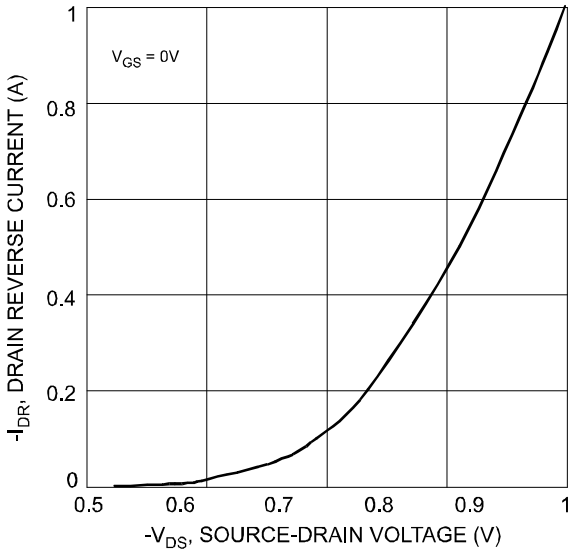


Fig. 18 Drain Reverse Current vs. Source-Drain Voltage

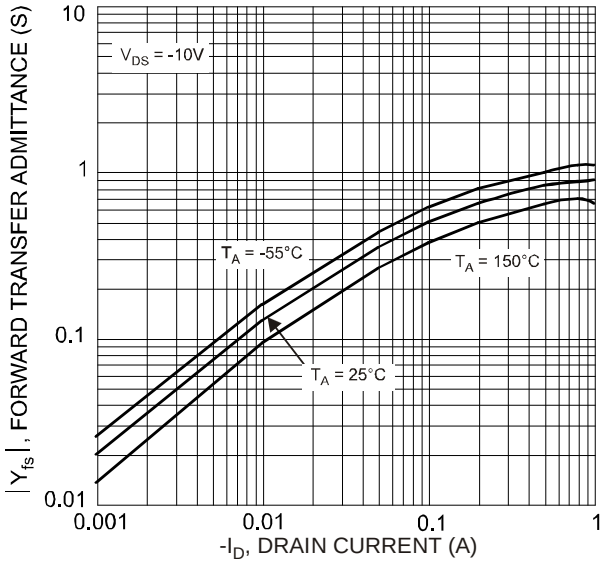


Fig. 19 Forward Transfer Admittance vs. Drain Current

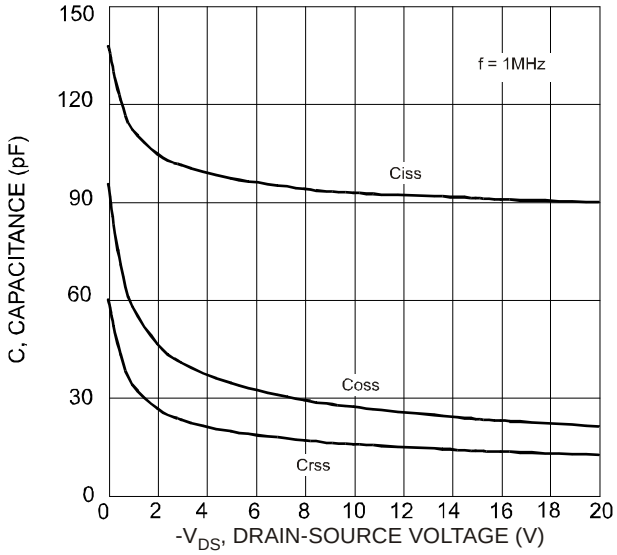
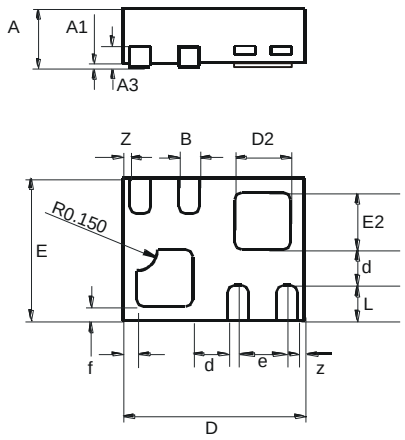


Fig. 20 Typical Capacitance

Package Outline Dimensions

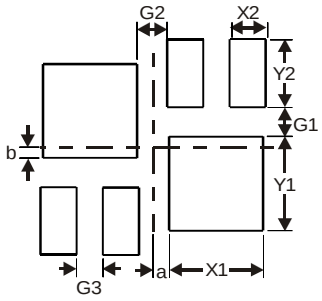
Please see http://www.diodes.com/package-outlines.html for the latest version.



X1-DFN1612-6			
Dim	**Min**	**Max**	**Typ**
A	0.47	0.53	0.50
A1	0	0.05	0.02
A3	—	—	0.13
b	0.15	0.25	0.20
D	1.55	1.675	1.60
d	—	—	0.25
D2	0.40	0.60	0.50
E	1.15	1.28	1.20
e	—	—	0.40
E2	0.45	0.65	0.55
f	—	—	0.15
L	0.20	0.30	0.25
Z	—	—	0.10
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.



Dimensions	Value (in mm)
G1	0.15
G2	0.175
G3	0.15
X1	0.60
X2	0.25
Y1	0.65
Y2	0.45
a	0.10
b	0.15

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

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