Lead-free Green

DGD2184
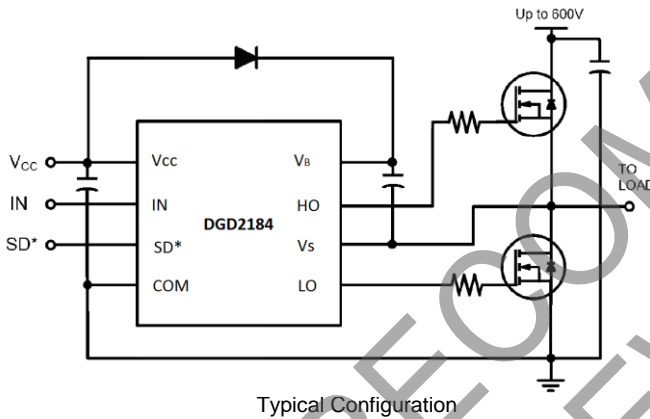
HALF BRIDGE GATE DRIVER IN SO-8

Description

The DGD2184 is a high voltage / high speed gate driver capable of driving N-Channel MOSFETs and IGBTs in a half bridge configuration. High voltage processing techniques enable the DGD2184's high-side to switch to 600V in a bootstrap operation.

The DGD2184 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) for easy interfacing with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. The DGD2184 has a fixed internal deadtime of 395ns (typ).

The DGD2184 is offered in SO-8 package, the operating temperature extends from -40°C to +125°C.

Applications

- DC-DC Converters
- DC-AC Inverters
- AC-DC Power Supplies
- Motor Controls
- Class D Power Amplifiers

Features

- Floating High-Side Driver in Bootstrap Operation to 600V
- Drives Two N-Channel MOSFETs or IGBTs in Half Bridge Configuration
- 1.4A Source / 1.8A Sink Output Current Capability
- Outputs Tolerant to Negative Transients
- Internal Dead Time of 395ns to Protect MOSFETs
- Wide Low-Side Gate Driver and Logic Supply: 10V to 20V
- Logic Input (IN and SD*) 3.3V Capability
- Schmitt Triggered Logic Inputs with Internal Pull Down
- Undervoltage Lockout for High and Low Side Drivers
- Extended Temperature Range: -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 ⓔ3
- Weight: 0.075 grams (Approximate)

Typical Configuration

SO-8

Top View

Ordering Information (Note 4)

| Part Number	Marking	Reel Size (inches)	Tape Width (mm)	Quantity Per Reel
DGD2184S8-13	DGD2184	13	12	2,500

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information
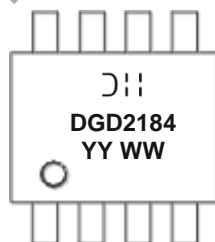
ꓛ╎╎ = Manufacturer's marking
DGD2184 = Product Type Marking Code
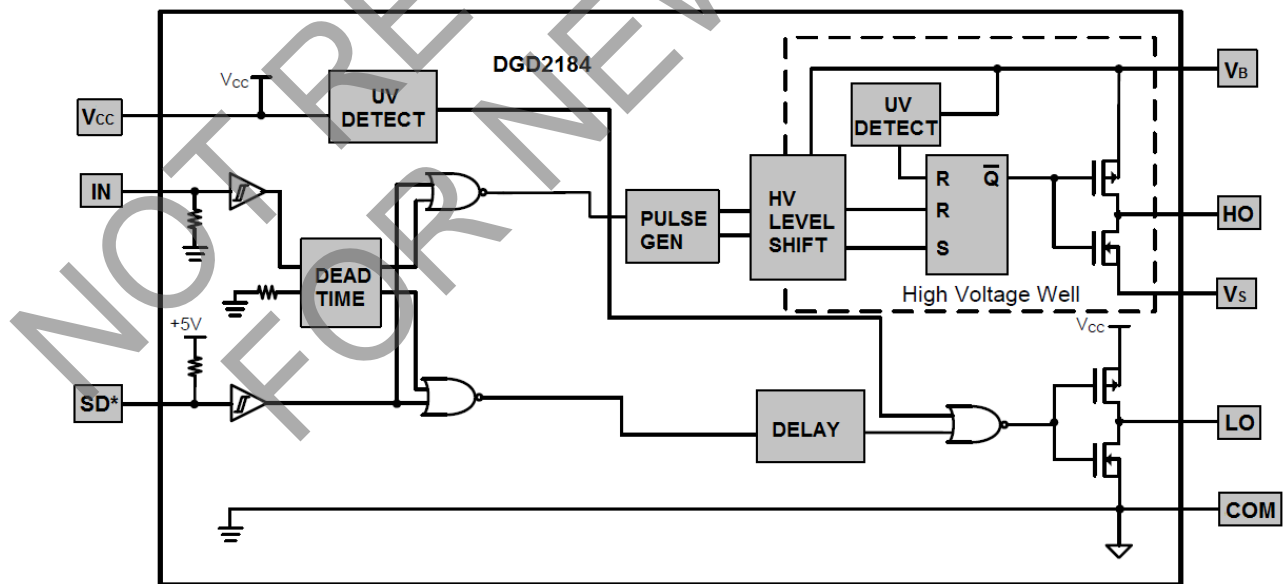YY = Year (ex: 19 = 2019)
WW = Week (01 to 53)

Pin Diagrams

IN	1		8	V_B	
SD*	2		7	HO	
COM	3		6	V_S	
LO	4		5	V_{CC}	
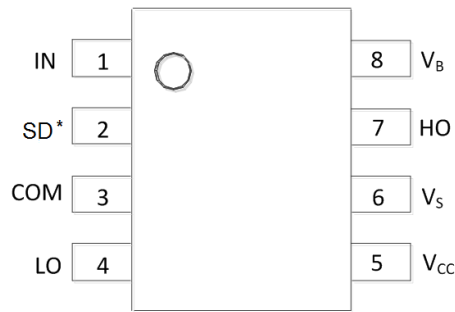
Top View: SO-8

Pin Descriptions

Pin Number	Pin Name	Function
1	IN	Logic input for High-side and Low-side Gate Driver Outputs (HO and LO), in Phase with HO
2	SD*	Logic Input for Shutdown, Enabled Low
3	COM	Low-Side and Logic Return
4	LO	Low-Side Gate Drive Output
5	V_{CC}	Low-Side and Logic Fixed Supply
6	V_S	High-Side Floating Supply Return
7	HO	High-Side Gate Drive Output
8	V_B	High-Side Floating Supply

Functional Block Diagram

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Absolute Maximum Ratings (@T$_A$ = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Supply Voltage	V$_B$	-0.3 to +624	V
High-Side Floating Supply Offset Voltage	V$_S$	V$_B$-24 to V$_B$+0.3	V
High-Side Floating Output Voltage	V$_{HO}$	V$_S$-0.3 to V$_B$+0.3	V
Offset Supply Voltage Transient	dV$_S$ / dt	50	V/ns
Low-Side Fixed Supply Voltage	V$_{CC}$	-0.3 to +24	V
Low-Side Output Voltage	V$_{LO}$	-0.3 to V$_{CC}$+0.3	V
Logic Input Voltage (IN and SD*)	V$_{IN}$	-0.3 to V$_{CC}$+0.3	V

Thermal Characteristics (@T$_A$ = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear derating factor (Note 5)	P$_D$	0.625	W
Thermal Resistance, Junction to Ambient (Note 5)	R$_{\theta JA}$	200	°C/W
Operating Temperature	T$_J$	+150	°C
Lead Temperature (Soldering, 10s)	T$_L$	+300	
Storage Temperature Range	T$_{STG}$	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High-Side Floating Supply Absolute Voltage	V$_B$	V$_S$ + 10	V$_S$ + 20	V
High-Side Floating Supply Offset Voltage	V$_S$	(Note 6)	600	V
High-Side Floating Output Voltage	V$_{HO}$	V$_S$	V$_B$	V
Low-Side Fixed Supply Voltage	V$_{CC}$	10	20	V
Low-Side Output Voltage	V$_{LO}$	0	V$_{CC}$	V
Logic Input Voltage (IN and SD*)	V$_{IN}$	0	V$_{CC}$	V
Ambient Temperature	T$_A$	-40	+125	°C

Note: 6. Logic operation for V$_S$ of -5V to +600V.

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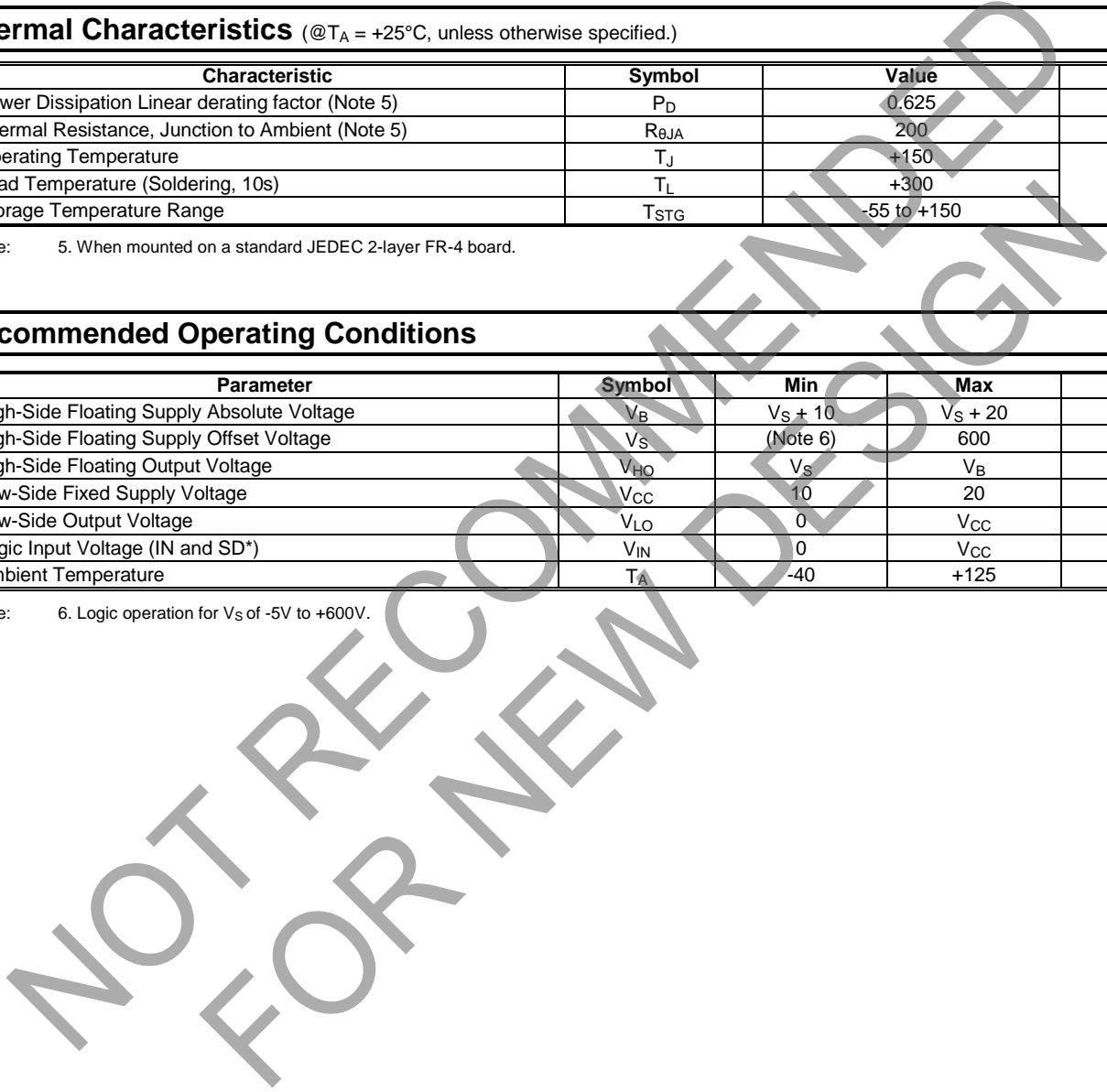
DC Electrical Characteristics (V$_{BIAS}$ (V$_{CC}$, V$_{BS}$) = 15V, @T$_A$ = +25°C, unless otherwise specified.) (Note 7)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Logic "1" Input Voltage (Note 8)	V$_{IH}$	2.5	–	–	V	V$_{CC}$ = 10V to 20V
Logic "0" Input Voltage (Note 8)	V$_{IL}$	–	–	0.8	V	V$_{CC}$ = 10V to 20V
SD* Input Positive Going Threshold	V$_{SDTH+}$	2.5	–	–	V	V$_{CC}$ = 10V to 20V
SD* Input Negative Going Threshold	V$_{SDTH-}$	–	–	0.8	V	V$_{CC}$ = 10V to 20V
High Level Output Voltage, V$_{BIAS}$ - V$_O$	V$_{OH}$	–	–	1.2	V	I$_O$ = 0mA
Low Level Output Voltage, V$_O$	V$_{OL}$	–	–	0.1	V	I$_O$ = 20mA
Offset Supply Leakage Current	I$_{LK}$	–	–	50	µA	V$_B$ = V$_S$ = 600V
Quiescent V$_{BS}$ Supply Current	I$_{BSQ}$	20	60	150	µA	V$_{IN}$ = 0V or 5V
Quiescent V$_{CC}$ Supply Current	I$_{CCQ}$	0.4	1.0	1.8	mA	V$_{IN}$ = 0V or 5V
Logic "1" Input Bias Current	I$_{IN+}$	–	25	60	µA	IN = 5V, SD* = 0V
Logic "0" Input Bias Current	I$_{IN-}$	–	–	1.0	µA	IN = 0V, SD* = 5V
V$_{BS}$ Supply Under-Voltage Positive Going Threshold	V$_{BSUV+}$	8.0	8.9	9.8	V	–
V$_{BS}$ Supply Under- Voltage Negative Going Threshold	V$_{BSUV-}$	7.4	8.2	9.0	V	–
V$_{CC}$ Supply Under- Voltage Positive Going Threshold	V$_{CCUV+}$	8.0	8.9	9.8	V	–
V$_{CC}$ Supply Under-Voltage Negative Going Threshold	V$_{CCUV-}$	7.4	8.2	9.0	V	–
Output High Short Circuit Pulsed Current	I$_{O+}$	1.4	1.9	–	A	V$_O$ = 0V, PW ≤ 10µs
Output Low Short Circuit Pulsed Current	I$_{O-}$	1.7	2.3	–	A	V$_O$ = 15V, PW ≤ 10µs

Notes: 7. The V$_{IN}$, and I$_{IN}$ parameters are applicable to the two logic input pins: IN and SD*. The V$_O$ and I$_O$ parameters are applicable to the respective output pins: HO and LO.
8. For optimal operation, it is recommended that the input pulses (IN and SD*) should have an minimum amplitude of 2.5V with a minimum pulse width of 800ns.

AC Electrical Characteristics (V$_{BIAS}$ (V$_{CC}$, V$_{BS}$) = 15V, C$_L$ = 1000pF, @T$_A$ = +25°C, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Turn-On Propagation Delay	t$_{ON}$	–	680	900	ns	V$_S$ = 0V
Turn-Off Propagation Delay	t$_{OFF}$	–	270	400	ns	V$_S$ = 0V or 600V
Shutdown Propagation Delay	t$_{SD}$	–	180	270	ns	–
Delay Matching, HO & LO Turn-On	t$_{DMON}$	–	–	90	ns	–
Delay Matching, HO & LO Turn-Off	t$_{DMOFF}$	–	–	40	ns	I$_o$ = 0A
Turn-On Rise Time	t$_R$	–	40	60	ns	V$_S$ = 0V
Turn-Off Fall Time	t$_F$	–	20	35	ns	V$_S$ = 0V
Deadtime: t$_{DT\ LO-HO}$ & t$_{DT\ HO-LO}$	t$_{DT}$	345	395	445	ns	–

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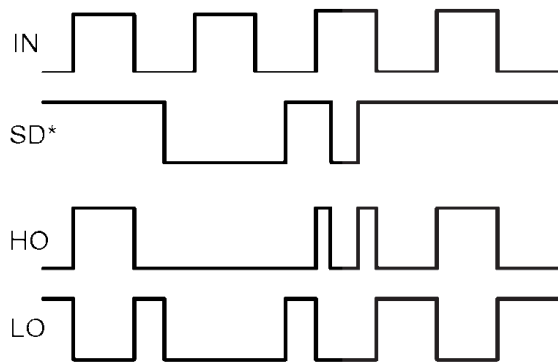© Diodes Incorporated

Timing Waveforms

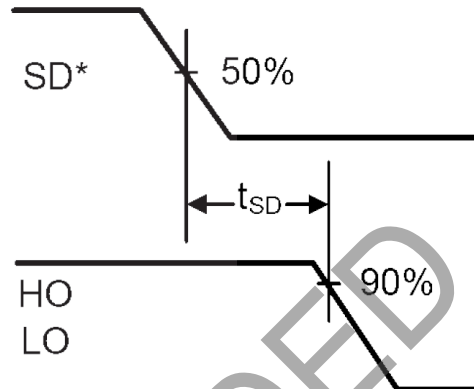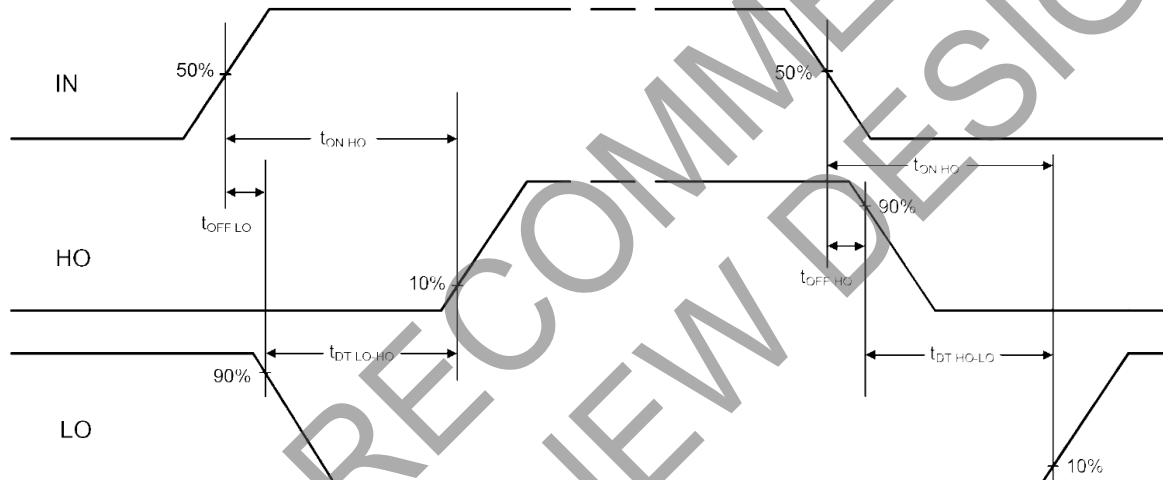**Figure 1.** Input / Output Timing Diagram

Figure 2. Shutdown Waveform Definitions

Deadtime $t_{DT\ LO-HO} = t_{ON\ HO} - t_{OFF\ LO}$
$t_{DT\ HO-LO} = t_{ON\ LO} - t_{OFF\ HO}$

Deadtime matching
$t_{MDT} = t_{DT\ LO-HO} - t_{DT\ HO-LO}$

Delay matching
$t_{DM\ OFF} = t_{OFF\ LO} - t_{OFFT\ HO}$

Figure 3. Switching Time Waveform Definitions

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Typical Performance Characteristics (@T$_A$ = +25°C, unless otherwise specified.)
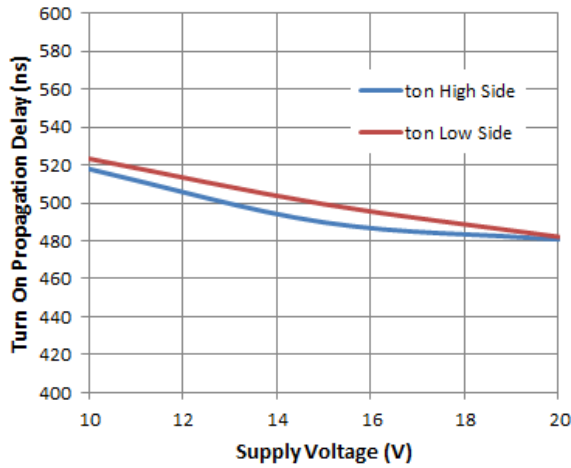
Figure 4. Turn-on Propagation Delay vs. Supply Voltage
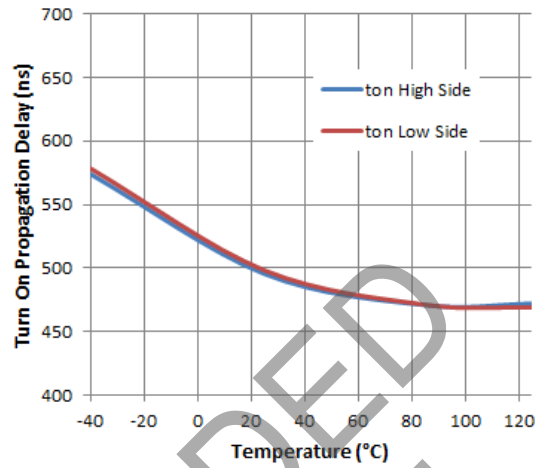
Figure 5. Turn-on Propagation Delay vs. Temperature
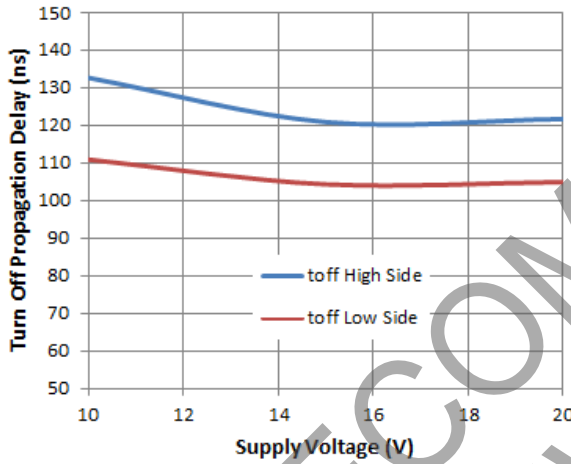
Figure 6. Turn-off Propagation Delay vs. Supply Voltage
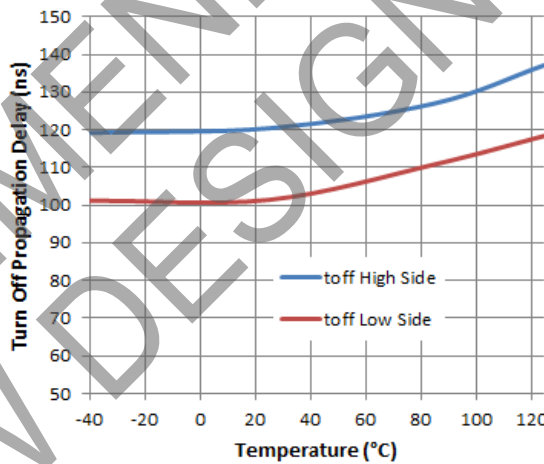
Figure 7. Turn-off Propagation Delay vs. Temperature
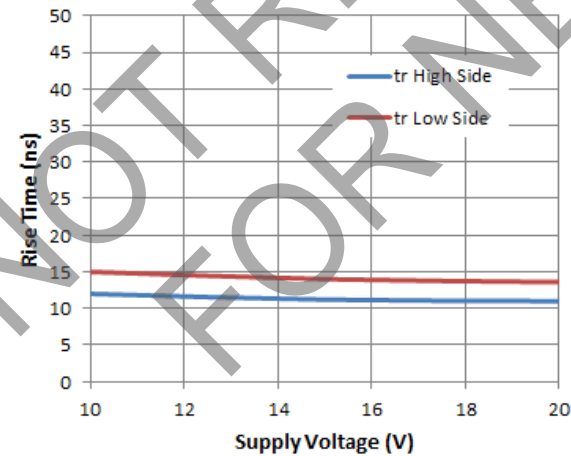
Figure 8. Rise Time vs. Supply Voltage
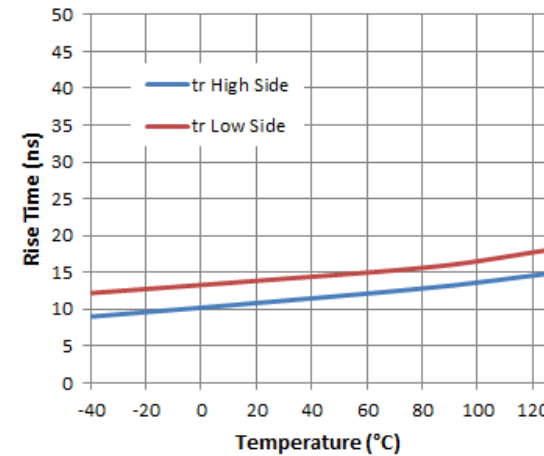
Figure 9. Rise Time vs. Temperature

Typical Performance Characteristics (continued)
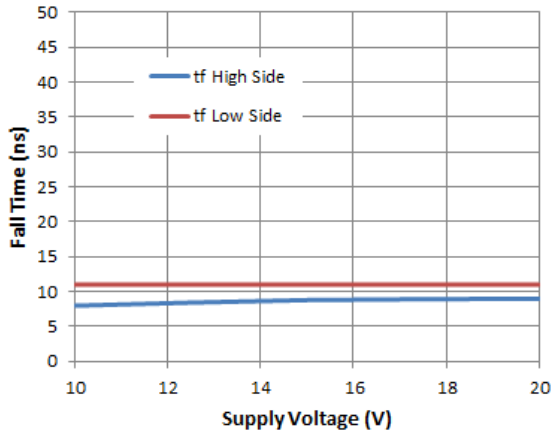
Figure 10. Fall Time vs. Supply Voltage
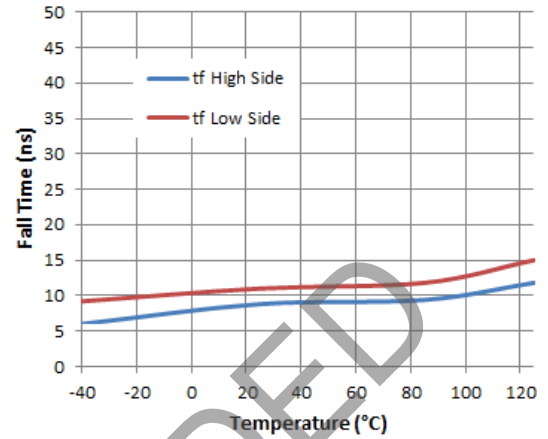
Figure 11. Fall Time vs. Temperature
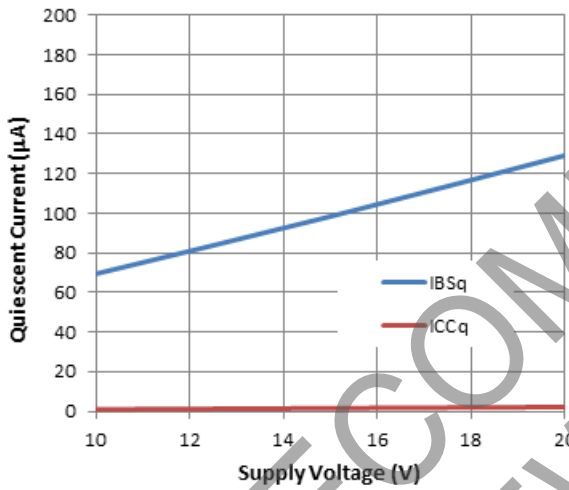
Figure 12. Quiescent Current vs. Supply Voltage
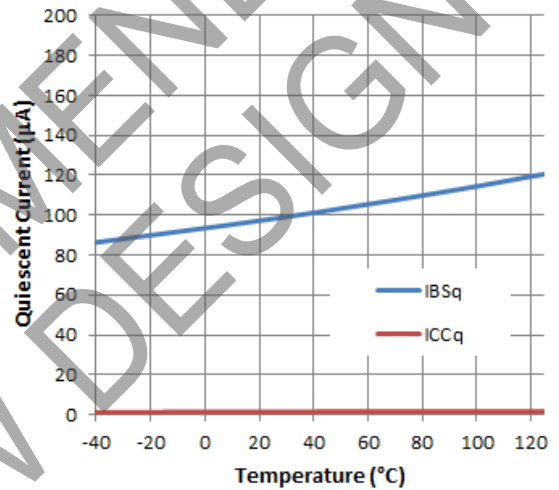
Figure 13. Quiescent Current vs. Temperature
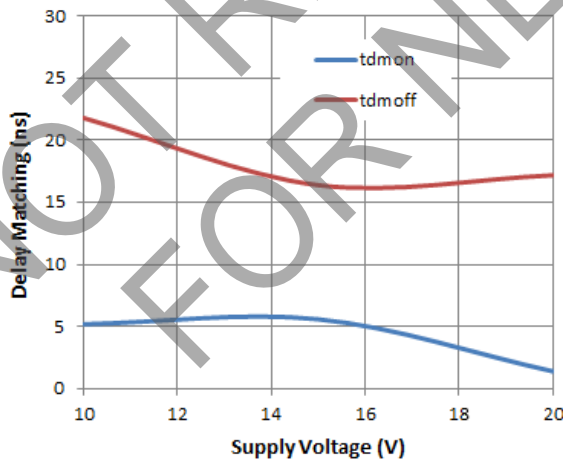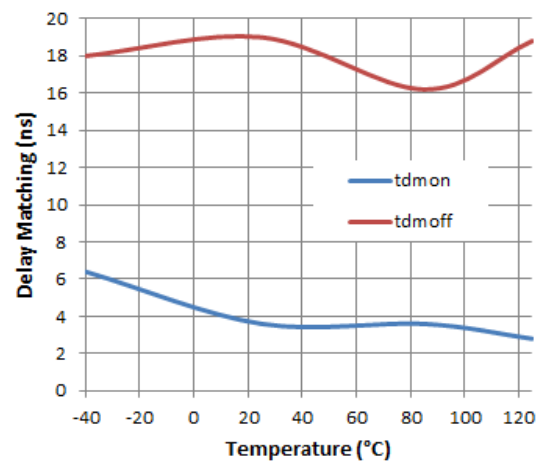

Figure 14. Delay Matching vs. Supply Voltage

Figure 15. Delay Matching vs. Temperature

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Typical Performance Characteristics (continued)
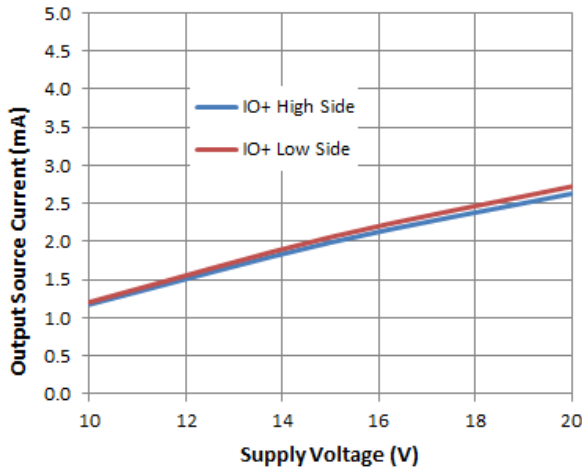
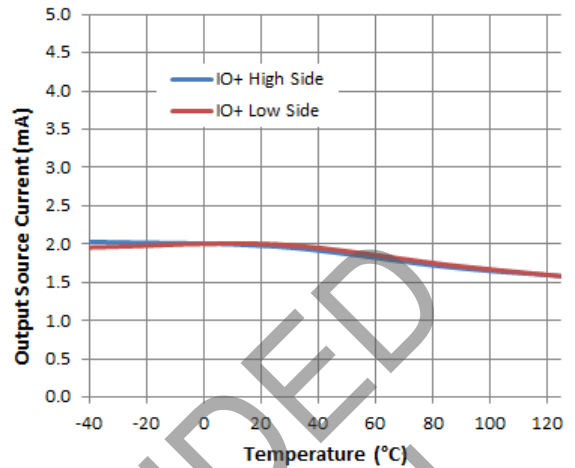Figure 16. Output Source Current vs. Supply Voltage

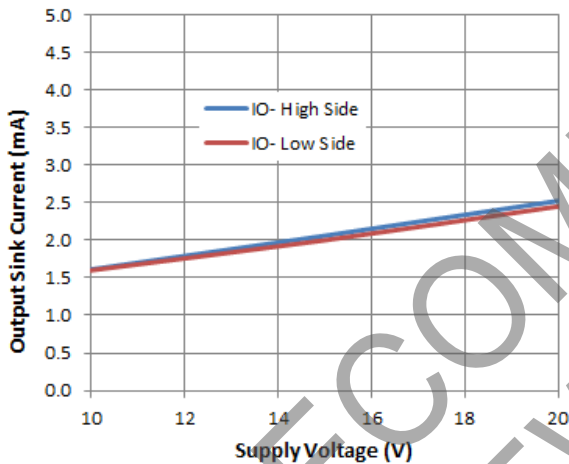Figure 17. Output Source Current vs. Temperature

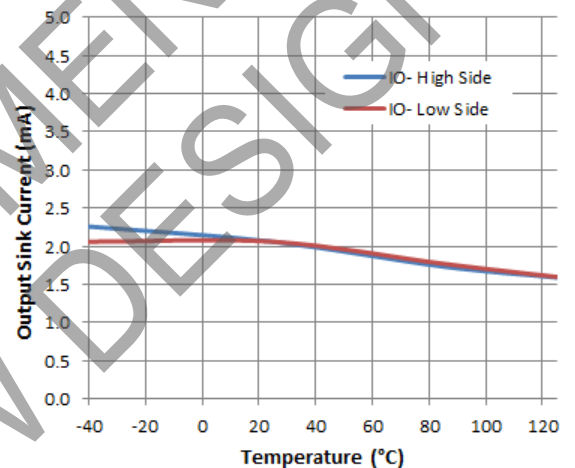Figure 18. Output Sink Current vs. Supply Voltage
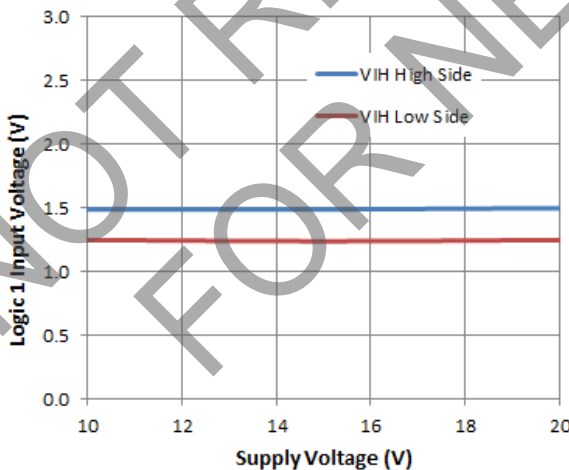

Figure 19. Output Sink Current vs. Temperature
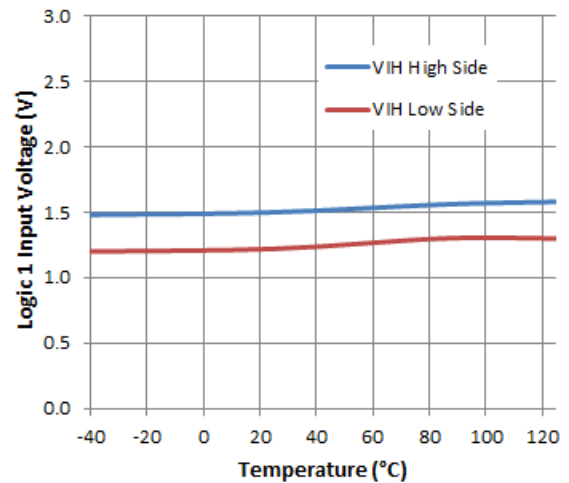

Figure 20. Logic 1 Input Voltage vs. Supply Voltage

Figure 21. Logic 1 Input Voltage vs. Temperature
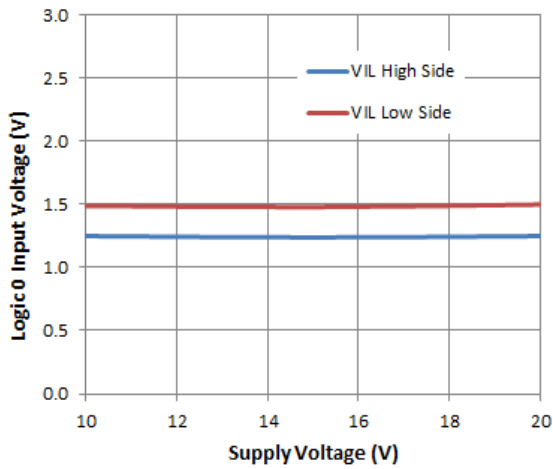
Typical Performance Characteristics (continued)

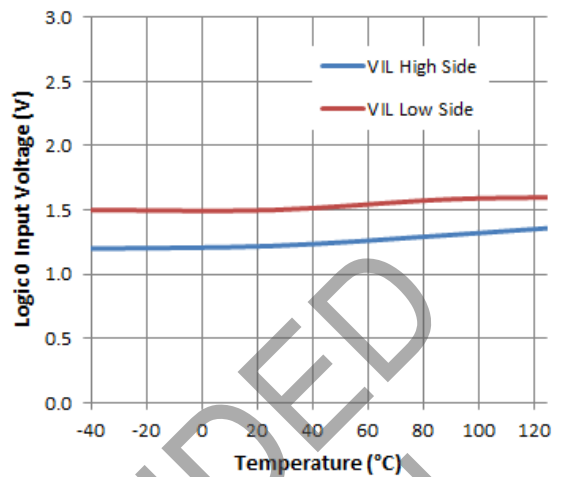**Figure 22.** Logic 0 Input Voltage vs. Supply Voltage

Figure 23. Logic 0 Input Voltage vs. Temperature
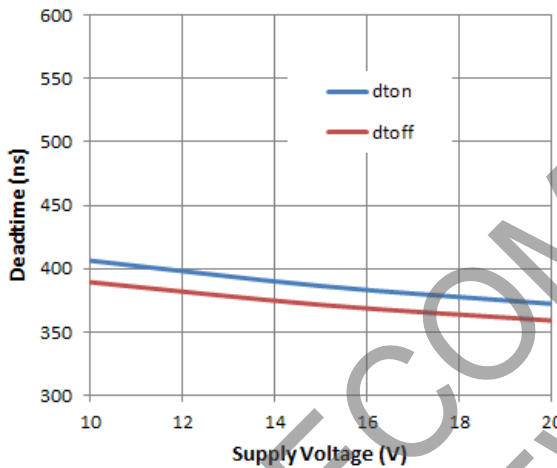

Figure 24. Deadtime vs. Supply Voltage
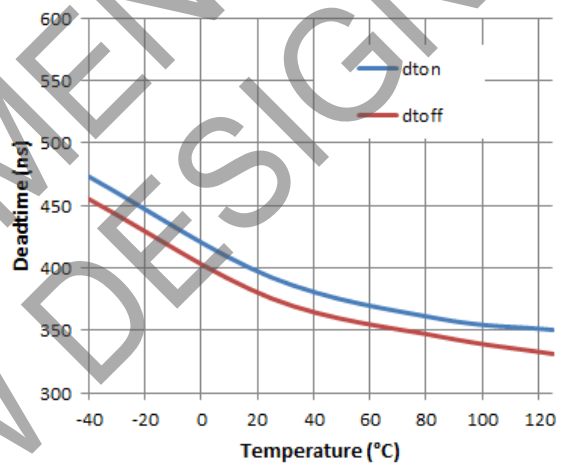
Figure 25. Deadtime vs. Temperature
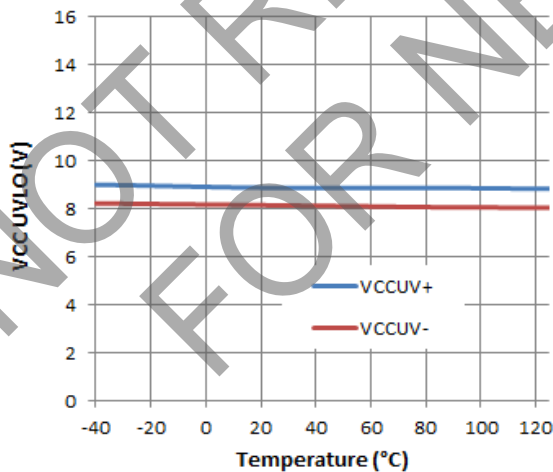
Figure 26. VCC UVLO vs. Temperature
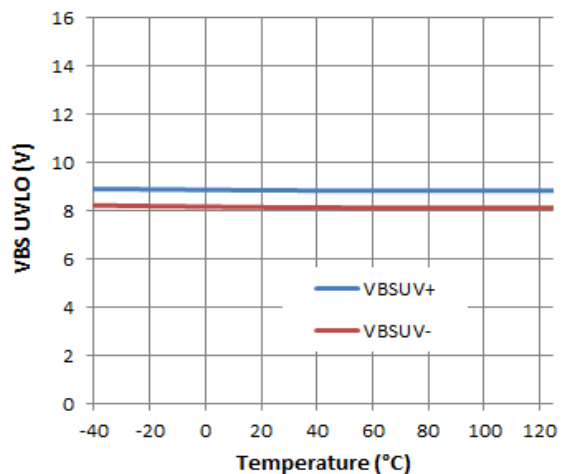
Figure 27. VBS UVLO vs. Temperature

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Typical Performance Characteristics (continued)
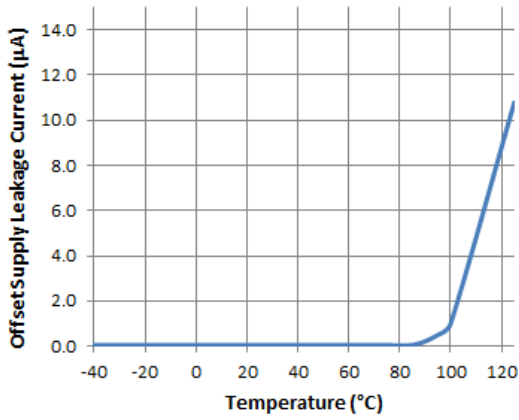
Figure 28. Offset Supply Leakage Current vs. Temperature

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.
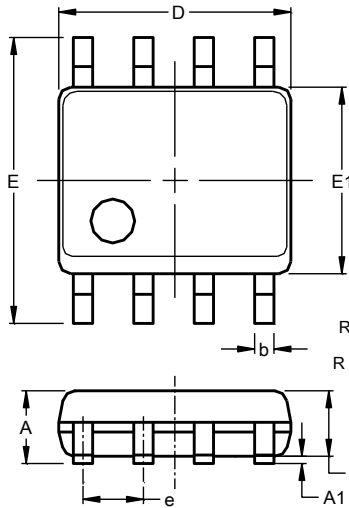
SO-8 (Type TH)

SO-8 (Type TH)			
Dim	**Min**	**Max**	**Typ**
A	1.35	1.75	--
A1	0.10	0.25	--
A2	--	--	1.45
b	0.35	0.51	--
c	0.190	0.248	--
D	4.80	5.00	4.90
E	5.80	6.20	6.00
E1	3.80	4.00	3.90
e	--	--	1.27
h	0.25	0.50	--
L	0.41	1.27	--
L1	--	--	1.04
Ø	0°	8°	--
All Dimensions in mm			

R 0.16+/-0.02
R 0.23+/-0.02

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8 (Type TH)
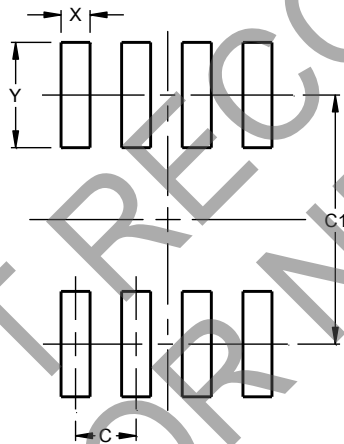
Dimensions	Value (in mm)
C	1.27
C1	5.20
X	0.60
Y	2.20

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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    1. are intended to implant into the body, or

    2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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