N-CHANNEL ENHANCEMENT MODE FIELD MOSFET

Product Summary

$V_{(BR)SSS}$	$R_{SS(ON)}$	Package	I_S T_A = +25°C
24V	26mΩ @ V_{GS} = 4.5V	X1-WLB1818-4	6.0A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{SS(ON)}$) with thin WLCSP packaging process and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Battery Management
- Load Switch
- Battery Protection

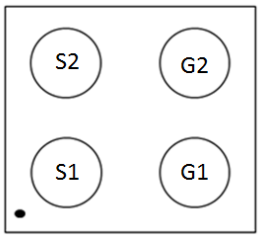
Features

- Built-in G-S Protection Diode Against ESD 2kV HBM
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

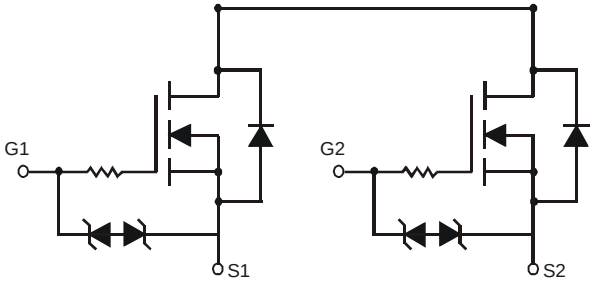
Mechanical Data

- Case: X1-WLB1818-4
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram

X1-WLB1818-4



Top View



N-Channel N-Channel

Equivalent Circuit

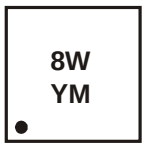
Ordering Information (Note 4)

Part Number	Case	Packaging
DMN2023UCB4-7	X1-WLB1818-4	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

X1-WLB1818-4



8W = Product Type Marking Code
YM = Date Code Marking
Y or $\overline{Y}$ = Year (ex: E = 2017)
M or $\overline{M}$ = Month (ex: 9 = September)

Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017
Code	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Source-Source Voltage			V_{SSS}	24	V
Gate-Source Voltage (Note 5)			V_{GSS}	±12	V
Continuous Source Current @ T_A = +25°C (Note 6)	Steady State	T_A = +25°C T_A = +70°C	I_S	6.0 4.8	A
Pulsed Source Current @ T_A = +25°C (Notes 6 & 7)			I_{SM}	20	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation @ T_A = +25°C (Note 6)	P_D	1.45	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 6)	$R_{\theta JA}$	88.21	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Source to Source Breakdown Voltage T_J = +25°C	$V_{(BR)SSS}$	24	—	—	V	I_S = 1mA, V_{GS} = 0V, Test Circuit 1
Zero Gate Voltage Source Current T_J = +25°C	I_{SSS}	—	—	1.0	µA	V_{SS} = 20V, V_{GS} = 0V, Test Circuit 1
Gate-Body Leakage	I_{GSS}	—	—	±10	µA	V_{GS} = ±8V, V_{SS} = 0V, Test Circuit 2
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.5	—	1.3	V	V_{SS} = 10V, I_S = 1.0mA, Test Circuit 3
Static Source-Source On-Resistance	$R_{SS(ON)}$	17	21.5	25.5	mΩ	V_{GS} = 6.5V, I_S = 3.0A, Test Circuit 5
		17.5	22	26		V_{GS} = 4.5V, I_S = 3.0A, Test Circuit 5
		18.5	23	27		V_{GS} = 4.0V, I_S = 3.0A, Test Circuit 5
		19	23.5	29		V_{GS} = 3.7V, I_S = 3.0A, Test Circuit 5
		19.5	24	33		V_{GS} = 3.1V, I_S = 3.0A, Test Circuit 5
		21.5	27	40		V_{GS} = 2.5V, I_S = 3.0A, Test Circuit 5
Forward Transfer Admittance	$\|Y_{fs}\|$	—	12	—	S	V_{SS} = 10V, I_S = 3.0A, Test Circuit 4
Body Diode Forward Voltage	$V_{F(S-S)}$	—	0.7	1	V	I_F = 3.0A, V_{GS} = 0V, Test Circuit 6
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	2564	3333	pF	V_{SS} = 10V, V_{GS} = 0V, f = 1.0MHz Test Circuit 7
Output Capacitance	C_{oss}	—	197	275		
Reverse Transfer Capacitance	C_{rss}	—	183	260		
Total Gate Charge	Q_g	—	29	37	nC	V_{GS} = 4.5V, V_{SS} = 10V, I_S = 6A Test Circuit 9
Turn-On Delay Time	$t_{D(ON)}$	—	10	15	ns	V_{SS} = 10V, R_L = 3.33Ω, I_S = 3.0A Test Circuit 8
Turn-On Rise Time	t_R	—	20	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	75	110	ns	
Turn-Off Fall Time	t_F	—	29	—	ns	

Notes:
5. AEC-Q101 V_{GS} maximum is ±9.6V.
6. Device mounted on FR-4 material with 1-inch^2 (6.45-cm^2), 2-oz.(0.071-mm thick) Cu.
7. Repetitive rating, pulse width limited by junction temperature.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.

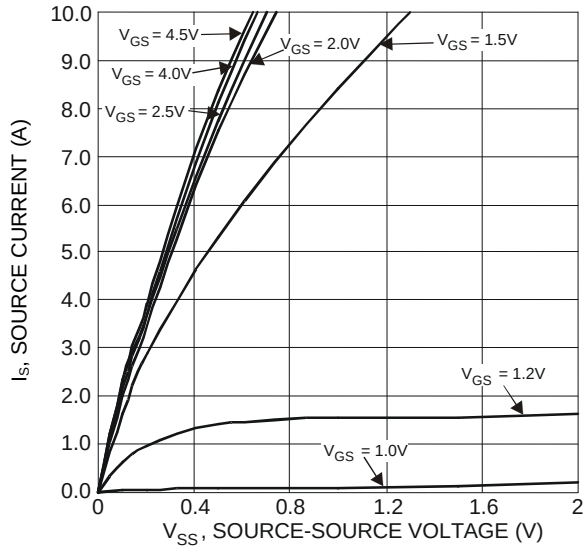


Figure 1. Typical Output Characteristics

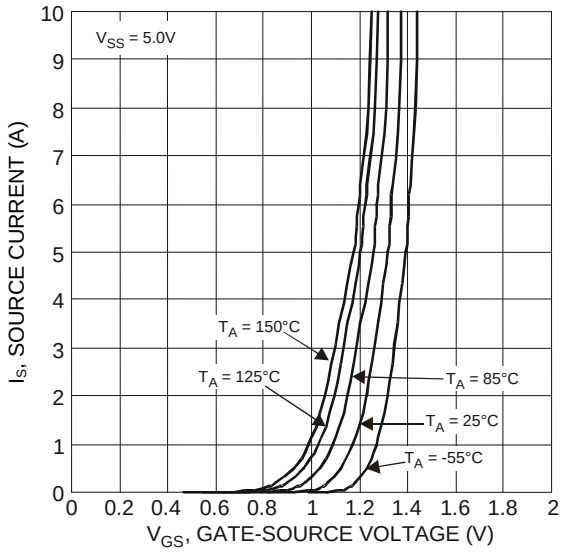


Figure 2. Typical Transfer Characteristics

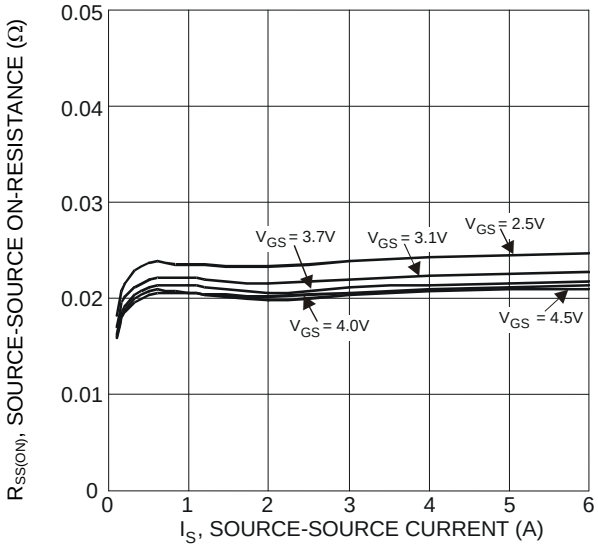


Figure 3. Typical On-Resistance vs. Source Current and Gate Voltage

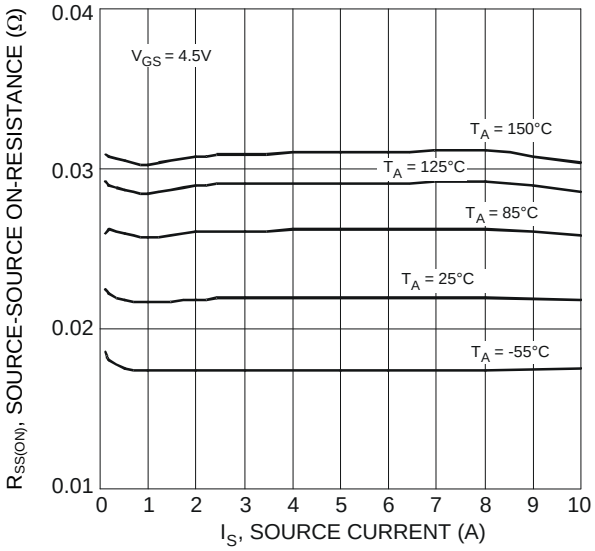


Figure 4. Typical On-Resistance vs. Source Current and Temperature

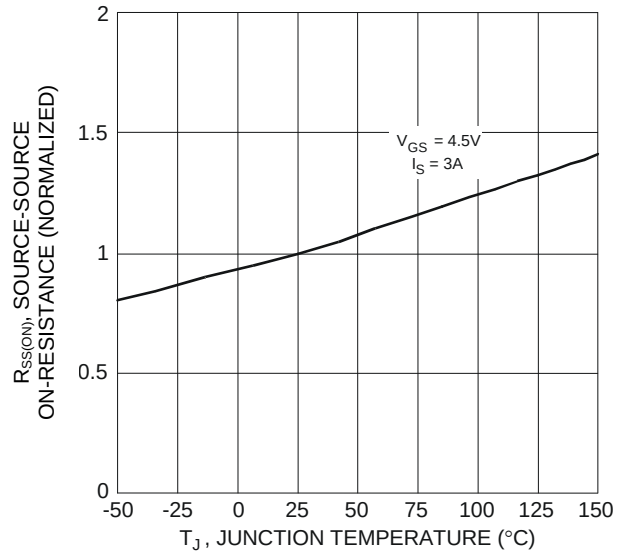


Figure 5. On-Resistance Variation with Temperature

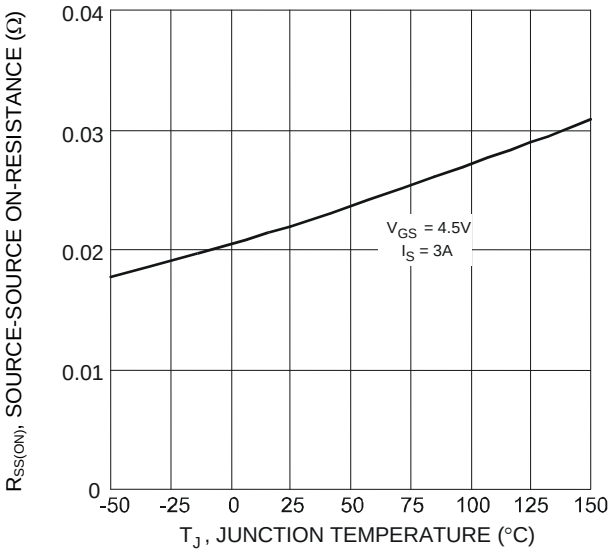


Figure 6. On-Resistance Variation with Temperature

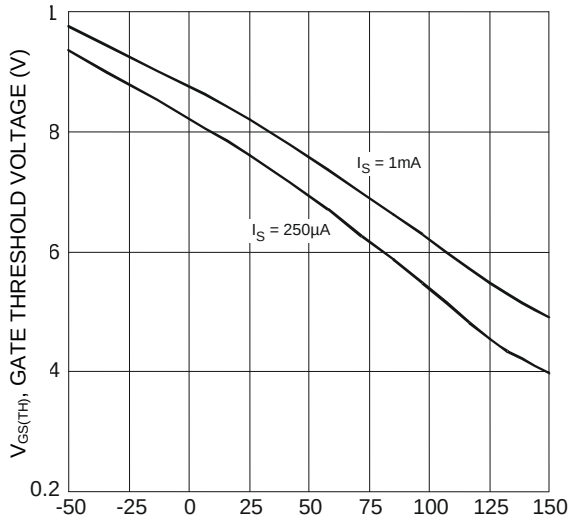


Figure 7. Gate Threshold Variation vs. Junction Temperature

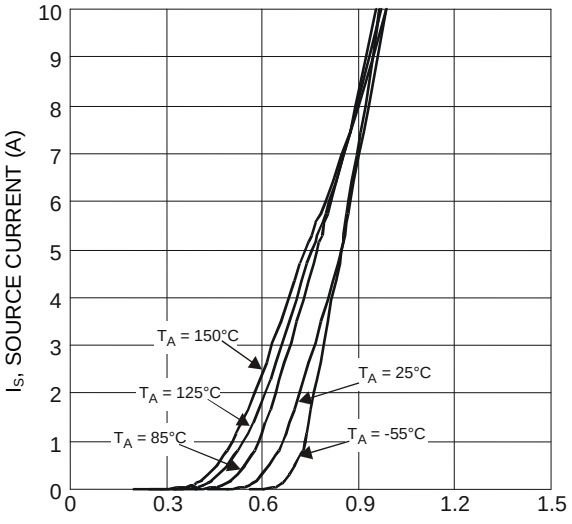


Figure 8. Diode Forward Voltage vs. Current

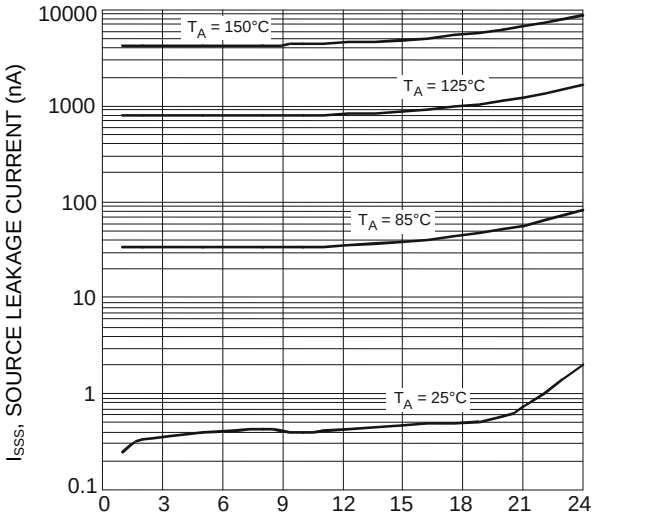


Figure 9. Typical Source-Source Leakage Current vs. Voltage

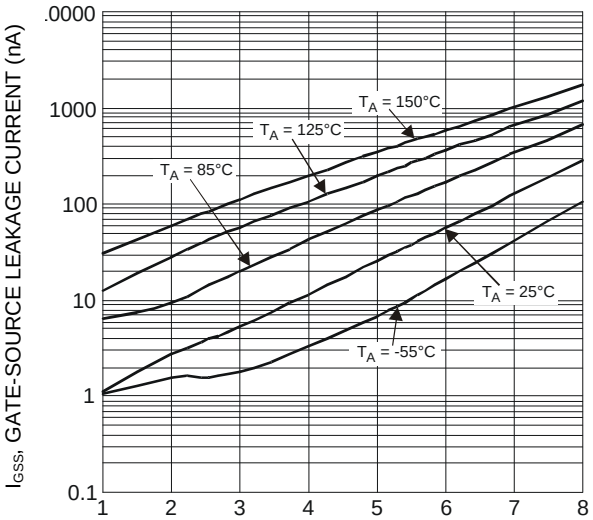


Figure 10. Typical Gate-Source Leakage Current vs. Gate-Source Voltage

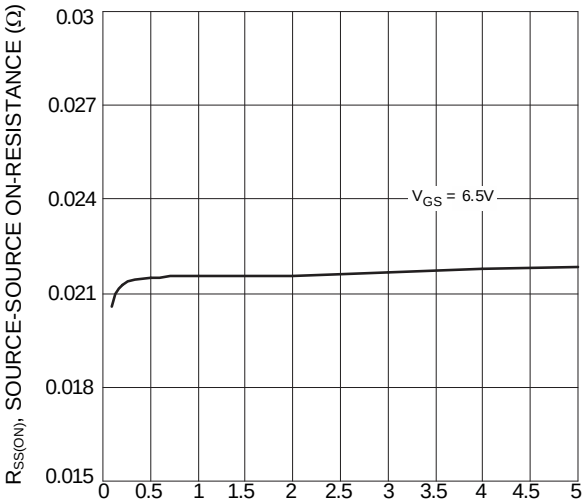


Figure 11. Typical On-Resistance vs. Source Current and Gate Voltage

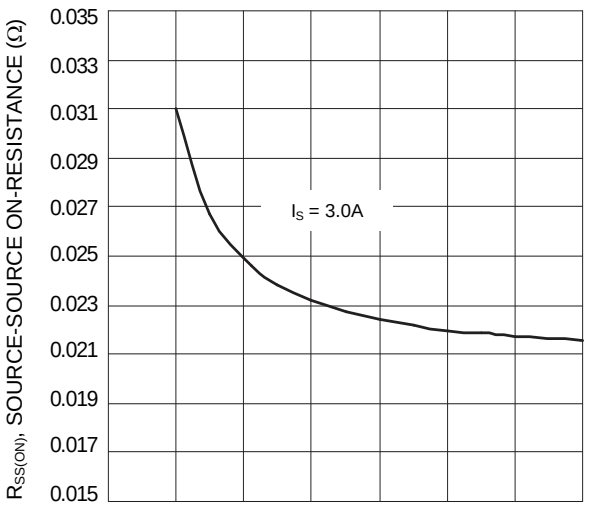


Figure 12 Typical Transfer Characteristic

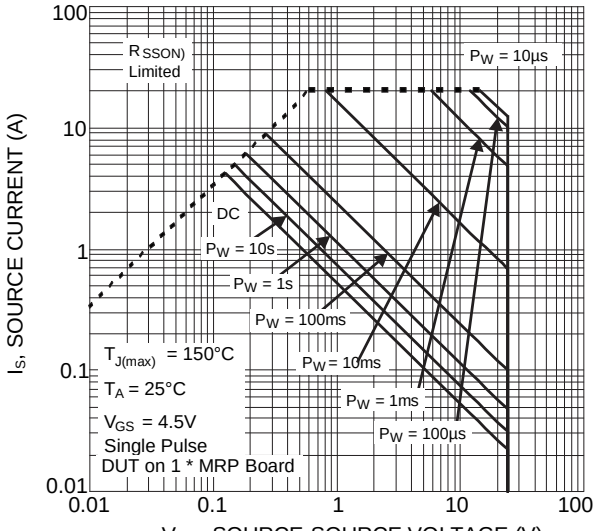
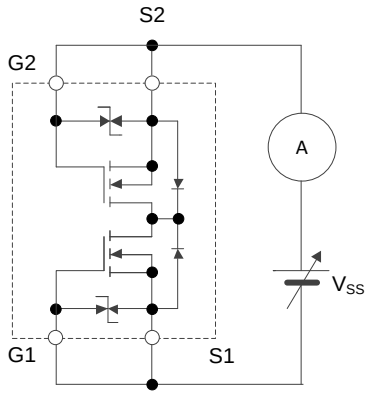
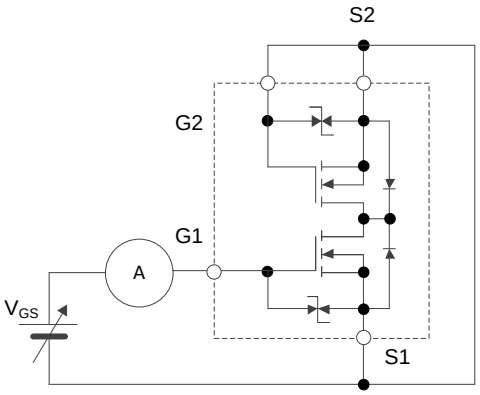


Figure 13. SOA, Safe Operation Area

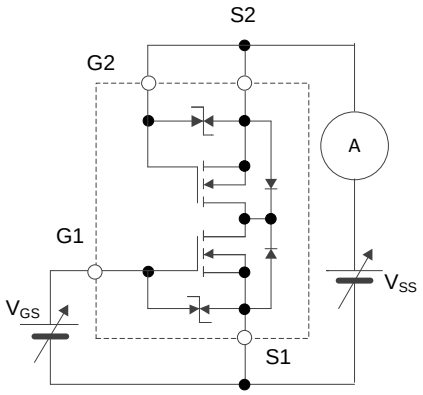
Test Circuits



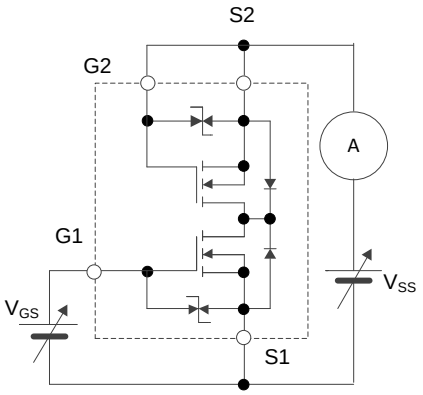
Test Circuit 1 I_{SSS}



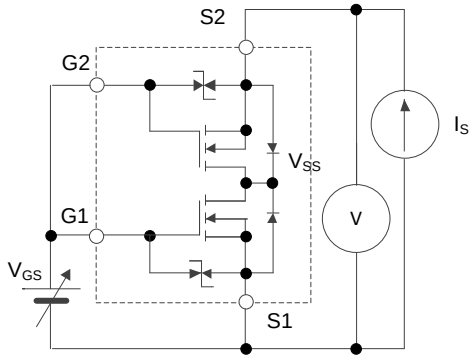
Test Circuit 2 I_{GSS}
When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



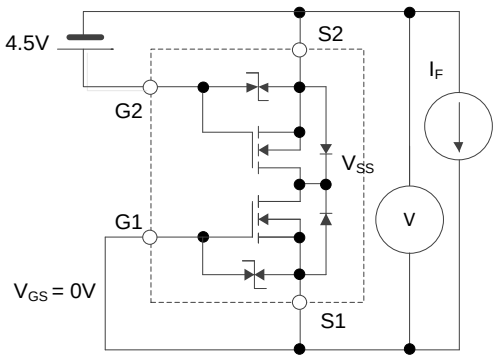
Test Circuit 3 $V_{GS(OFF)}$
When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



Test Circuit 4 $|Y_{fs}|$
$\Delta I_S/\Delta V_{GS}$

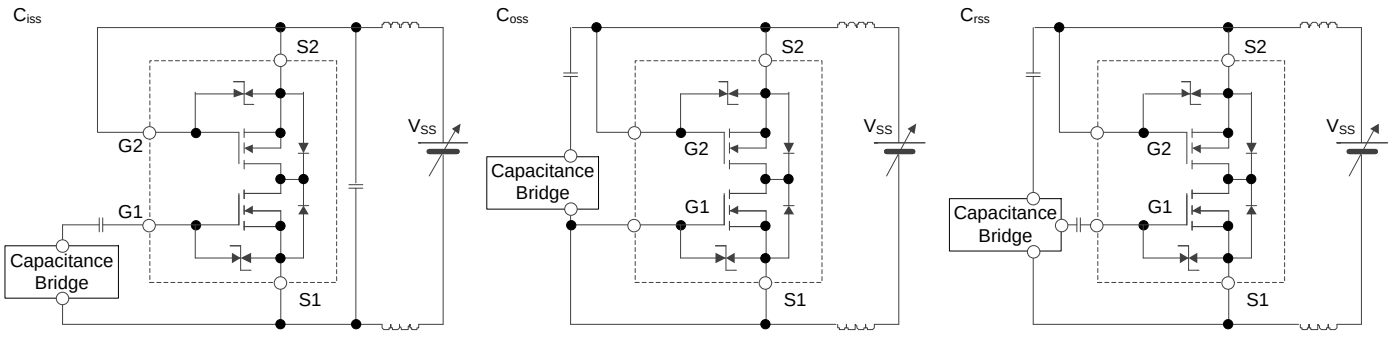


Test Circuit 5 $R_{SS(ON)}$
V_{SS}/I_S

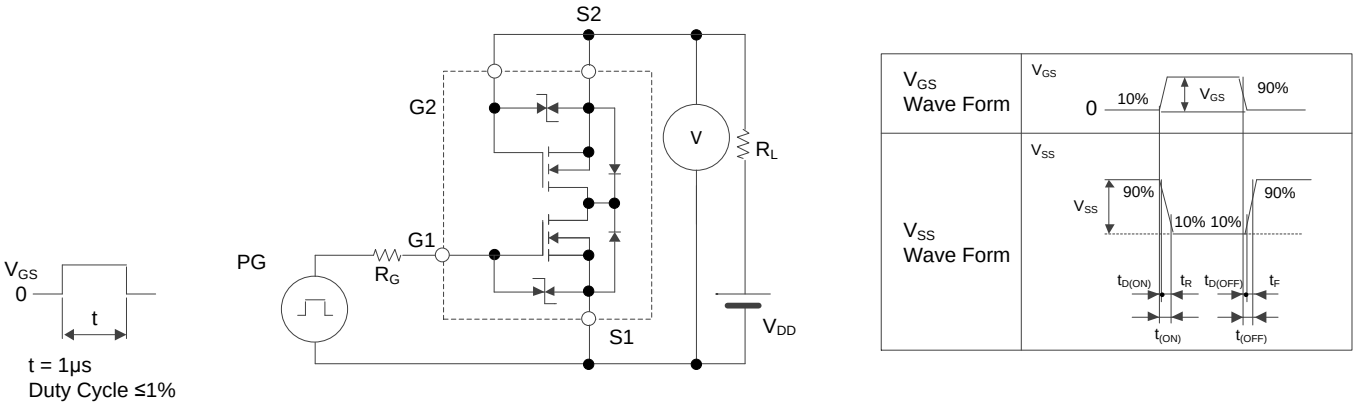


Test Circuit 6 $V_{F(S-S)}$
When FET1 is measured, FET2 is added V_{GS} +4.5V.

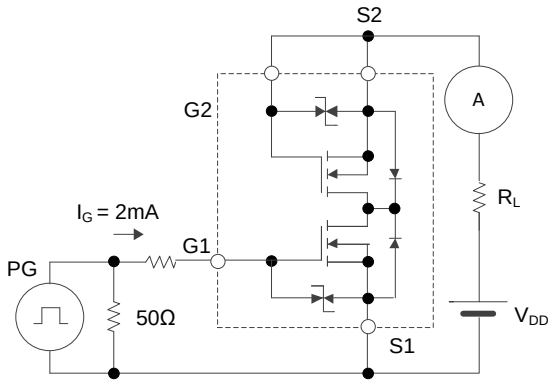
Test Circuits (Cont.)



Test Circuit 7



Test Circuit 8 $t_{D(ON)}$, t_R, $t_{D(OFF)}$, t_F

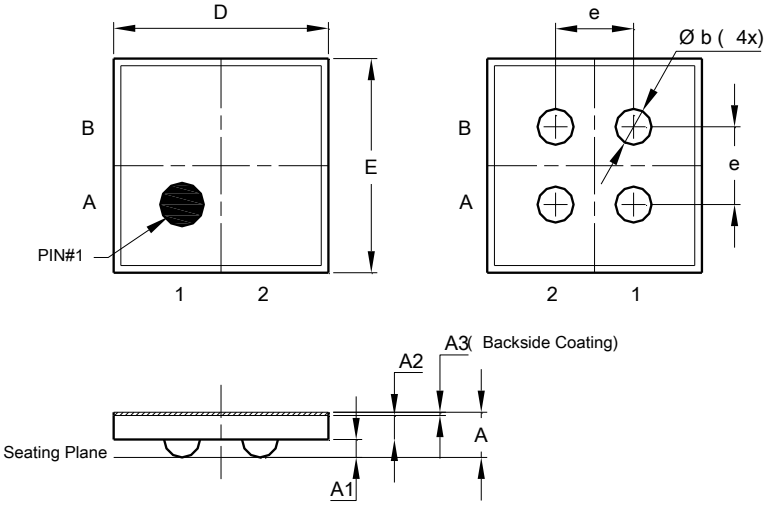


Test Circuit 9 Q_G

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X1-WLB1818-4

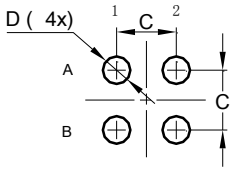


X1-WLB1818-4			
Dim	**Min**	**Max**	**Typ**
A	0.3420	0.4080	0.3750
A1	0.1350	0.1650	0.1500
A2	0.1850	0.2150	0.2000
A3	0.0220	0.0280	0.0250
b	0.2700	0.3300	0.3000
D	1.7800	1.8000	1.7900
E	1.7800	1.8000	1.7900
e	0.650 BSC		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X1-WLB1818-4



Dimensions	Value (in mm)
C	0.65
D	0.30

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

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