2:1 Active HDMI™ Compatible Switch with Optimized Equalization for Enhanced Signal Integrity

Features

- Supply voltage, V_{DD} = 3.3V ±5%
- Each Port can support DVI or HDMI™ signals
- Supports both AC-coupled and DC-coupled inputs
- Supports DeepColor™
- High Performance, up to 2.5 Gbps per channel
- Switching support for 3 side band signals (SCL, SDA and HPD)
- 5V Tolerance on all side band signals
- SCL, SDA, and HPD pins are the only pins that can support HOT INSERTION
- Integrated 50-Ohm (±10%) termination resistors at each high speed signal input
- TMDS input termination control on all high speed inputs
- HDCP reset circuitry for quick communication when switching from one port to another
- Configurable output swing control (500mV, 750mV, 1000mV)
- Configurable Pre-Emphasis levels (0dB, 1.5dB, 3.5dB, & 6.0dB)
- Configurable De-Emphasis (0dB, -3.5dB, -6.0dB, -9.5dB)
- Optimized Equalization
  Single default setting will support all cable lengths
- ESD spec on all input TMDS pins is ±6kV per IEC61000-4-2
- Propagation delay ≤ 2ns
- High Impedance Outputs when disabled
- Packaging (Pb-free & Green): 56-contact TQFN (ZF56)

Description

Pericom Semiconductor's PI3HDMI201 2:1 active switch circuit is targeted for high-resolution video networks that are based on DVI/HDMI™ standards and TMDS signal processing. The PI3HDMI201 is an active 2 TMDS to 1 TMDS receiver switch with Hi-Z outputs. The device receives differential signals from selected video components and drives the video display unit. It provides three controllable output swings. The allowable output swings are 500mV, 750mV and 1000mV. This solution also provides a unique advanced pre-emphasis technique to increase rise and fall times which are reduced during transmission across long distances.

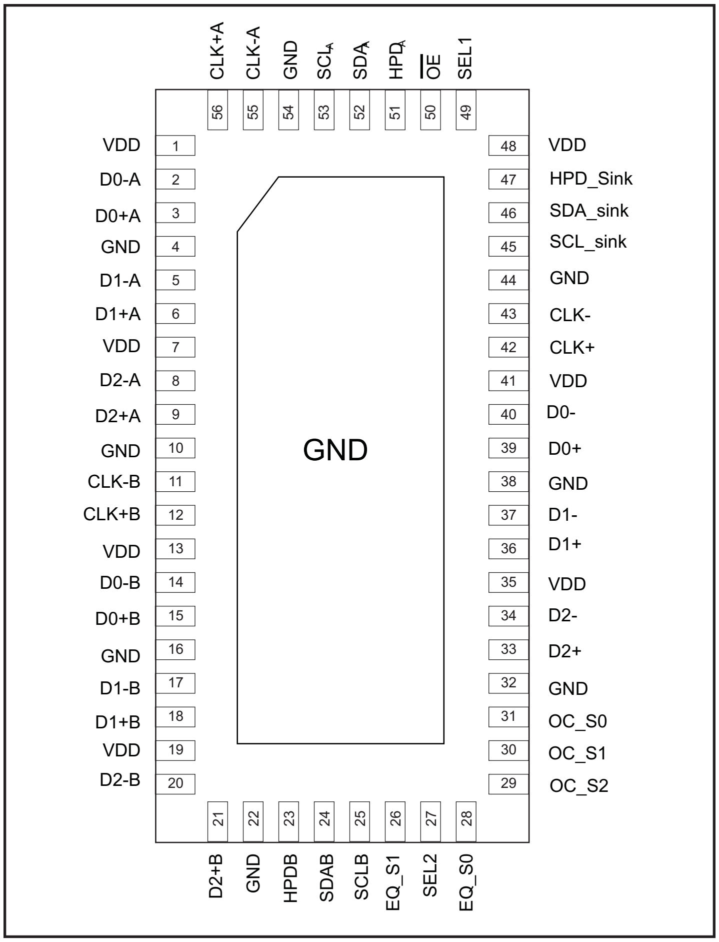
Each complete HDMI/DVI channel also has slower speed, side band signals, that are required to be switched. Pericom's solution provides a complete solution by integrating the side band switch together with the high speed switch in a single solution. Using Equalization at the input of each of the high speed channels, Pericom can successfully eliminate deterministic jitter caused by long cables from the source to the sink. The elimination of the deterministic jitter allows the user to use much longer cables (up to 25 meters).

The maximum DVI/HDM Bandwidth of 2.5 Gbps provides 36-bit DeepColor™ support, which is offered by HDM revision 1.3. Due to its active uni-directional feature, this switch is designed for usage only for the video receiver's side. For consumer video networks, the device sits at the receiver's side to switch between multiple video components, such as PC, DVD, STB, D-VHS, etc. The PI3HDMI201 also provides enhanced robust ESD/EOS protection of ±6kV, which is required by many consumer video networks today.

The Optimized Equalization provides the user a single optimal setting that can provide HDMI compliance in regards to jitter for all cable lengths: 1meter to 20meters and color depths of 8bit/ch, or 12bit/ch.

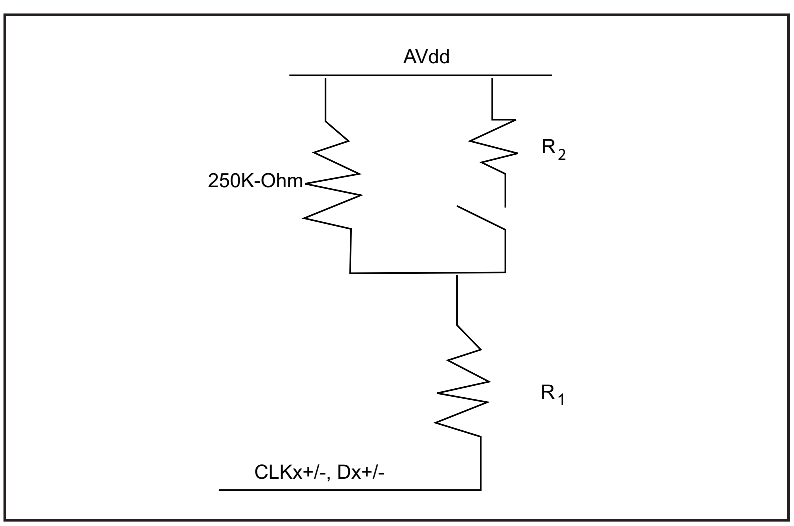
Pericom also offers the ability to fine tune the equalization settings in situations where cable length is known. For example, if 25meter cable length is required, Pericom's solution can be adjusted to 16dB EQ to accept 25meter cable length.

Pin Configuration (Top View)



Receiver Block

Each input has integrated equalization that can eliminate deterministic jitter caused by 25meter 24AWG cables. All activity can be configured using pin strapping. The Rx block is designed to receive all relevant signals directly from the HDMI™ connector without any additional circuitry, 3 High speed TMDS data, 1 pixel clock, 1 HPD signal, and DDC signals. TMDS channels have following termination scheme for Rx Sense support.

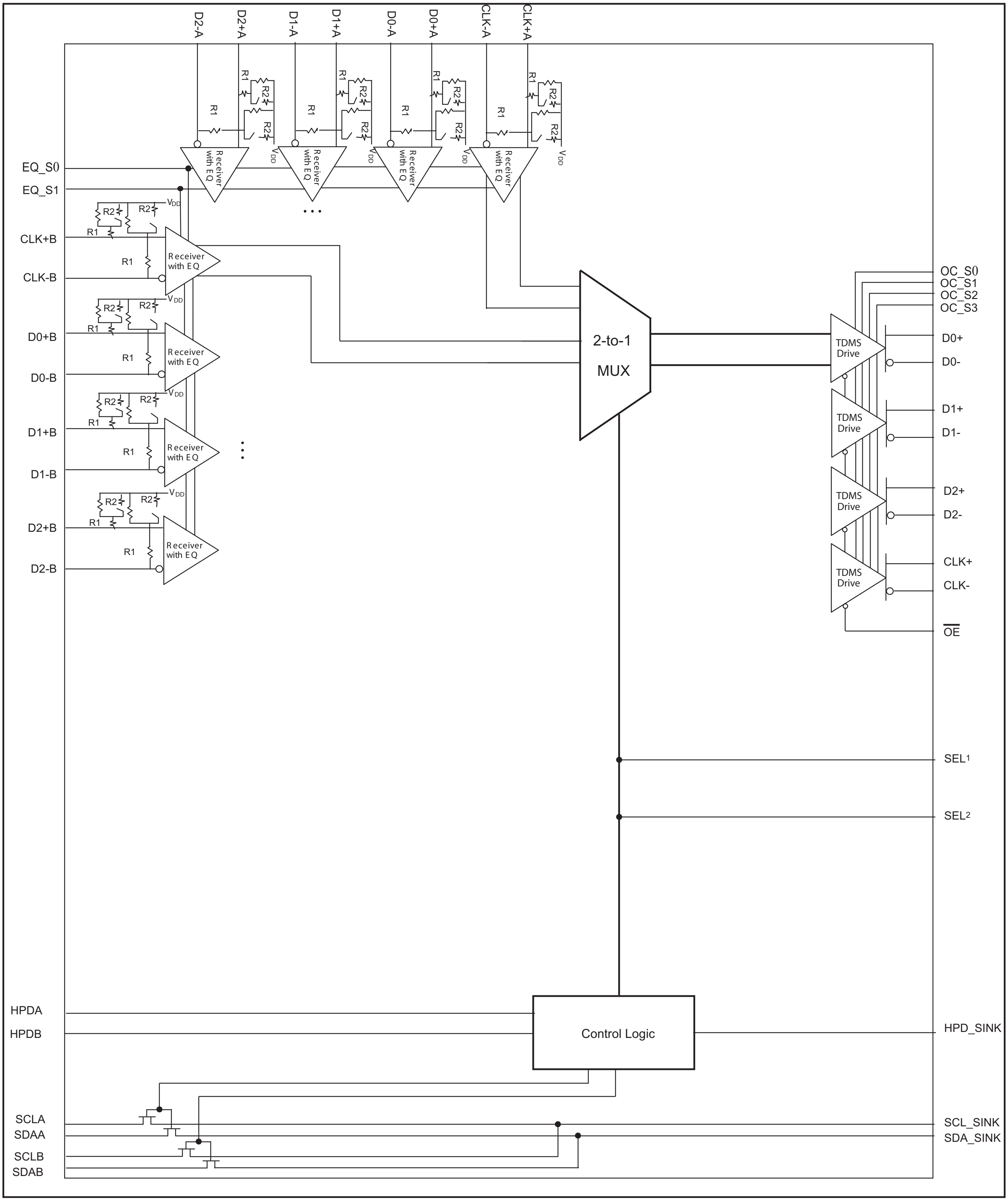


x = A or B

Pin Description

Pin #	Pin Name	I/O	Description
3 6 9 56	D_0+A D_1+A D_2+A CLK+A	I	Port A TMDS Positive inputs
15 18 21 12	D_0+B D_1+B D_2+B CLK+B	I	Port B TMDS Positive inputs
2 5 8 55	D_0-A D_1-A D_2-A CLK-A	I	Port A TMDS Negative inputs
14 17 20 11	D_0-B D_1-B D_2-B CLK-B	I	Port B TMDS Negative inputs
4, 10, 16, 22, 32, 38, 44, 54	GND		Ground
51	HPD_A	O	Port A HPD output
23	HPD_B	O	Port B HPD output
47	HPD_Sink	I	Sink side hot plug detector input.
50	$\overline{OE}$	I	Output Enable, Active LOW
53	SCL_A	I/O	Port A DDC Clock
25	SCL_B	I/O	Port B DDC Clock
45	SCL_Sink	I/O	Sink Side DDC Clock
52	SDA_A	I/O	Port A DDC Data
24	SDA_B	I/O	Port B DDC Data
46	SDA_Sink	I/O	Sink Side DDC Data
49	SEL1	I	Source Input Selector (See Truth Table)
1, 7, 13, 19, 35, 41, 48	V_{DD}		3.3V Power Supply
39 36 33 42	D_0+ D_1+ D_2+ CLK+	O	TMDS positive outputs
40 37 34 43	D_0- D_1- D_2- CLK-	O	TMDS negative outputs
28 26	EQ_S0 EQ_S1	I	Equalizer controls, Internal pull-ups are added to both.
31 30 29	OC_S0 OC_S1 OC_S2	I	Output buffer controls Note: all 3 pins have internal pull-ups
27	SEL2	I	Source Input Selector (See Truth Table)

Switch Block Diagram



Truth Table

$\overline{OE}$	SEL1	SEL2	Function for TMDS output	HPD_A	HPD_B
0	1	X	Port A is active & TMDS Rx Termination on Port B goes to 250K-Ohm	HPD_sink	L
0	0	1	Port B is active, & TMDS Rx Termination on Port A goes to 250K-Ohm	L	HPD_sink
0	0	0	All TMDS outputs & TMDS inputs are Hi-Z, SCL/SDA (Port A & B) are off	L	L
1	X	X	All TMDS outputs are Hi-Z	Follow SEL1 and SEL2	Follow SEL1 and SEL2

OC Setting Value Logic Table

Input Control Pins			Setting Value	
OC_S2(1)	OC_S1(1)	OC_S0(1)	V_{swing} (mV)	Pre-emphasis (dB)
1	1	1	500	0
1	1	0	750	0
1	0	1	1000	0
1	0	0	600	0
0	1	1	500	0
0	1	0	500	1.5
0	0	1	500	3.5
0	0	0	500	6

Note:

1. Integrated pull-ups

EQ Setting Value Logic Table for high speed data bits (TMDS CLK input is left at 3dB default always)

EQ_S1(1)	EQ_S0(1)	Setting Value
0	0	15dB on all high speed data inputs
0	1	3dB on all high speed data inputs
1	0	8dB on all high speed data inputs
1	1	Optimized Equalization on all high speed data inputs (Default setting which can support all cable lengths from 1meter to 20meters)

Notes:

1) Integrated internal pull-ups

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C
Supply Voltage to Ground Potential .... –0.5V to +4.0V
DC Input Voltage .... –0.5V to V_{DD}
DC Output Current 120mA
Power Dissipation 1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	3.135	3.3	3.465	V
T_A	Operating free-air temperature	0		70	°C
TMDS Differential Pins (D_X±A, D_X±B, CLK±A, CLK±B)					
V_{ID}	Receiver peak-to-peak differential input voltage	150		1560	mVp-p
V_{IC}	Input common mode voltage	2		V_{DD} + 0.01	V
V_{DD}	TMDS output termination voltage	3.135	3.3	3.465	V
R_T	Termination resistance	45	50	55	Ohm
	Signaling rate	0		2.5	Gbps
Control Pins (OC_Sx, EQ_Sx, SEL, $\overline{OE}$)					
V_{IH}	LVTTL High-level input voltage	2		V_{DD}	V
V_{IL}	LVTTL Low-level input voltage	GND		0.8	V
DDC Pins (SCL, SCL_SINK, SDA, SDA_SINK)					
$V_{I(DDC)}$	Input voltage	GND		5.5	V
Status Pins (HPD_SINK)					
V_{IH}	LVTTL High-level input voltage	2		5.3	V
V_{IL}	LVTTL Low-level input voltage	GND		0.8	V

TMDS Compliance Test Results

Item	HDMI™ 1.3 Spec	Pericom Product Spec
Operating Conditions		
Termination Supply Voltage, V_{DD}	3.3V ≤ 5%	3.30 ± 5%
Terminal Resistance	50-Ohm ± 10%	45 to 55-Ohm
Source DC Characteristics at TP1		
Single-ended high level output voltage, VH	V_{DD} ± 10mV	V_{DD} ±10mV
Single-ended low level output voltage, VL	(V_{DD} - 600mV) ≤ VL ≤ (V_{DD} - 400mV)	(V_{DD} - 600mV) ≤ VL ≤ (V_{DD} - 400mV)
Single-ended output swing voltage, Vswing	400mV ≤ Vswing ≤ 600mV	400mV ≤ Vswing ≤ 600mV
Single-ended standby (off) output voltage, Voff	V_{DD} ± 10mV	V_{DD} ± 10mV
Transmitter AC Characteristics at TP1		
Risetime/Falltime (20%-80%)	75ps ≤ Risetime/Falltime ≤ 0.4 Tbit (75ps ≤ tr/tf ≤ 242ps) @ 1.65 Gbps	240ps
Intra-Pair Skew at Transmitter Connector, max	0.15 Tbit (90.9ps @ 1.65 Gbps)	60ps max
Inter-Pair Skew at Transmitter Connector, max	0.2 Tpixel (1.2ns @ 1.65 Gbps)	100ps max
Clock Jitter, max	0.25 Tbit (151.5ps @ 1.65 Gbps)	82ps max
Sink Operating DC Characteristics at TP2		
Input Differential Voltage Level, Vdiff	150 ≤ Vdiff ≤ 1200mV	150mV ≤ V_{DIFF} ≤ 1200mV
Input Common Mode Voltage Level, V_{ICM}	(V_{DD} - 300mV) ≤ Vicm ≤ (V_{DD}-37.5mV) Or V_{DD} ±10%	(V_{DD} - 300mV) ≤ Vicm ≤ (V_{DD}-37.5mV) Or V_{DD} ±10%
Sink DC Characteristics When Source Disabled or Disconnected at TP2		
Differential Voltage Level	V_{DD} ± 10mV	V_{DD} ±10mV

Electrical Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
I_{CC}	Supply Current	$V_{IH} = V_{DD}$, $V_{IL} = V_{DD}$ - 0.4V, R_T = 50-Ohm, V_{DD} = 3.3V, OC_SX = LOW, x = 0, 1, 2		120		mA
P_D	Power Dissipation			400		mW
I_{CCQ}	Standby Current	$\overline{OE}$ = HIGH, SEL1 = Low, SEL2 = Low, V_{DD}=3.3V		8		mA
TMDS Differential Pins (D_X±A, D_X±B, D_X±, CLK±A, CLK±B, CLK±)						
V_{OH}	Single-ended high-level output voltage	V_{DD} = 3.3V, R_T = 50-Ohm Pre-emphasis/De-emphasis = 0dB	V_{DD}- 10		V_{DD} + 10	mV
V_{OL}	Single-ended low-level output voltage		V_{DD} - 600		V_{DD} - 400	
V_{swing}	Single-ended output swing voltage		400		600	
$V_{OD(O)}$	Overshoot of output differential voltage			6%	15%	2x V_{swing}
$V_{OD(U)}$	Undershoot of output differential voltage			12%	25%	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			0.5	5	mV
$\lvert I_{(OS)}\rvert$	Short circuit output current				12	mA
$V_{ODE(SS)}$	Steady state output differential voltage	OC_Sx = GND, Dx±AB = 250 Mbps HDMI™ data pattern, X = 0, 1, 2 CLK±A, B = 25 MHz clock	560		840	mVp-p
$V_{ODE(PP)}$	Peak-to-peak output differential voltage		800		1200	
$V_{I(open)}$	Single-ended input voltage under high impedance input or open input	I_I = 10µA	V_{DD} - 10		V_{DD} + 10	mV
R_{INT}	Input termination resistance	V_{IN} = 2.9V	45	50	55	Ohm
DDC I/O Pins (SCL, SCL_SINK, SDA, SDA_SINK)						
$\lvert I_{lkg}\rvert$	Input leakage current	V_I = 5.5V	-50		50	µA
		$V_I = V_{DD}$	-20		20	
C_{IO}	Input/output capacitance	V_I = 0V		7.5		pF
R_{ON}	Switch resistance	I_O = 3mA, V_O = 0.4V		25	50	Ohm
V_{PASS}	Switch output voltage	V_I = 3.3V, I_I = 100µA	1.5(2)	2.0	2.5(3)	V
Status Pins (HPD)						
$V_{OH(TTL)}$	TTL High-level output voltage	I_{OH} = -4mA	2.4			V
$V_{OL(TTL)}$	TTL Low-level output voltage	I_{OL} = 4mA			0.4	V

(Table Continued)

Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.[1]	Max.	Units
Control Pins (SEL, $\overline{OE}$)						
$\lvert I_{IH} \rvert$	High-level digital input current	V_{IH}= 2.0V or V_{DD}	-10		10	µA
$\lvert I_{IL} \rvert$	Low-level digital input current	V_{IL} = GND or 0.8V	-10		10	
Status Pins (HPD_SINK)						
$\lvert I_{IH} \rvert$	High-level digital input current	V_{IH} = 5.3V	-50		50	µA
		V_{IH} = 2.0V or V_{DD}	-10		10	
$\lvert I_{IL} \rvert$	Low-level digital input current	V_{IL} = GND or 0.8V	-10		10	

Notes:

1. All typical values are at 25°C and with a 3.3V supply.
2. The value is tested in full temperature range at 3.0V.
3. The value is tested in full temperature range at 3.6V.

Switching Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.[1]	Max.	Units
TMDS Differential Pins (Dx±, CLK±)						
tpd	Propagation delay	V_{DD} = 3.3V, R_T = 50-Ohm, pre-emphasis/de-emphasis = 0dB			2000	ps
t_r	Differential output signal rise time (20% - 80%)		75		240	
t_f	Differential output signal fall time (20% - 80%)		75		240	
$t_{sk(p)}$	Pulse skew			10	50	
$t_{sk(D)}$	Intra-pair differential skew			23	50	
$t_{sk(o)}$	Inter-pair differential skew[2]				100	
$t_{jit(pp)}$	Peak-to-peak output jitter from CLK± residual jitter	pre-emphasis/de-emphasis = 0dB, Dx±A, B = 1.65 Gbps HDMI™ data pattern, x = 0, 1, 2 CLK±A, B = 165 MHz clock		15	30	
$t_{jit(pp)}$	Peak-to-peak output jitter from Dx± residual jitter			18	50	
t_{DE}	De-emphasis duration	de-emphasis = -3.5dB, Dx±A, B = 250 Mbps HDMI™ data pattern, x = 0, 1, 2 CLK±A, B = 25 MHz clock		240		
t_{SX}	Select to switch output				10	ns
t_{en}	Enable time				200	
t_{dis}	Disable time				10	
DDC I/O Pins (SCL, SCL_SINK, SDA, SDA_SINK)						
$t_{pd(DDC)}$	Propagation delay from SCLn to SCL_SINK or SDAn to SDA_SINK or SDA_SINK to SDAn	C_L = 10pF		0.4	2.5	ns
Control and Status Pins (SEL, HPD_SINK, HPD)						
$t_{pd(HPD)}$	Propagation delay (from HPD_SINK to the active port of HPD)	C_L = 10pF		2	6.0	ns
$t_{sx(HPD)}$	Switch time (from port select to the latest valid status of HPD)			3	6.5	

Notes:

1. All typical values are at 25°C and with a 3.3V supply.
2. $t_{sk(o)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel 2 to 4 of a device when inputs are tied together.

Application Information

Supply Voltage

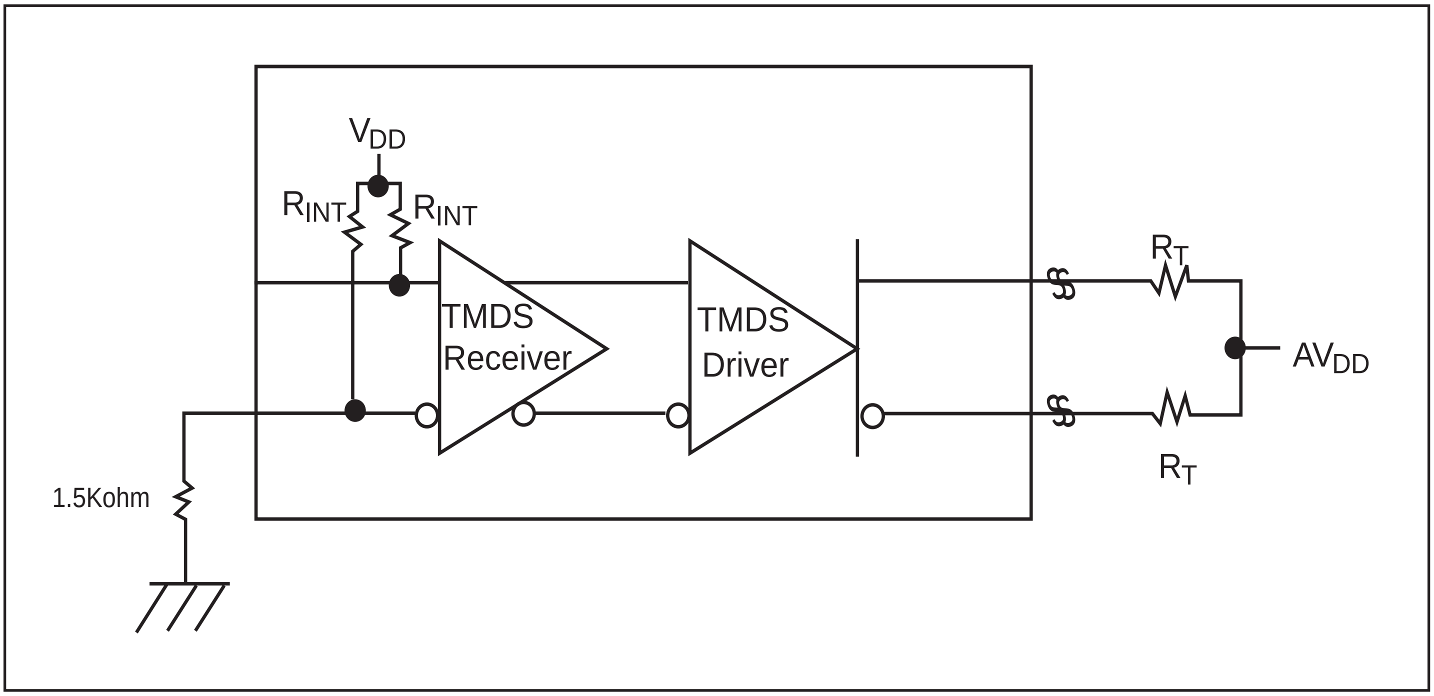
All V_{DD} pins are recommended to have a 0.1µF capacitor tied from V_{DD} to GND to filter supply noise

TMDS inputs

Standard TMDS terminations have already been integrated into Pericom's PI3HDMI201 device. Therefore, external terminations are not required. Any unused port must be left floating and not tied to GND.

TMDS output oscillation elimination

The TMDS inputs do not incorporate a squelch circuit. Therefore, we recommend the input to be externally biased to prevent output oscillation. One pin will be pulled high to V_{DD} with the other grounded through a 1.5KOhm resistor as shown.



TMDS Input Fail-Safe Recommendation

Recommended Power Supply Decoupling Circuit

Figure 1 is the recommended power supply decoupling circuit configuration. It is recommended to put 0.1µF decoupling capacitors on each V_{DD} pins of our part, there are four 0.1µF decoupling capacitors are put in Figure 1 with an assumption of only four V_{DD} pins on our part, if there is more or less V_{DD} pins on our Pericom parts, the number of 0.1µF decoupling capacitors should be adjusted according to the actual number of V_{DD} pins. On top of 0.1µF decoupling capacitors on each V_{DD} pins, it is recommended to put a 10µF decoupling capacitor near our part's V_{DD}, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.

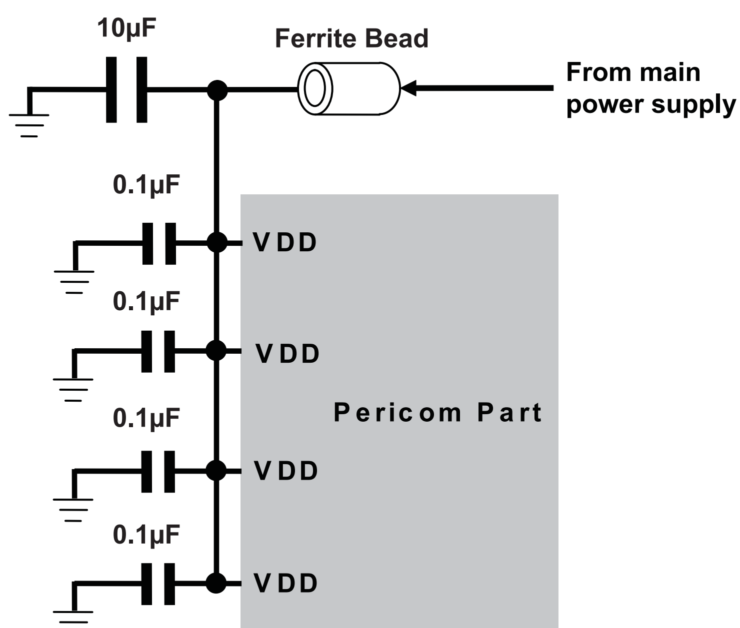


Figure 1 Recommended Power Supply Decoupling Circuit Diagram

Requirements on the Decoupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

Layout and Decoupling CapacitorPlacement Consideration

i. Each 0.1µF decoupling capacitor should be placed as close as possible to each V_{DD} pin.
ii. V_{DD} and GND planes should be used to provide a low impedance path for power and ground.
iii. Via holes should be placed to connect to V_{DD} and GND planes directly.
iv. Trace should be as wide as possible
v. Trace should be as short as possible.
vi. The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
vii. 10µF capacitor should also be placed closed to our part and should be placed in the middle location of 0.1µF capacitors.
viii. Avoid the large current circuit placed close to our part; especially when it is shared the same V_{DD} and GND planes. Since large current flowing on our V_{DD} or GND planes will generate a potential variation on the V_{DD} or GND of our part.

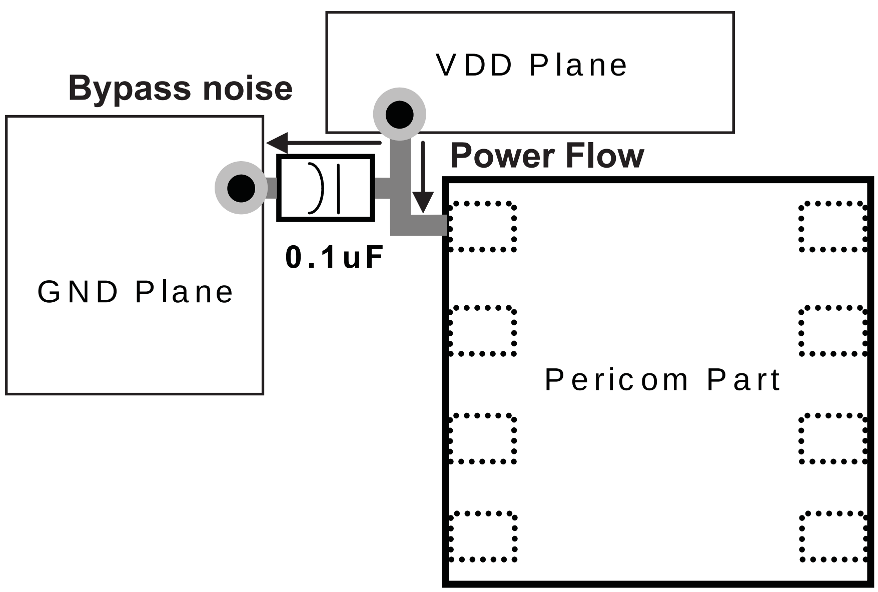
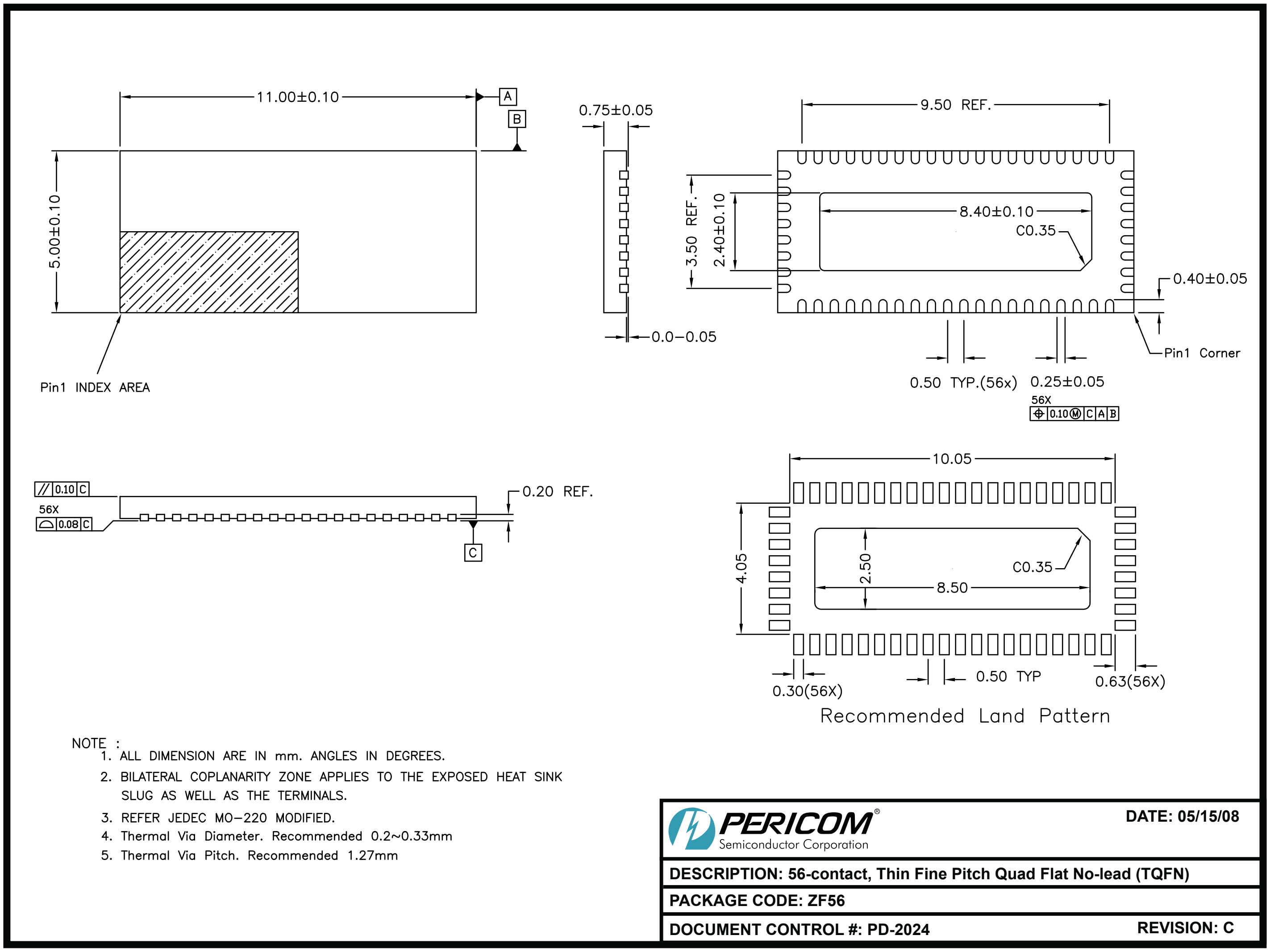


Figure 2 Layout and Decoupling Capacitor Placement Diagram

Package Mechanical: 56-pin, Low Profile Quad Flat Package (ZF56)



08-0208

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDMI201ZFE	ZF	56-pin, Pb-free & Green TQFN

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel
- HDMI & DeepColor are trademarks of Silicon Image

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