

PI3HDMI511A
PI3HDMI511A HDMI Application Information

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1 Introduction

PI3HDMI511A is an HDMI 1.4 re-driver for source application. It can re-drive TMDS signals coming from dual-mode DP source or HDMI source. As HDMI data rate can be faster than 2.2Gbps, signal integrity is critical. Source termination is therefore implemented in PI3HDMI511A to high-speed transmission. External components in typical application circuit and layout guideline are described in this application information.

2 External Component Requirements

PI3HDMI511A is designed to accept AC-coupled as well as DC-coupled main link signals.

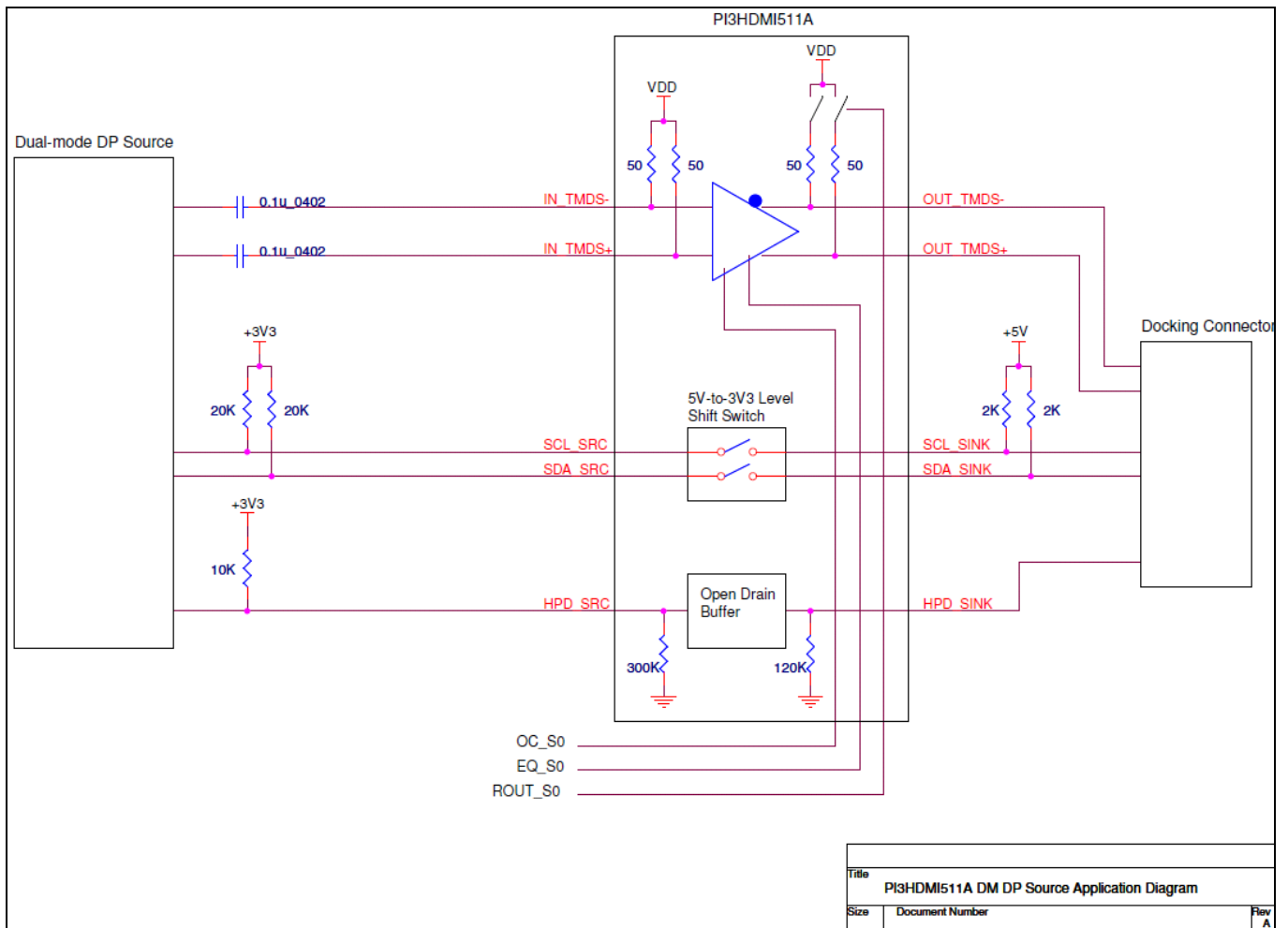


Figure 1: PI3HDMI511A HDMI Source Application

2.1 AC Coupling Capacitors on Output Main Link

For dual-mode DP source, AC coupling capacitors should be placed before where TMDS signals enter PI3HDMI511A if signals from the dual-mode DP source are DC coupled.

2.2 Pull-up Resistors on DDC Channel

Each of SCL and SDA is pulled up to 3.3V via a 20kΩ resistor to create a high voltage level for dual-mode DP source. The 2kΩ pull-ups to 5V are the requirement of HDMI Specification Version 1.4. As 5V-to-3.3V level shifter is implemented in the design, external FET is not required.

2.3 Pull-up Resistor on HPD Channel

As HPD_SRC of PI3HDMI511A is an open drain buffer design, external pull-up should be implemented.

3 Layout Design Guideline

Layout guideline especially for high-speed transmission is critical. Please refer to PIxxxx High Speed Layout Guideline, AN345, for detailed recommendations.

4 References

- (1) VESA DisplayPort Standard Version 1 Revision 2, Video Electronics Standards Association, January 5, 2010
- (2) VESA DisplayPort Dual-Mode Standard Version 1, Video Electronics Standards Association, February 10, 2012
- (3) VESA DisplayPort Interoperability Guideline Version 1.1a, Video Electronics Standards Association, February 5, 2009
- (4) High-Definition Multimedia Interface Specification Version 1.4b, HDMI Licensing, LLC, October 11, 2011
- (5) PCI Express Board Design Guidelines Draft, Intel Corporation, June 2003

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